



AN930.3:Series 3 2.4 GHz Matching Guide

The Series 3 devices include chip variants that provide 2.4 GHz operation.

This application note describes the matching techniques applied to the SixG301 in the 2.4 GHz band.

For information on PCB layout requirements for proper 2.4 GHz operation, refer to [AN928.3:Series 3 Layout Design Guide](#).

KEY POINTS

- Description of the applied 2.4 GHz matching networks and techniques for the Series 3 devices
- Detailed discussion of the design steps and design examples
- Measured TX fundamental and harmonic performance
- Measured receive sensitivity values

Table of Contents

1. Device Compatibility	3
2. Introduction	4
2.1 Related Literature	4
3. RF Architecture Overview	5
3.1 SixG301 Front-End Overview	5
4. 2.4 GHz RF Matching Design Steps	6
4.1 Determining the Optimum Termination Impedance for the PA	6
4.1.1 SixG301 Optimum PA Load Impedance	6
4.2 Choosing the RF Matching Topology	6
4.3 Initial Design with Ideal, Loss-Free Elements	7
4.4 Design with Parasitics and Losses	8
5. VNA Measurements	10
6. Recommended Matching Networks	11
6.1 SixG301 Matching Networks for QFN Packages for Both 0/ +10 dBm PA	.11
6.2 Measurement Results	.12
7. Revision History	13

1. Device Compatibility

This application note supports the SixG301 family and its related OPNs.

- SiMG301
- SiBG301

2. Introduction

This application note is intended to help users achieve the best 2.4 GHz RF match for targeted applications. It describes the details of matching network design procedures and presents additional test results.

4-element discrete LC match with an additional series dc-blocking capacitor is used for SixG301 SoC to achieve 0 dBm and +10 dBm output power using their dedicated PAs.

The 4x4 mm 32-pin and 5x5 mm 40-pin QFN package pinouts are shown in the following figures. The 2.4 GHz RF I/O pins are highlighted with a red box.

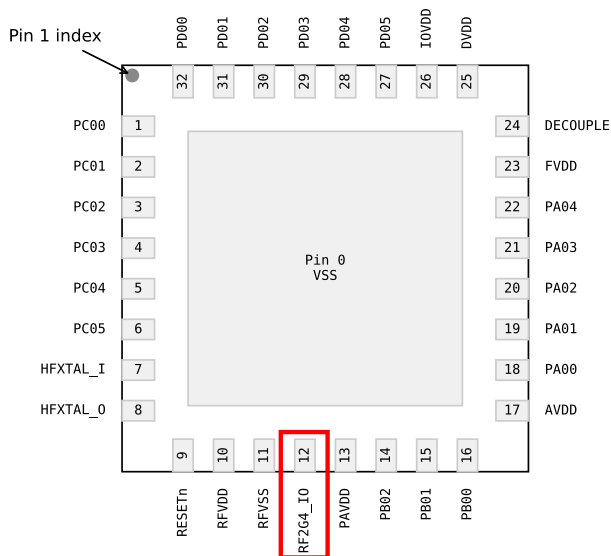


Figure 2.1. SixG301 QFN32 (RF I/O Pins Highlighted)

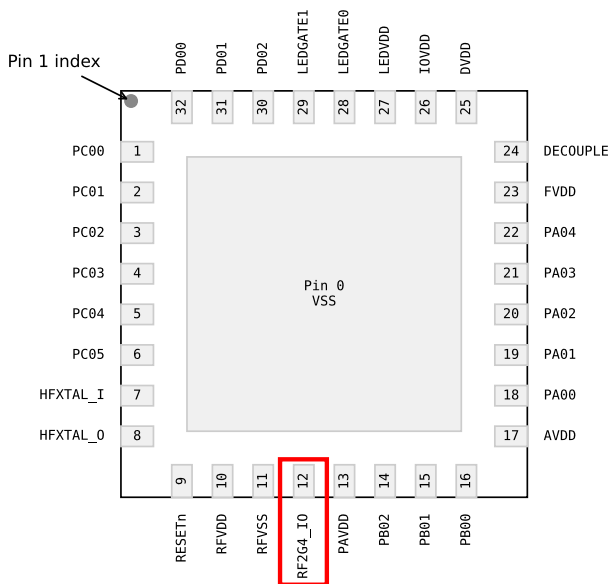


Figure 2.2. SixG301 QFN40 (RF I/O Pin Highlighted)

2.1 Related Literature

Related documentation includes:

- [AN928.3: Series 3 Layout Design Guide](#)
- [AN0002.3: Series 3 Hardware Design Considerations](#)

3. RF Architecture Overview

3.1 SixG301 Front-End Overview

The on chip part of the front-end comprises two PA structures optimized for the TX power levels of 0 and +10 dBm and a single ended LNA. Only +10 dBm PA is biased through the PAVDD pin. On the chip package a single RF I/O port is available. Externally, a single-ended, combined matching/filtering network is required.

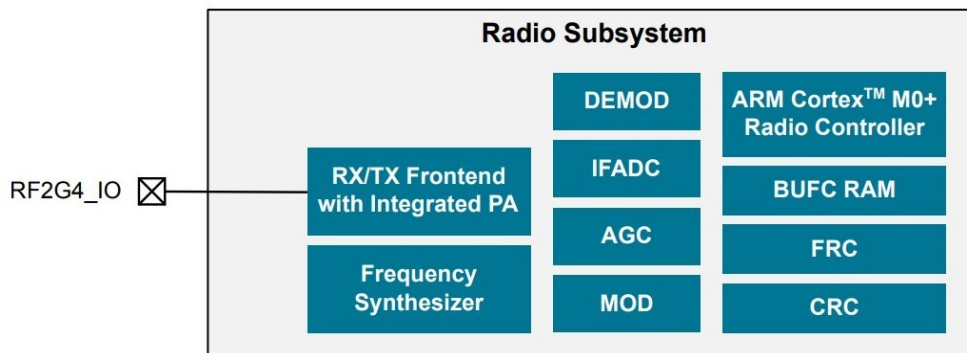


Figure 3.1. SixG301 Radio Subsystem

A few highlights on the RF front-end blocks:

- Class-D PA, optimized for +10/0 dBm TX power levels.
 - QFN32/40 +10 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.675 V
 - QFN32/40 0 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.64 V

4. 2.4 GHz RF Matching Design Steps

2.4 GHz RF matching design for Series 3 SixG301 chips consists of the following steps:

1. Determine the optimum termination impedance for the PA.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the pcb have a major effect, so tuning/optimization of the design is required. Here an optional EM simulation can be done, but simulations with well-estimated pcb parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

Note:

1. The first step has been performed by Silicon Labs and is an attribute of the internal PA. These determined values can be used as a basis for custom matching network designs and there is no need to re-measure them by the user.
2. Steps 2 to 5 are only necessary if the matching network and layout design are different from the recommendations in this application note. If the reader follows these matching and layout guidelines strictly, RF performance is expected to be close to that of the Silicon Labs radio boards, and simulation/bench tuning may not be needed.

4.1 Determining the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the RF2G4_IO pin if 50 Ω termination is applied at the antenna port.

The RF2G4_IO RF port termination determines the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX mode. In addition, proper harmonic suppression and good RX sensitivity in reception mode are required.

4.1.1 SixG301 Optimum PA Load Impedance

The optimum PA load impedance values are listed below. The impedance values are given at the chip pin looking into the RF matching network.

- For both 0 dBm/ +10 dBm PA: $Z_{pin} = 13.4 + j4$

4.2 Choosing the RF Matching Topology

In addition to creating an optimum termination impedance on the IC side, the matching solution must exhibit sufficiently robust harmonic filtering characteristics to comply with emissions standards. There are many different types of RF matching topologies. Separate matching and harmonic filtering sections can be utilized, or they can be combined in one circuit, which is the recommended for SixG301. To minimize the number of elements, all matches presented here are of the combined type, with low-pass circuits employed for their inherent harmonic suppression characteristics.

SixG301 matching topology:

- 4- element combined discrete LC match for both 0 and +10 dBm PA, i.e., for power levels equal or below +10 dBm

4.3 Initial Design with Ideal, Loss-Free Elements

After choosing the appropriate topology for the application based on the TX power level requirements, the third step of the matching design procedure is to generate a lumped element schematic of the match with ideal loss-free elements and without PCB parasitics. The matching circuit should show an input impedance of Z_{load_opt} at the RF IO port of the chip while it is terminated by $50\ \Omega$ load at its output (ANT port). The impedance matching procedure is shown in the next sections, where, for simplification, the matching design is started from a termination impedance (Z_L) which is the complex conjugate of the Z_{load_opt} impedance. The reason is that the matching network will show the required Z_{load_opt} impedance at its RF port only if it is perfectly matched there to a termination impedance which is the complex conjugate of the Z_{load_opt} impedance.

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free ideal capacitors and inductors are used, and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization. The impedance transformation procedure for PA of SixG301 is shown in the Smith Chart figures below.

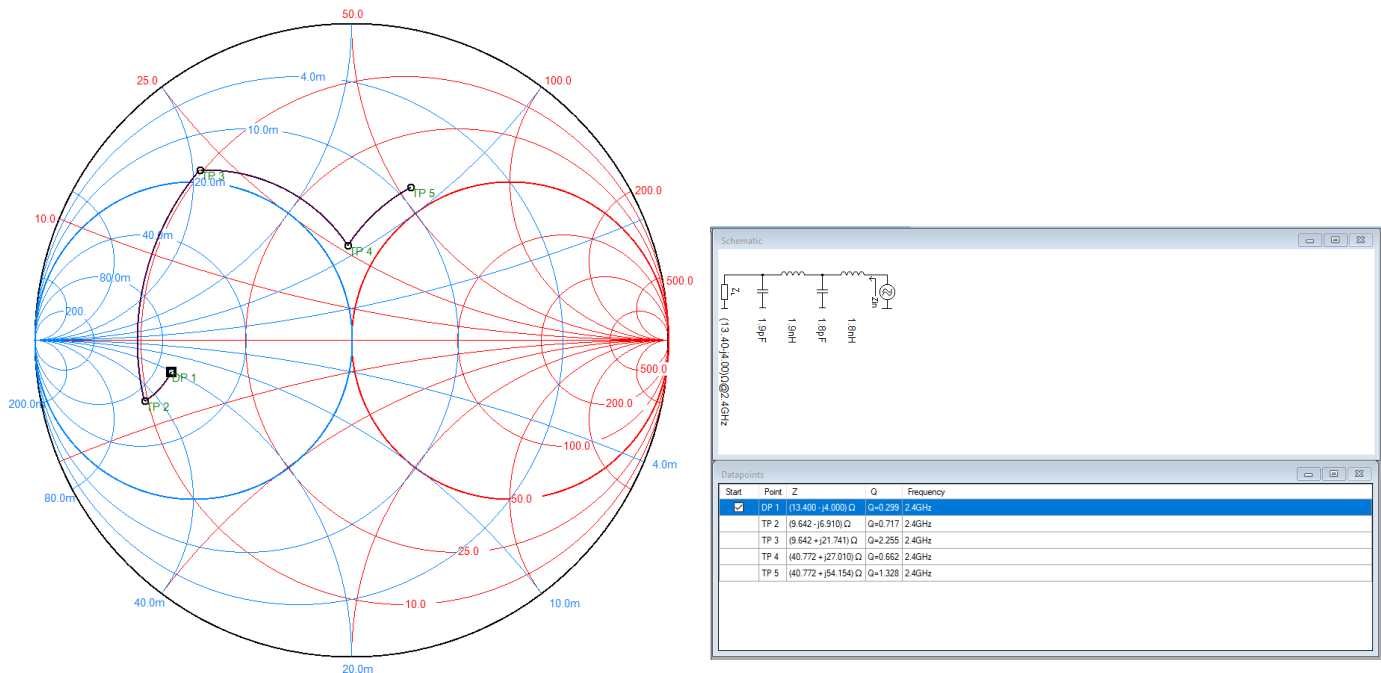


Figure 4.1. SixG301 4-element Match with SMD Tuned for the 0/+10 dBm Power Level

At first glance, it can seem that the matching criteria is underwhelming, as the resulting $40 + j50\ \Omega$ impedance from the ANT point of view is far from $50\ \Omega$. In fact, in terms of S-parameters, it translates to $S_{11} = -5.6\ \text{dB}$, which is rather large reflection coefficient, resulting in an estimated $S_{21} = 1.4\ \text{dB}$ insertion loss due to the mismatch.

However, in the next chapter, it is demonstrated that rightfully (and necessarily) considering the PCB layout and SMD component parasitics in the simulation, the matching criteria is adequately fulfilled.

4.4 Design with Parasitics and Losses

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the used SMD components and the PCB parasitic effects need to be considered during the matching network design. The SMD components at these high-frequency ranges behave as a resonator. A capacitor can be realized by a series RLC resonant circuit, meanwhile an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L-C components, and can have considerable series parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. For more details, please check SMD manufacturer website at www.murata.com, about the appropriate SMD equivalent circuits.

SMD components with different sizes have different parasitics, so it is also important to calculate with the appropriate values. Silicon Labs reference designs use **SMD 0201** components.

The PCB parasitics also have effects on the RF performance versus tuned component values of the matching network. Silicon Labs reference design matching network component values are typically given with a 4-layer PCB with a separation of about 300 μm between the top (component-side) and first inner layer. This distance mostly determines the parasitics capacitance and via inductance, which influences the return-path impedance between the matching network and chip GND (especially at the harmonics). Also, the series trace placed between the chip pin and matching network is part of the match, the dimensions of which should be followed carefully from Silicon Labs reference designs. Refer to [AN928.2: EFR32 Series 2 Layout Design Guide](#) for more layout details.

In the case of using different PCB stack-up (e.g. 2-layer PCB with board thickness > 300 μm), the matching network component values need tuning to keep the RF performance values, especially the harmonic suppressions.

The recommended matching network for the RF port is shown in the section [6. Recommended Matching Networks](#). The circuit provides the optimum impedance load for the SixG301 part while ensuring sufficient harmonic suppression. Some of the shunt capacitors are tuned to have self-resonance at the frequency ranges falling close to TX harmonics and therefore, they provide enhanced attenuation at specific harmonics. The impedance transformation procedure for PA of SixG301 is shown in the Smith Chart figures below.

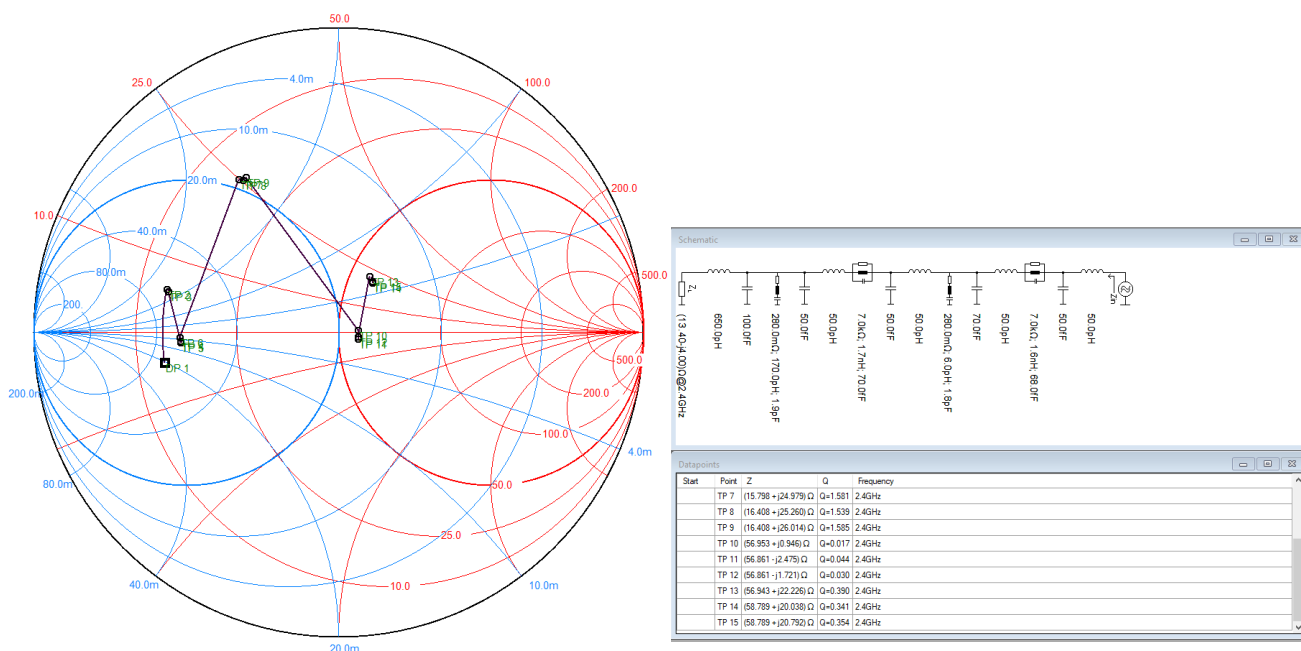


Figure 4.2. SixG301 4-element Match with SMD and PCB Layout Parasitics

The figure below shows simulation results using CST Studio which a 3D EM Field Solver. The main advantage of using such solvers is that it characterizes the PCB parasitics more accurately than the user can do with lumped model estimations. Generally, more accurate simulation results can be yielded when a 3D Field Solvers is used instead of handling the PCB layout and SMD components parasitics as lumped effects.

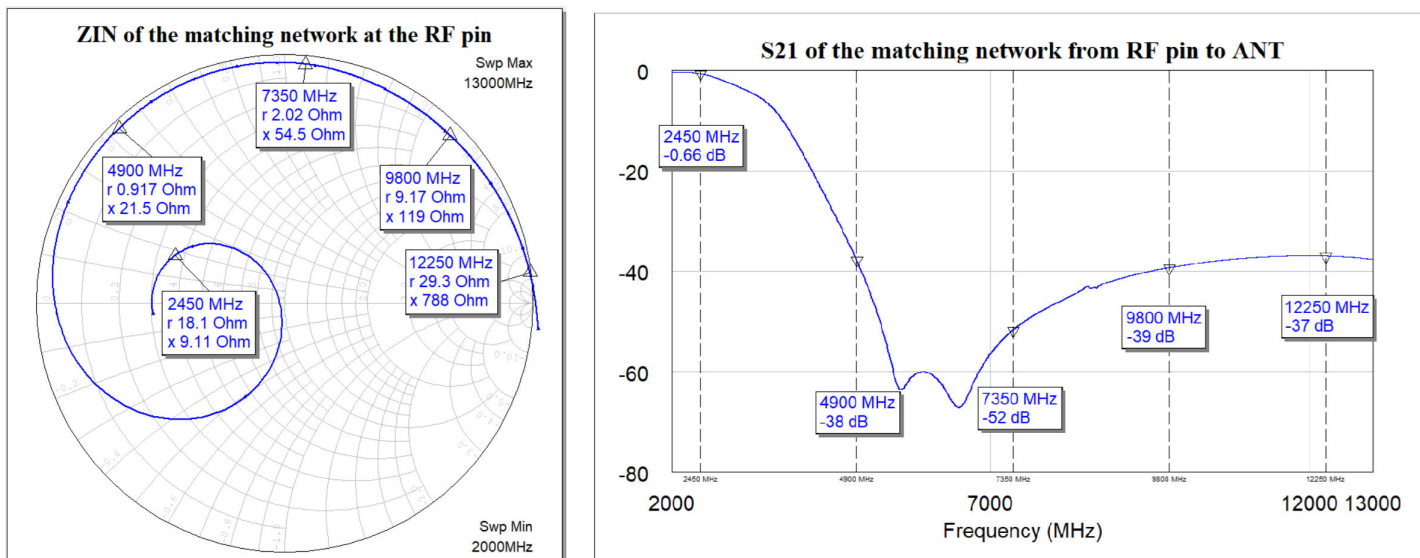


Figure 4.3. S11 and S21 Simulation of 4-element Match with CST Model

The EM Field Solver simulations suggest that the recommended RF front-end is targeting the $13.4 + j4 \Omega$ design goal with adequate accuracy ($S_{11} = -12$ dB (not shown) and $S_{21} = -0.6$ dB). Additionally, good S_{21} harmonic filtering properties can be observed.

5. VNA Measurements

The figure below shows the 2-port S-parameter measurements of the BRD4408A matching network. The measurements were taken using a Vector Network Analyzer (VNA), with proper calibration to the end of the measurement probes which were soldered onto the input (with IC removed) and output of the matching network (ANT port).

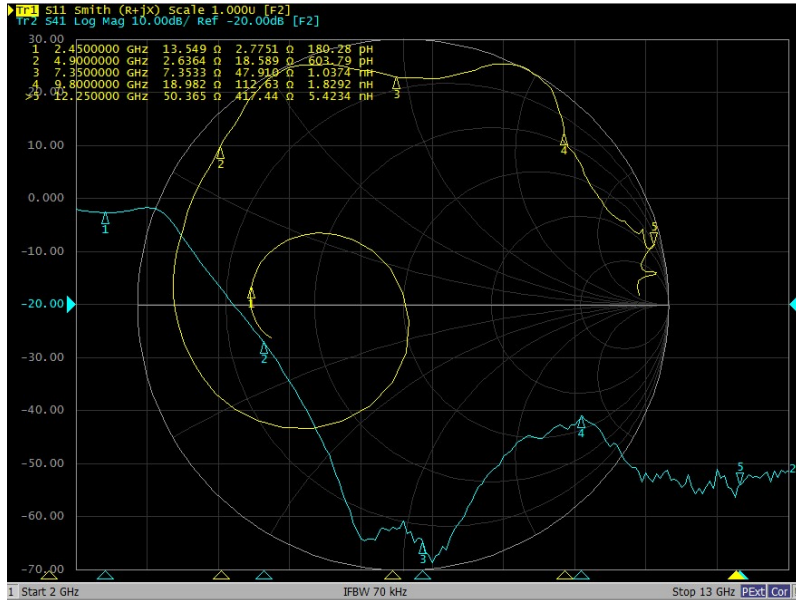


Figure 5.1. Matching Network ZIN Input Impedance (Yellow) and S21 Transfer Characteristics (Blue) Measurements up to 13 GHz

6. Recommended Matching Networks

6.1 SixG301 Matching Networks for QFN Packages for Both 0/ +10 dBm PA

Use the matching network shown below with SixG301 for a maximum transmitting power requirement of +10 dBm. The series dc-blocking capacitor is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +10 dBm, i.e., simultaneously optimized with the 0 and +10 dBm PA as well.

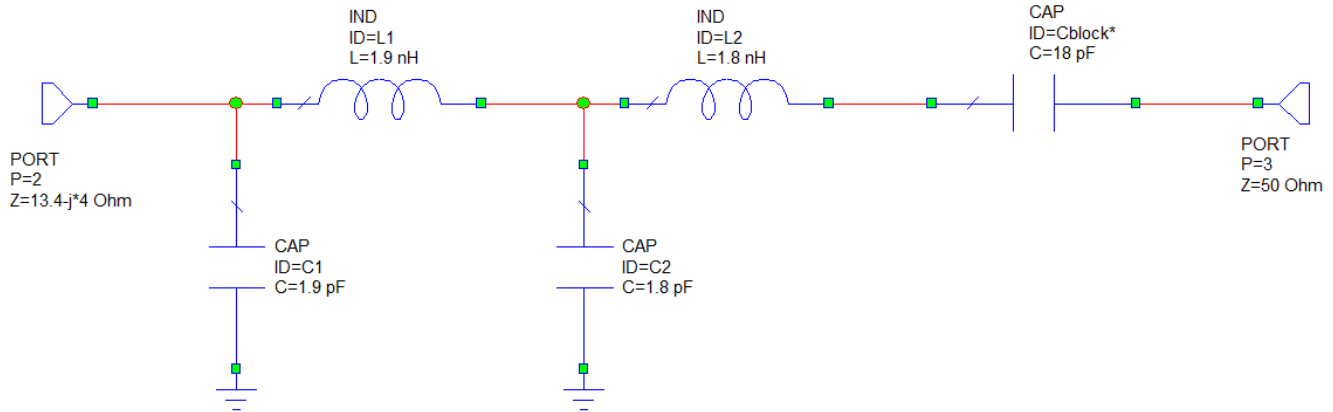


Figure 6.1. Combined Matching Network Schematic for Both 0 and +10 dBm PA (QFN Package)

The matching network component values are optimized for a 4-layer PCB with a separation of 300 μm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 μm .

Table 6.1. Final SMD Values for the 0/ +10 dBm PA Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.05 pF	GRM0335C1H1R9WA01	Murata
L1	1.9 nH	± 0.05 nH	LQP03HQ1N9W02	Murata
C2	1.8 pF	± 0.05 pF	GRM0335C1H1R8WA01	Murata
L2	1.8 nH	± 0.05 nH	LQP03HQ1N8W02	Murata
C block* (0 dBm PA Only)	18 pF	$\pm 2\%$	GJM0335C1E180GB01	Murata

6.2 Measurement Results

Table 6.2. Measurement Results for Each Power Level (PA), Avg., Conducted

Match	PA	RX Sensitivity [dBm]	TX Power [dBm]	PA Current [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
0/ + 10 dBm	0 dBm	-98.6	0	11.4	-60.91	-72.39	-90.21	-89.95
0/ + 10 dBm	+10 dBm		10	28.6	-53.17	-73.79	-85.5	-84.92

Note:

1. The maximum achievable output power of the 0 dBm and +10 dBm PA are +1.9 dBm and +11.9 dBm.
2. RX Sensitivity test conditions: 1 Mbps 500 kHz 2GFSK PHY, BER < 0.1 %.

7. Revision History

Revision 0.1

September, 2025

Initial release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!



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