AN951: Driving Long Traces on PCIe Backplanes for Simple Evaluation

It is becoming common in server and storage applications to require more than twenty 100 MHz PCIe Gen 2/3 clock outputs for various system functions and ICs. Along with this high fan-out count, designing clock traces longer than ten inches and hybrid models driving high speed cables over HSMC connectors in addition to long traces are becoming increasingly common. In these design cases, designers are always concerned about jitter margin and performance, receiver signal integrity requirements that the driver needs to satisfy, and the impact of aggressor signals on PCIe jitter performance.

This application note analyzes different real world PCIe circuit designs and how different trace lengths, trace impedance, and aggressors will impact signal integrity and jitter performance. The analysis is done using evaluation boards designed to closely replicate the different scenarios of the circuit design mentioned above.

KEY EVB FEATURES

- Two types of traces:
  - Traces on the top layer of a 6-layer PCB.
  - Traces in the middle layer (layer 3) of a 6-layer PCB.
- 100 Ω differential impedance trace (Z_0 = 50 Ω).
- 85 Ω differential impedance trace (Z_0 = 42.5 Ω).
- An aggressor signal along with the PCIe clock signal.
- HSMC connectors for high speed cables instead of driving the traces on the board.

1. Overview

Figure 1.1 Example of the Evaluation Boards Used on page 1 is an example of the evaluation boards. Each board has labels describing the trace type, total trace length, and the differential trace impedance.

Figure 1.2 Measurement Setup on page 1 shows the block diagram for the measurement setup.

Figure 1.1. Example of the Evaluation Boards Used

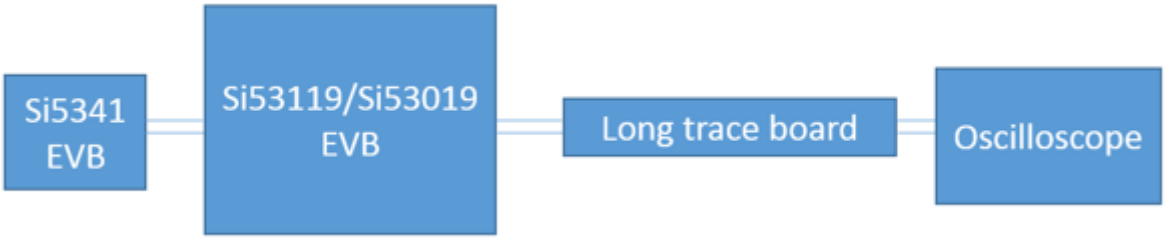

Figure 1.2. Measurement Setup

It should be noted that the analysis in this application note is based on the data taken with the Si53119 PCIe buffer device with Si5341 as the clock source. However, similar performance can be expected using any PCIe clock generator/buffer IC noted in the table below.

Table 1.1. Silicon Labs PCIe Server Buffer Family

Part Number	Outputs	Output Buffer Type
Si53106	6	Push-Pull
Si53108	8	Push-Pull
Si53112	12	Push-Pull
Si53115	15	Push-Pull
Si53119	19	Push-Pull
Si53019	19	Constant Current

Two common analyses are:

1. Push-pull versus current mode HCSL output buffer designs, as covered in AN871: "Driving Long PCIe Clock Lines" (100 Ω differential impedance).
2. Impact of trace length for 85 Ω impedance traces, as covered in this application note (push-pull buffer design).

2. Impact of Trace Length for 85 Ω Impedance Traces (Push-pull Buffer Design)

Figure 2.1 Aggressor Signals vs. HCSL Signals on the Long Trace Board on page 2 shows the input HCSL clock signal (Clk+, Clk–) coupled with the aggressor signal (Agg+, Agg–). The aggressor used is a 105 MHz differential noise at 3.3 V CMOS levels. Differential noise negates the noise immunity offered by differential signaling to noise, i.e., common mode noise. Both HCSL clock signal and aggressor signals are inputs to the long trace evaluation board. Figure 2.2 Slew Rate vs. Trace Length on page 2 through Figure 2.6 PCIe Gen 3 Jitter (RMS) vs. Trace Length on page 4 show the impact of trace length and trace type on the HSCL clock signal driven by a push-pull buffer.

Figure 2.1. Aggressor Signals vs. HCSL Signals on the Long Trace Board

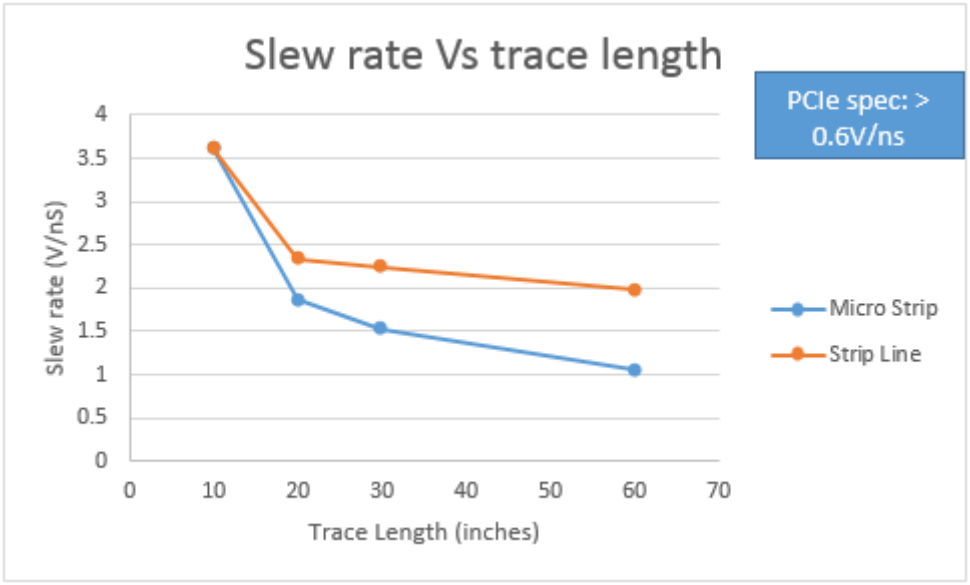

Figure 2.2. Slew Rate vs. Trace Length

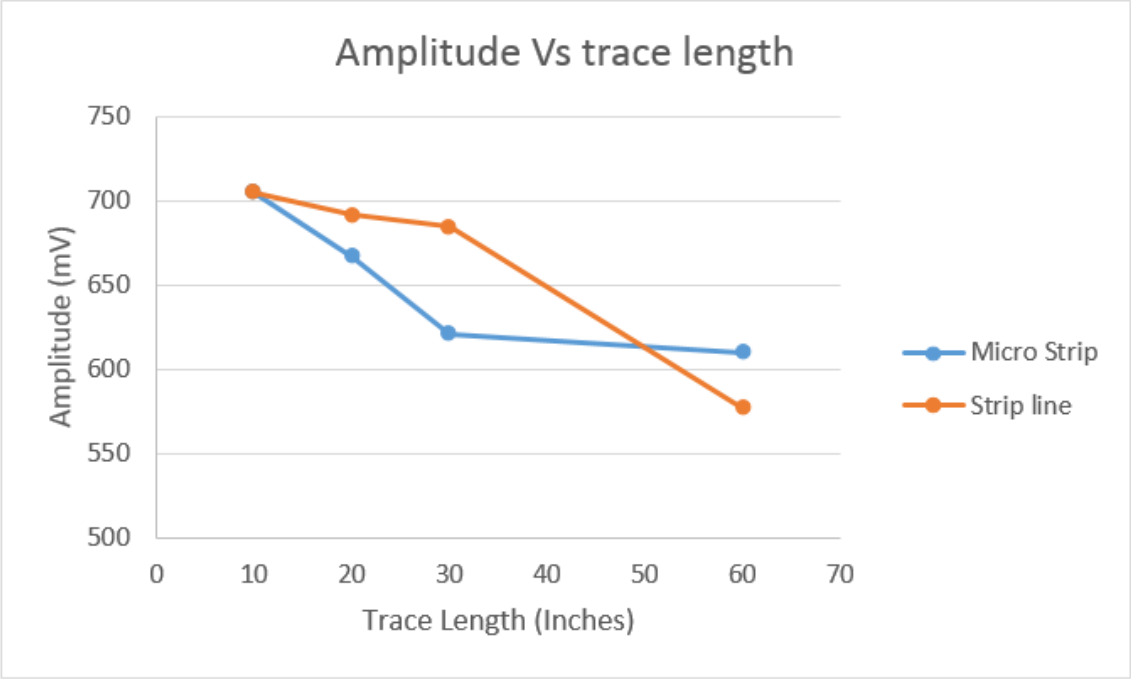

Figure 2.3. Signal Amplitude vs. Trace Length

The signal amplitude and slew rate degrade at slower gradient on Strip Line traces as compared to Micro Strip traces. Refer to Figure 2.2 Slew Rate vs. Trace Length on page 2 and Figure 2.3 Signal Amplitude vs. Trace Length on page 3 for an illustration of this.

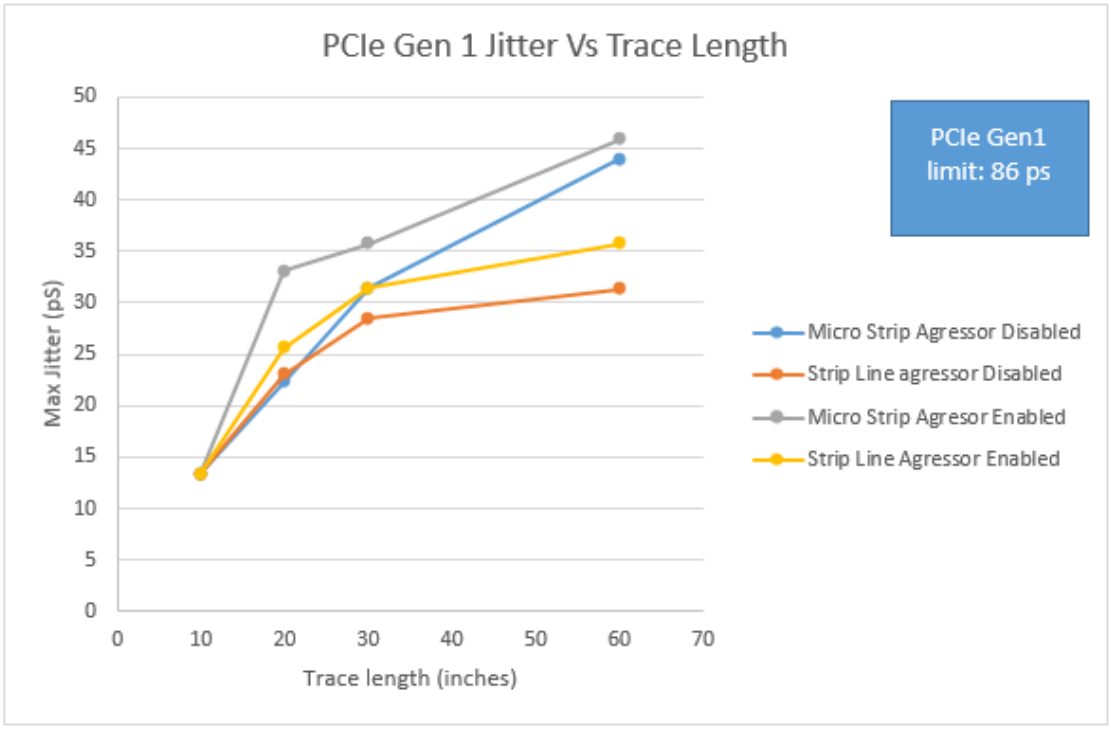

Figure 2.4. PCIe Gen 1 Peak-Peak Jitter vs. Trace Length

PCIe Gen 1 jitter degrades with trace length but is still within specifications. Strip Line traces perform better with trace length.

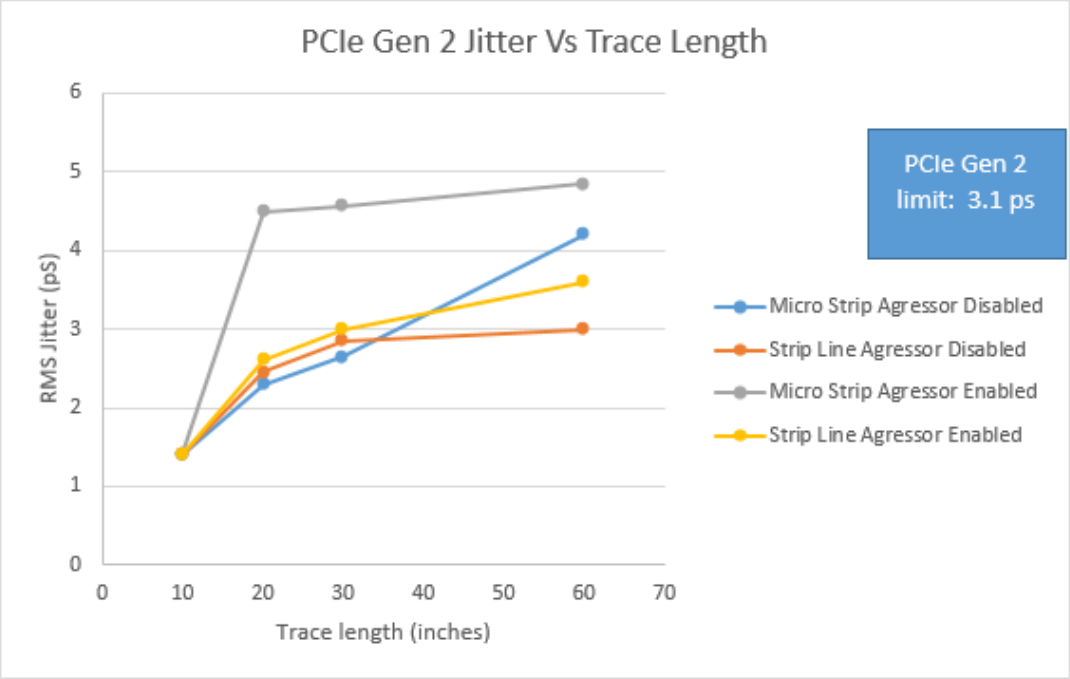

Figure 2.5. PCIe Gen 2 Jitter (RMS) vs. Trace Length

PCIe Gen 2 jitter degrades with trace length and can violate specifications. Strip Line traces perform better with trace length. For PCIe Gen 2 jitter compliance, care must be taken to minimize interference in order to enable driving long traces.

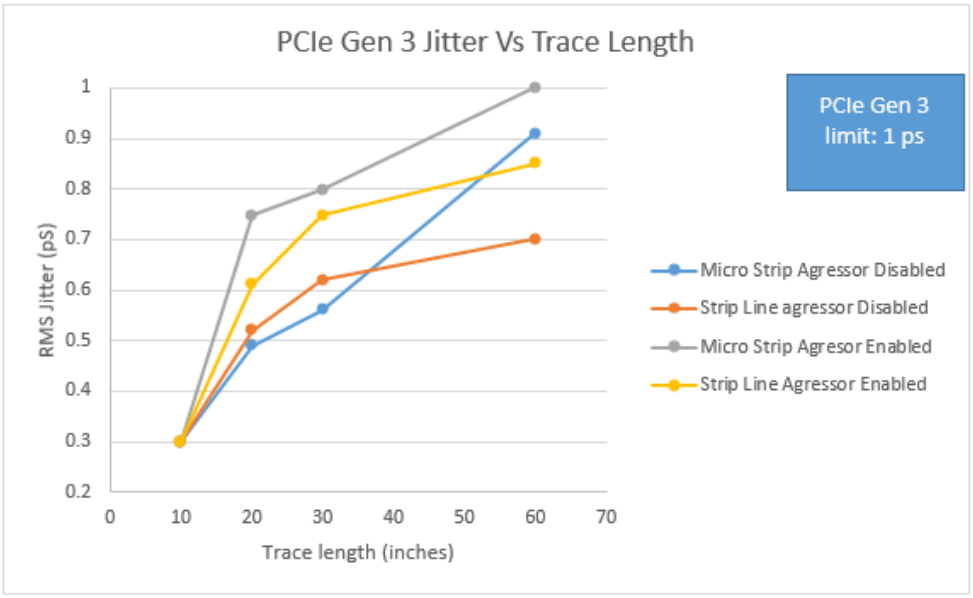

Figure 2.6. PCIe Gen 3 Jitter (RMS) vs. Trace Length

Figure 2.2 Slew Rate vs. Trace Length on page 2 through Figure 2.6 PCIe Gen 3 Jitter (RMS) vs. Trace Length on page 4 show that the Strip Line traces provide better PCIe performance, noise immunity and signal integrity over Micro Strip traces. The noise immunity of Strip Line traces are highlighted in the jitter transfer plots shown for PCIe Gen 1 phase jitter plots (See the figures below).

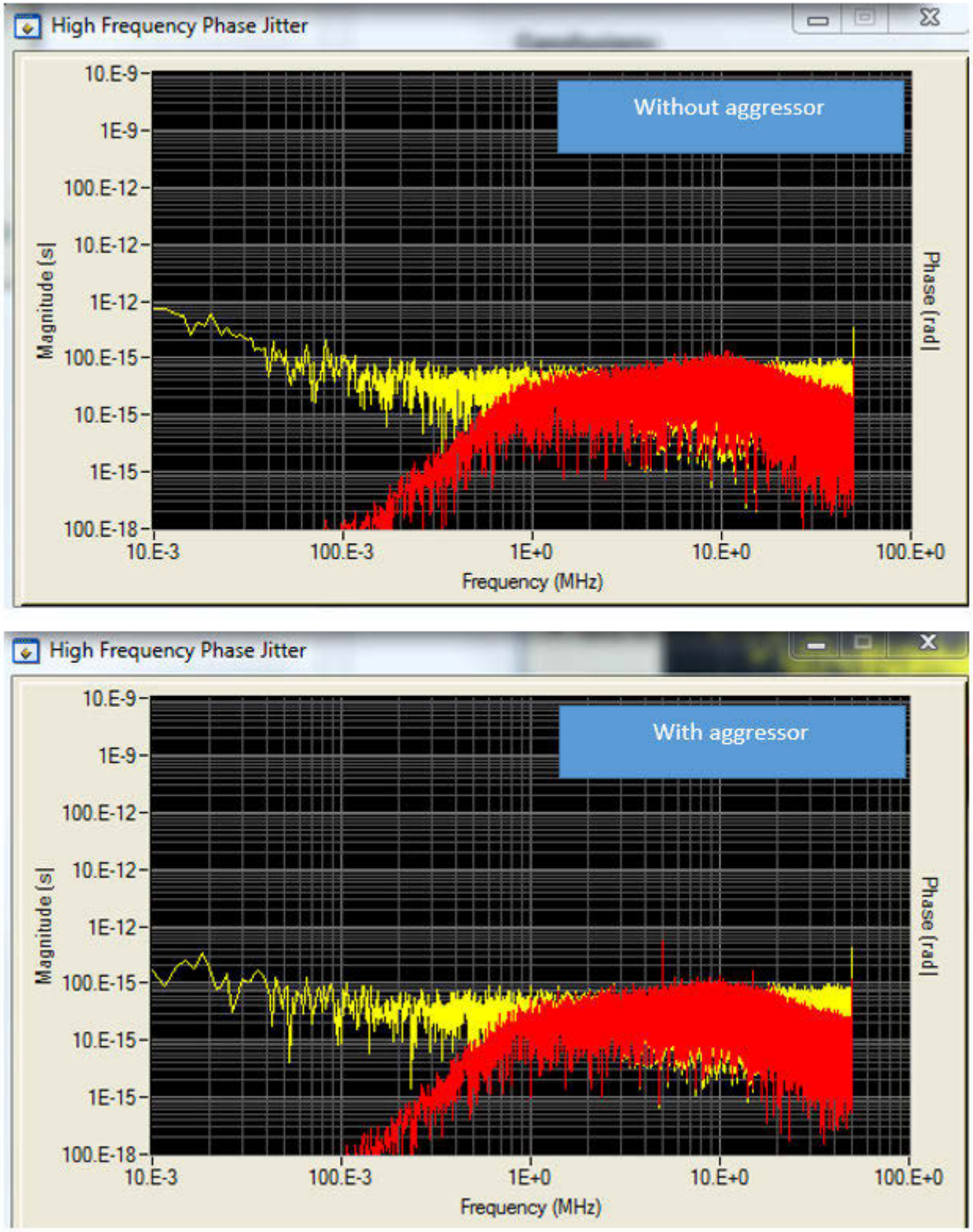

Figure 2.7. PCIe Gen 1 Jitter Transfer With and Without Aggressor Signal: Strip Line Trace

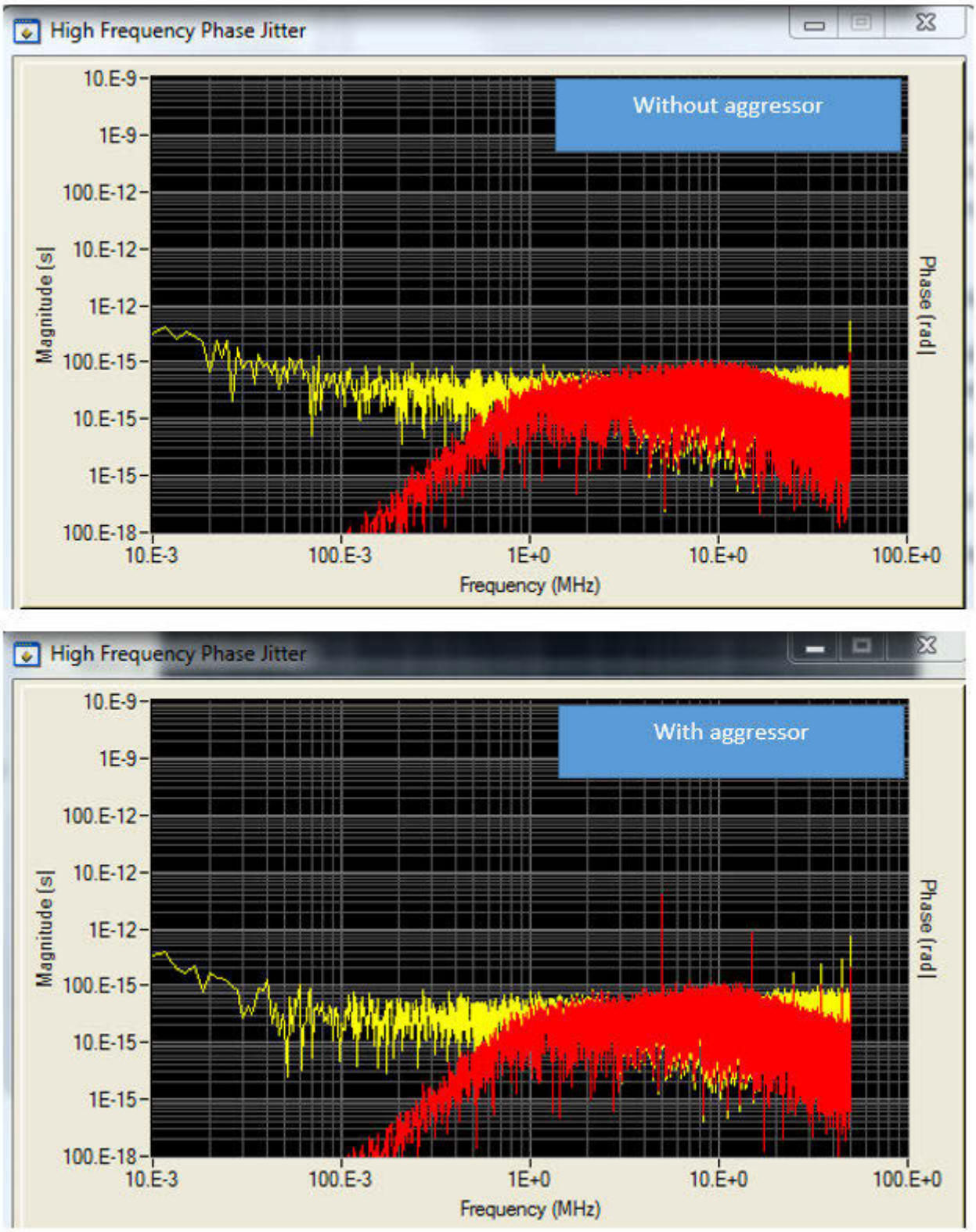

Figure 2.8. PCIe Gen 1 Jitter Transfer With and Without Aggressor Signal: Micro Strip Trace

3. Conclusion

From the observations discussed, the key insights from the study are:

1. The signal amplitude and slew rate degrade at slower gradient on Strip Line traces as compared to Micro Strip traces.
2. This smaller gradient also helps reduce the gradient for PCIe jitter degradation, i.e., PCIe jitter performance on strip lines traces are better than on micro strip traces.
3. The strip line traces offer better immunity to differential noise, which in turn improves jitter performance, again pointing to better jitter performance on strip line traces as compared to micro strip traces.

Hence, it is preferable to use strip line traces when driving long traces on backplanes.

The long trace EVB can be used to make a similar analysis by emulating system design conditions to evaluate effect of long traces on PCIe performance.

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com