AN962: Implementing Master-Slave Timing Redundancy in Wireless and Packet-Based Network Applications

Robust synchronization distribution schemes have historically been essential to communication networks and are more important than ever in today's evolving networks. Synchronization is needed between communication networks to efficiently transfer data. Mobile networks rely on both frequency and phase synchronization to support high-speed data transmission and manage call hand-offs as subscribers move from one cell area to another, and data centers require synchronization to maintain accurate time of day for distributed computing and high-frequency trading. It is, therefore, important that these systems be designed with redundant synchronization architectures to prevent single points of failure.

A widely-used synchronization distribution architecture uses two centralized timing cards with multiple line cards communicating over a common backplane. This architecture provides a redundant master slave timing system in which timing cards are used to deliver the system clock to the line cards. The two timing cards provide redundancy, ensuring uninterrupted synchronization and system robustness. The slave acts as the backup to the master in case of a failure. In this type of architecture, one timing card is designated as the master and the other the slave. The master selects the input reference clock, and the slave, which is the backup timing card, closely tracks the master system clock and provides redundant system clocks aligned to it by both frequency and phase. In case of a master timing card failure, the slave quickly becomes the master without interruption to the line cards.

Robust redundant network synchronizers are important for system-level protection against failure conditions. This application note focuses on the details of implementing a master-slave timing redundancy system using Silicon Lab's products.

KEY POINTS

- Phase transient from master/slave switch <1 ns.
- Master acquires slave settings and slave acquires master settings while in holdover
- Master PLL bandwidth is set to 0.1 Hz while slave PLL bandwidth is set to 100 Hz to allow the slave to quickly track the master
- A microprocessor controls some of the setting changes of timing cards and line cards based on certain event triggers
- There are two reasons to do a switch: a failure condition or a routine test

1. Overview

In a master and slave system, one timing card is designated as the master and the other the slave. The master will select the input reference clock. The slave, which is the backup timing card, will closely track the master system clock and provide redundant system clocks that are both frequency and phase aligned to the master. In the case of a failure on the master timing card, the slave quickly switches to be the master without interruption to the line cards. Silicon Labs offers products like the Si5348 network synchronizer for these timing card applications. The device is Stratum 3 / 3E compliant and can be used in Synchronous Ethernet / IEEE1588 packet-based applications. For line card applications, Silicon Labs offers products like the Si5345 to provide synchronization, jitter cleaning, clock multiplication and high-speed SerDes clocking.

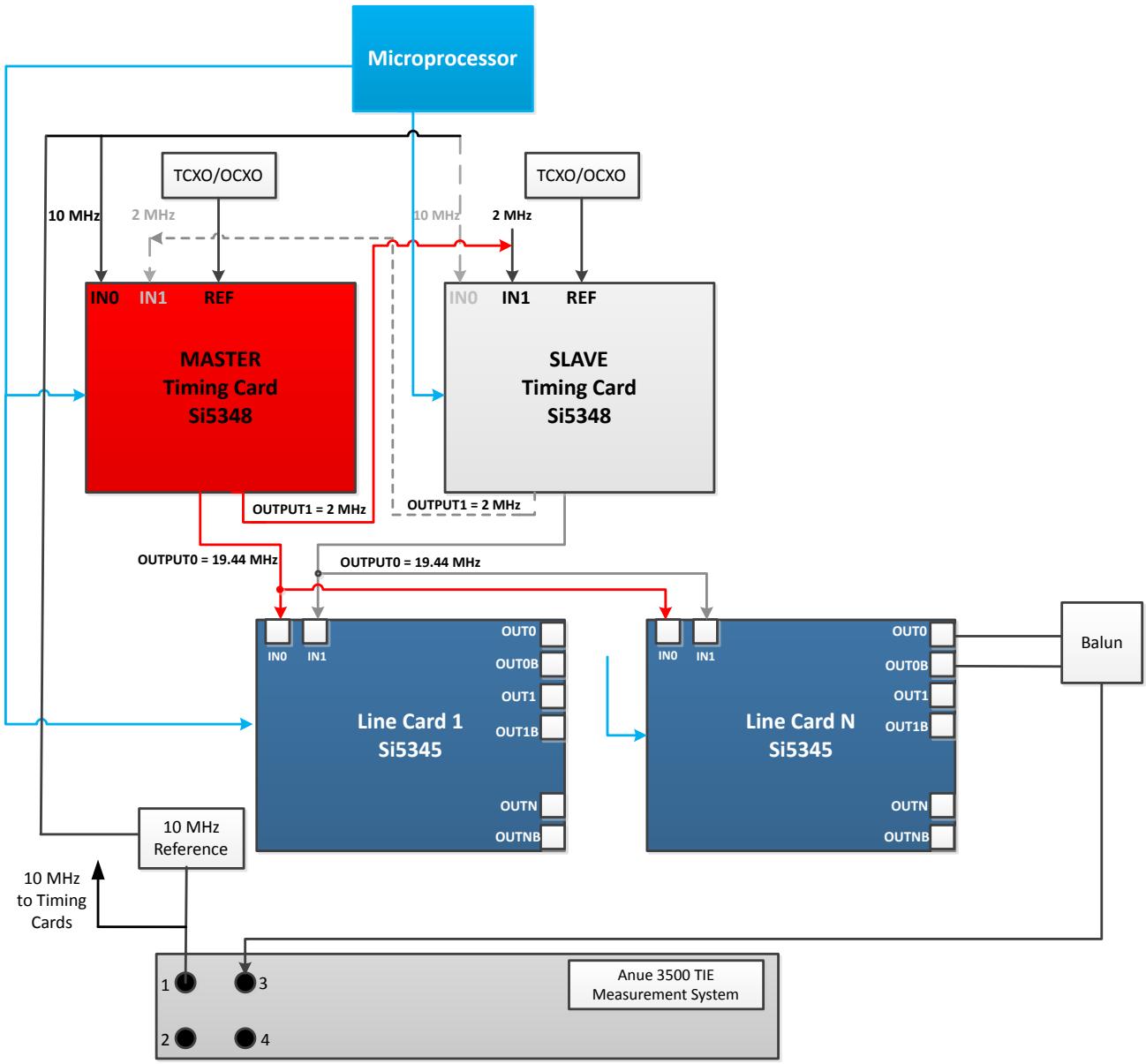

Figure 1.1. Master-Slave Timing Card Redundancy System Block Diagram

2. System Configuration

The following system configuration is a specific example that has been set up and tested in a lab environment. The bandwidth settings may vary depending on the circumstances and are not mandatory. At system power up, one of the timing cards is configured as the master (shown in red in Figure 1.1 Master-Slave Timing Card Redundancy System Block Diagram on page 1) and the other as the slave (shown in grey). For this application, the master network synchronizer has a PLL bandwidth of 0.1 Hz, while the slave has a PLL bandwidth of 100 Hz. The slave bandwidth is set much higher to allow quick response time for the slave to track the movements of the master.

The master is configured to have a specific priority of different input clocks with hitless switching enabled. The slave is connected to the same input clocks as the master but is configured to track the master. This is shown as IN1 on the slave timing card above. The other input connections are there for symmetry, enabling the slave to switch over to master mode.

The line cards are configured to prioritize the input from the master (shown in IN0 on the line card inFigure 1.1 Master-Slave Timing Card Redundancy System Block Diagram on page 1). If a failure is detected on the master or a routine switch is initiated, the line cards automatically switch over to IN1. Hitless switching is enabled on the line cards, and the PLL bandwidth is set to 100 Hz.

3. Sequencing Details of a Master to Slave Switch Process

A switch can be forced or initiated due to a failure condition on the master.

The following table shows the sequence of events that occurs during a forced master/slave switch process.

Table 3.1. Master/Slave Forced Switch Sequence

Event	Host Processor	Original Master	Original Slave	Line Card
1		Locked to external references, BW=0.1Hz	Locked to Master, BW=100Hz	Locked to Master
2	Force Slave in Holdover		Enter Holdover	
3	Switch line card input from master to slave			Locked to Slave
4	Configure Slave as Master		BW=0.1Hz, Lock to external references	Locked to Slave in Holdover
5	Force Slave exit from Holdover		Lock acquisition to 0.1Hz bandwidth New Master	Lock acquisition to New Master
6	Configure Master as Slave	BW=100Hz		
7	Change input priority to New Master			
8		**New Slave, Locked to New Master**	**Locked New Master**	**Locked to New Master**

The master starts off locked to the external reference with a bandwidth set to 0.1 Hz, while the slave is locked to the master with a bandwidth set to 100 Hz. The line card is locked to the master. The host processor then forces the slave into holdover during a routine master to slave switch. Then, the processor switches the input on the line card from the master over to the slave, which is in holdover. The line card locks to the slave. The slave is immediately configured to the original master settings. Then, the slave is forced to exit from holdover and is now considered the new master. The new master goes through a lock acquisition to external references using the 0.1 Hz bandwidth settings, and the line card is then locked to the new master. The old master is reconfigured as the slave with a 100 Hz bandwidth and is locked to the new master.

The following table shows the sequence of events during a master failure. In this case an LOS (loss of signal) fault is detected on the slave, which causes it to go into holdover. Step 3 is eliminated due to master clock failure, causing the line card to automatically switch over to the slave in holdover. Otherwise, the sequence of events are the same as a routine switch.

Table 3.2. Master/Slave Switch Sequence Initiated from Master Failure

Event	Host Processor	Master	Slave	Line Card
1		Locked to external references, BW=0.1Hz	Locked to Master, BW=100Hz	Locked to Master
2	LOS Detected on Slave		Automatically Enter Holdover	Automatically Switch to Slave
4	Configure Slave as Master		BW=0.1Hz, Lock to external references	Locked to Slave in Holdover
5	Force Slave exit from Holdover		Lock acquisition to 0.1Hz bandwidth New Master	Lock acquisition to New Master
6	Configure Master as Slave	BW=100Hz		
7	Change input priority to New Master			
8		**New Slave, Locked to New Master**	**Locked New Master**	**Locked to New Master**

4. Phase Measurements during Master/Slave Switch

The figure below shows an output transient recorded from the Anue 3500 measurement system. A 25 MHz output signal is monitored on Input 3 of the Anue system. This signal comes from the output of the line card. The Anue box uses the same GPS for the reference on Input 1 as is used for the input of the line cards. The TIE measurement is recorded during the entire switch process. Some delays were added in the software sequence to be able to identify the different steps so that they would show up in the graph, but the switch-over process Steps 1 through 6 (from the tables above) can happen within a few milliseconds. The results show that the phase transient is as low as 1 ns during a master/slave switch sequence. The exit from holdover from steps 7 to 8 can be even smaller with more advanced features that have been developed in the Si5348 network synchronizer and Si5345 line card clock IC.

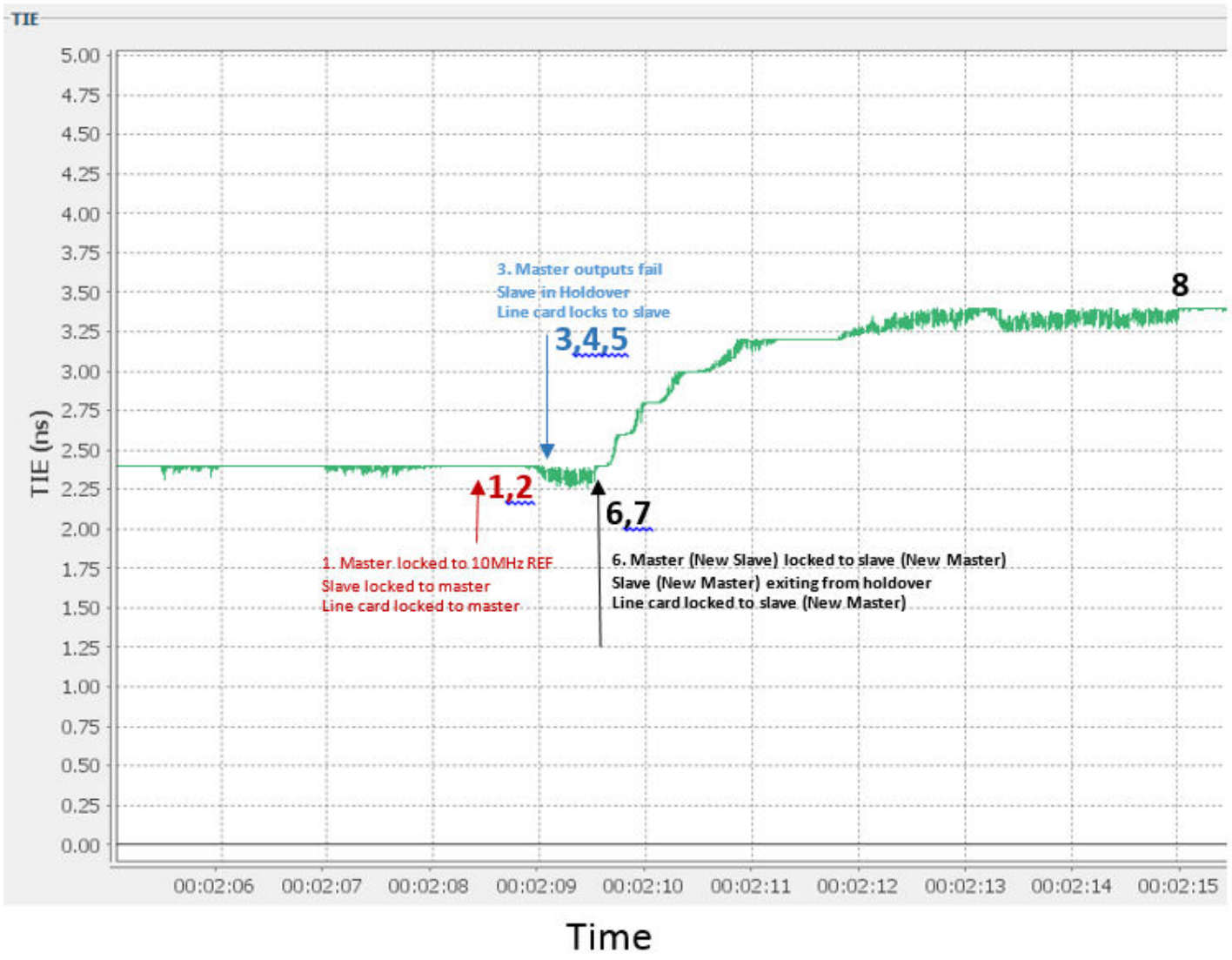

Figure 4.1. Phase Transient from Line Card during Master/Slave Switchover Process

5. Conclusions

Redundant network synchronizers are used in a master/slave configuration to provide system-level protection in the case of a failure condition. The switching process from master timing card to the slave timing card can happen seamlessly with less than 1 ns of phase transient when high-performance network synchronizers and line card PLLs are used.

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com