AN0002.0: EFM32 and EZR32 Wireless MCU Series 0 Hardware Design Considerations

This application note details hardware design considerations for EFM32 and EZR32 Wireless MCU Series 0 devices. For hardware design considerations for EFM32 and EFR32 Wireless Gecko Series 1 devices, refer to *AN0002.1: EFM32 and EFR32 Wireless MCU Series 1 Hardware Design Considerations*

Topics specifically covered are supported power supply configurations, supply filtering considerations, debug interface connections, and external clock sources.

In addition, reference designs for the EFM32 Series 0 microcontrollers are included.

KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- The debug interface consists of two communication pins (SWCLK and SWDIO).
- External clock sources must be connected to the device correctly for proper operation.
- This application note includes:
  - This PDF document
  - Reference Design (zip)
    - OrCAD schematic design files
    - PDF Schematics
    - Symbol libraries (OrCAD, CSV, and Edif formats)

1. Device Compatibility

This application note supports multiple device families, and some functionality is different depending on the device.

EFM32 Series 0 consists of:

- EFM32 Gecko (EFM32G)
- EFM32 Giant Gecko (EFM32GG)
- EFM32 Wonder Gecko (EFM32WG)
- EFM32 Leopard Gecko (EFM32LG)
- EFM32 Tiny Gecko (EFM32TG)
- EFM32 Zero Gecko (EFM32ZG)
- EFM32 Happy Gecko (EFM32HG)

EZR32 Wireless MCU Series 0 consists of:

- EZR32 Wonder Gecko (EZR32WG)
- EZR32 Leopard Gecko (EZR32LG)
- EZR32 Happy Gecko (EZR32HG)

2. Power Supply Overview

2.1 Introduction

Although the EFM32 and EZR32 Wireless MCU Series 0 devices have an exceptionally small average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses corresponding to the clock edges. Particularly when several I/O lines are switching simultaneously, transient current pulses on the power supply can be in the order of several hundred mA for a few nanoseconds, even though the average current consumption is quite small.

These kinds of transient currents cannot be properly delivered over high impedance power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, decoupling capacitors are employed to supplement the current during these short transients.

2.2 Decoupling Capacitors

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin, ground pin, and PCB (Printed Circuit Board) ground plane.

All external decoupling capacitors should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 to +85 °C (standard temperature range devices) or -55 to +125 °C (extended temperature range devices).

For regulator output capacitors (e.g., DECOUPLE and DCDC), the system designer should pay particular attention to the characteristics of the capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages or using cheaper dielectrics) can experience a dramatic reduction in capacitance value across temperature or as the DC bias voltage increases. Any change pushing the regulator output capacitance outside the datasheet specified limits may result in output instability on that supply.

2.3 Power Supply Requirements

An important consideration for all devices is the voltage requirements and dependencies between the power supply pins. The system designer needs to ensure that these power supply requirements are met, regardless of power configuration or topology. Please see the device data sheet for absolute maximum rating and additional details regarding relative system voltage constraints.

EFM32 Series 0 Power Supply Requirements

- VDD_DREG = AVDD = IOVDD

EZR32 Wireless MCU Series 0 Power Supply Requirements

- VDD_DREG = AVDD = IOVDD = RFVDD

Power Supply Pin Overview

Note that not all supply pins exist on all devices. The table below describes the supply pins and where it appears.

Table 2.1. Power Supply Pin Overview

Pin Name	Product Family	Description
VDD_DREG	All devices	Input to the internal Digital LDO
AVDD	All devices	Supply to analog peripherals
DECOUPLE	All devices	Output of the internal Digital LDO & Digital logic power supply
IOVDD	All devices	GPIO supply voltage
USB_VREGI	All USB-enabled devices	Input to the internal 3.3 V LDO. Typically connected to the USB 5V supply.
USB_VREGO	All USB-enabled devices	Output of the internal 3.3 V LDO.
RFVDD	EZR32 Wireless MCU Series 0 only	Supply to radio analog. Note, RFVDD also supplies the radio power amplifier.

2.4 DECOUPLE

All EFM32 and EZR32 Wireless MCU Series 0 devices include an internal linear regulator that powers the core and digital logic. The DECOUPLE pin is the the output of the Digital LDO, and requires a 1 uF capacitor.

The VDD_DREG pin is the input to the LDO and the DECOUPLE pin is the output of the LDO.

For regulator output capacitors (e.g., DECOUPLE), the system designer should pay particular attention to the characteristics of the capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages) can experience a dramatic reduction in capacitance value as across temperature or as the bias voltage increases. Any change pushing the regulator output capacitance outside the datasheet specified limits may result in output instability on that supply.

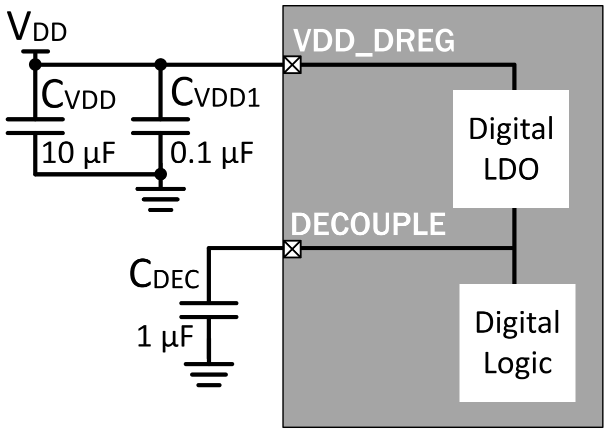


Figure 2.1. VDD_DREG and DECOUPLE

2.5 IOVDD

The IOVDD pin(s) provide decoupling for all of the GPIO pins on the device. A 0.1 uF capacitor per IOVDD pin is recommend, along with a 10 uF bulk capacitor. The bulk capacitor value may safely be reduced if there are other large bulk capacitors on the same supply (e.g., if IOVDD=AVDD=Main Supply, and there are multiple 10uF capacitors already).

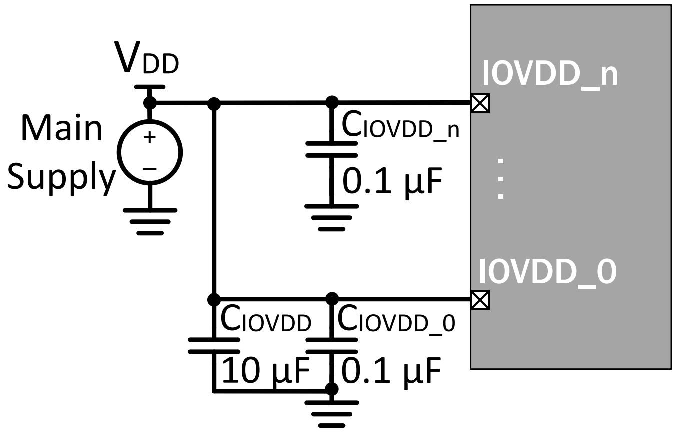


Figure 2.2. IOVDD Decoupling

2.6 AVDD

The analog peripheral performance of the device is impacted by the quality of the AVDD power supply. For applications with less demanding analog performance, a simpler decoupling scheme for AVDD may be acceptable. For applications requiring the highest quality analog performance, more robust decoupling and filtering is required.

Note that the number of AVDD analog power pins may vary by device and package.

2.6.1 AVDD Standard Decoupling

The figure below illustrates a standard approach for decoupling the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}).

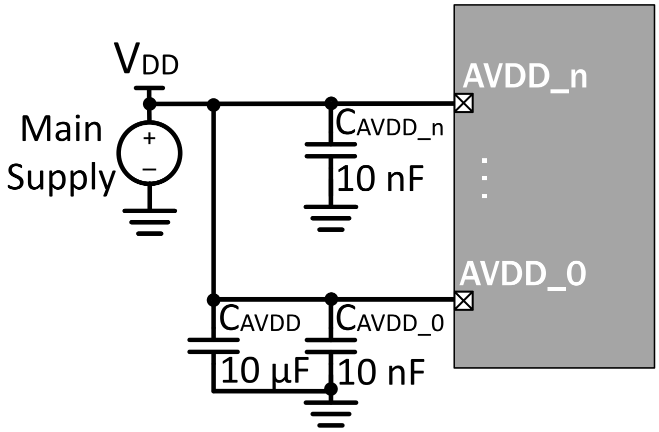


Figure 2.3. AVDD Standard Decoupling

2.6.2 AVDD Improved Decoupling

The figure below illustrates an improved approach for decoupling and filtering the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}). In addition, a ferrite bead and series 1 Ω resistor provide additional power supply filtering and isolation.

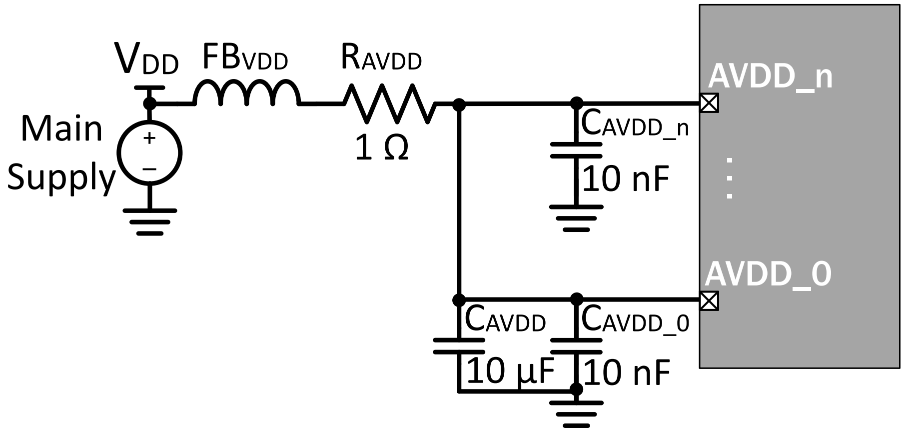


Figure 2.4. AVDD Improved Decoupling

The table below lists some recommended ferrite bead part numbers suitable for AVDD filtering.

Table 2.2. Recommended Ferrite Beads

Manufacturer	Part Number	Impedance	I_{MAX} (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Würth Electronics	74279266	1 kΩ @ 100 MHz	200	0.600	-55 to +125	0603/1608
Murata	BLM21BD102SN1D	1 kΩ @ 100 MHz	200	0.400	-55 to +125	0805/2012

2.7 USB (USB_VREGI & USB_VREGO)

Some EFM32 and EZR32 Wireless MCU Series 0 devices integrate a USB controller and a 3.3V LDO. The figure below illustrates a standard approach for connecting and decoupling the USB_VREGI, and USB_VREGO pins. In addition, the USB5V sense line (USB_VBUS) is shown connected directly to V_{USB}.

To avoid violating the USB specification, the total capacitance on V_{USB} should not exceed 10 µF. Consult *AN0046: USB Hardware Design Guide* for detailed hardware guidance for USB applications.

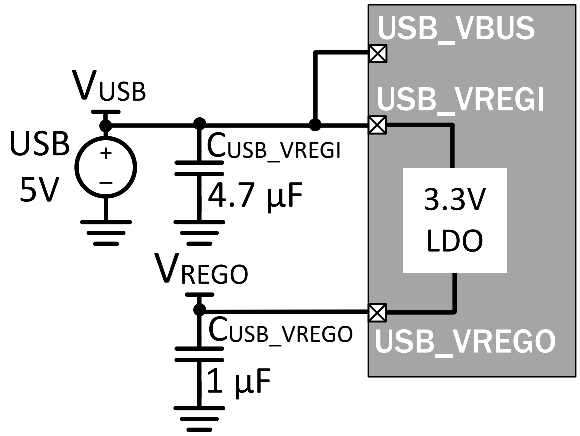


Figure 2.5. USB_VREGI and USB_VREGO Decoupling

3. Example Power Supply Configurations

3.1 EFM32 Series 0 —Standard Decoupling Example

The figure below illustrates a standard approach for decoupling. This configuration is simple and uses minimal components, while providing sufficient noise suppression for many typical applications.

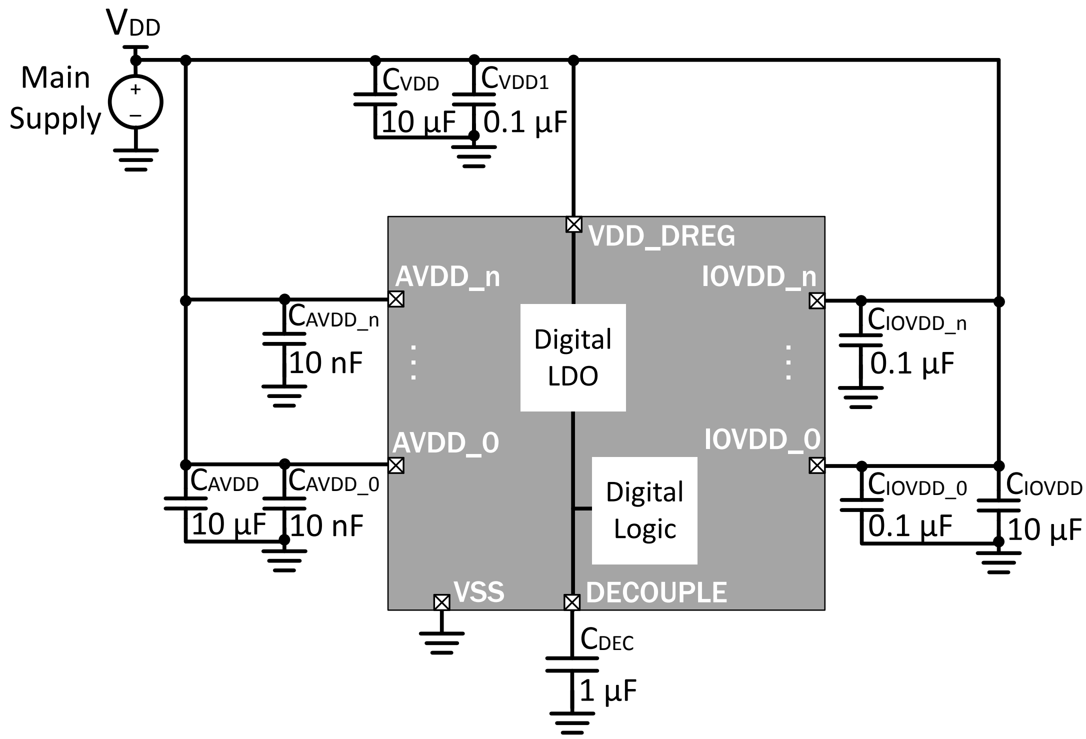


Figure 3.1. EFM32 Series 0 Standard Decoupling Example

3.2 EFM32 Series 0 —Improved AVDD Filtering Example

In the following figure, a decoupling approach providing better noise suppression and isolation between the digital and analog power pins using a ferrite bead and a resistor is illustrated. This configuration is preferred when higher ADC accuracy is required. Refer to Table 2.2 Recommended Ferrite Beads on page 6 for recommended ferrite bead part numbers.

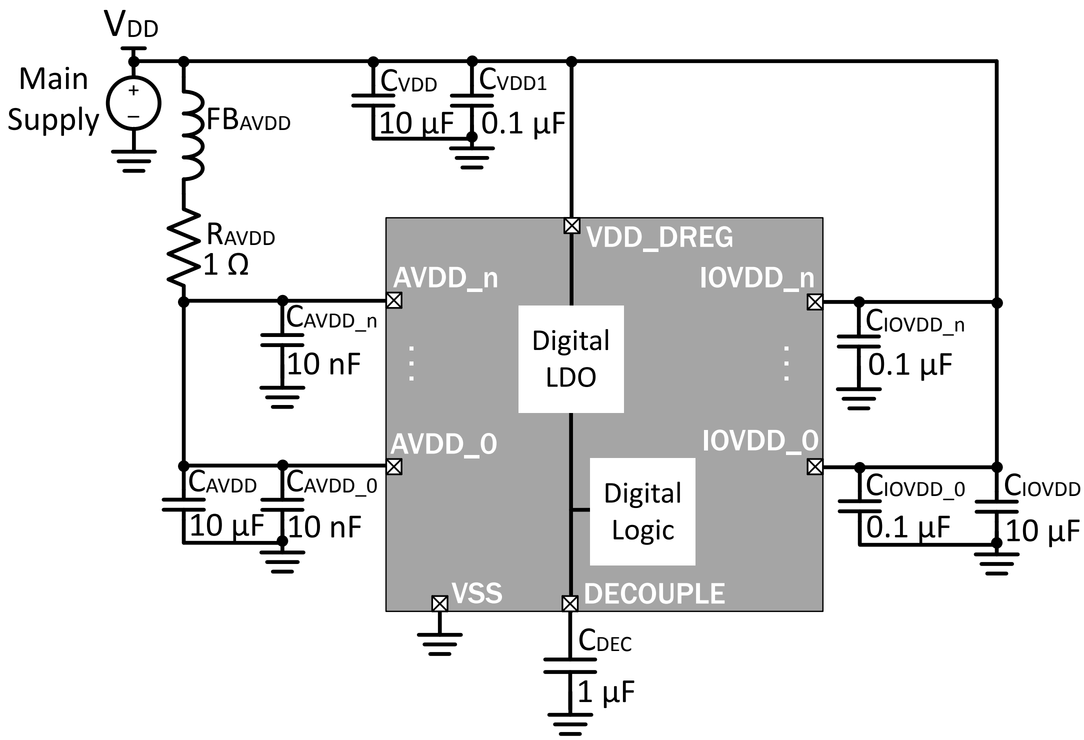


Figure 3.2. EFM32 Series 0 Improved AVDD Filtering Example

Note: Note that during power-on for EFM32GG and EFM32G Series 0 devices, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the filter in Figure 3.2 EFM32 Series 0 Improved AVDD Filtering Example on page 9 can cause a significant delay on the AVDD_x pins. For improved AVDD filtering for EFM32GG and EFM32G Series 0 devices, refer to section 3.3 EFM32GG and EFM32G Series 0 Only—Improved AVDD Filtering Example

3.3 EFM32GG and EFM32G Series 0 Only—Improved AVDD Filtering Example

Similar to section 3.2 EFM32 Series 0 —Improved AVDD Filtering Example, the figure below shows improved noise suppression and isolation between the digital and analog power pins for high ADC accuracy. Refer to Table 2.2 Recommended Ferrite Beads on page 6 for recommended ferrite bead part numbers.

There is a unique restriction on EFM32GG and EFM32G Series 0 devices that at power on, the AVDD_x pins must not be powered up after the IOVDD_x and VDD_DREG pins. If the rise time of the power supply is short, the AVDD filter can cause a significant delay on the AVDD_x pins. Therefore, for EFM32GG and EFM32G Series 0 devices, an additional 1 Ω resistor should also be added to the VDD_DREG supply path, as shown in the figure below.

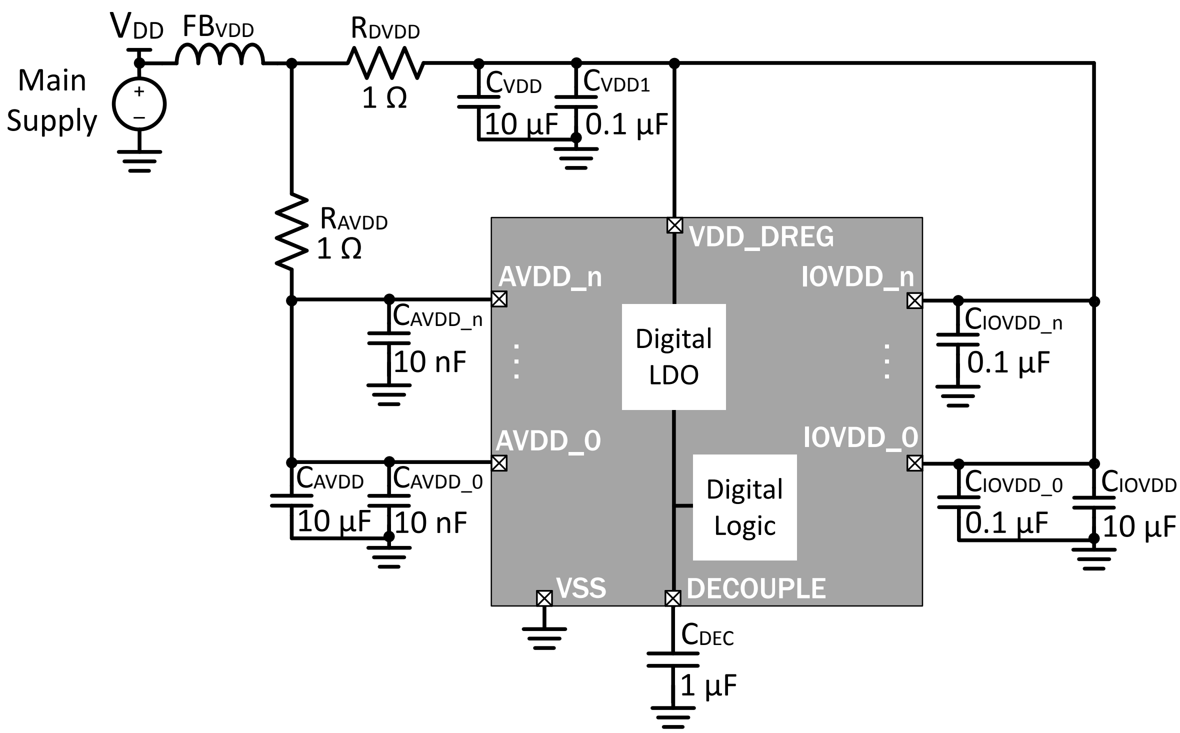


Figure 3.3. EFM32GG and EFM32G Series 0 Improved AVDD Filtering Example

3.4 EZR32 Wireless MCU Series 0 —Standard Decoupling Example

The figure below illustrates a standard approach for decoupling a EZR32 Wireless MCU Series 0 device.

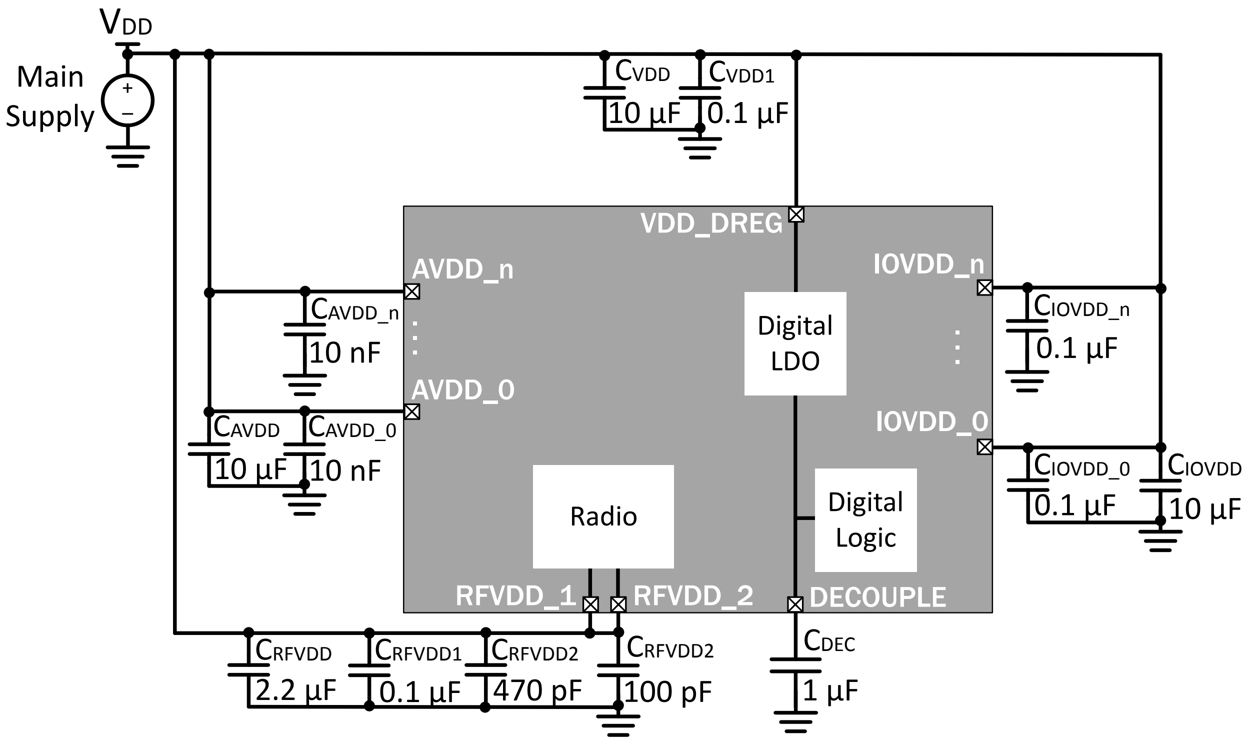


Figure 3.4. EZR32 Wireless MCU Series 0 Standard Decoupling Example

4. Debug Interface and External Reset Pin

4.1 Serial Wire Debug

The Serial Wire (SWD) interface is supported by all EFM32 and EZR32 Wireless MCU Series 0 devices. The SWD debug interface consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional SWO (serial wire output). The SWO line is used for instrumentation trace and program counter sampling, and is not needed for programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and it is therefore recommended to include this line in a design.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

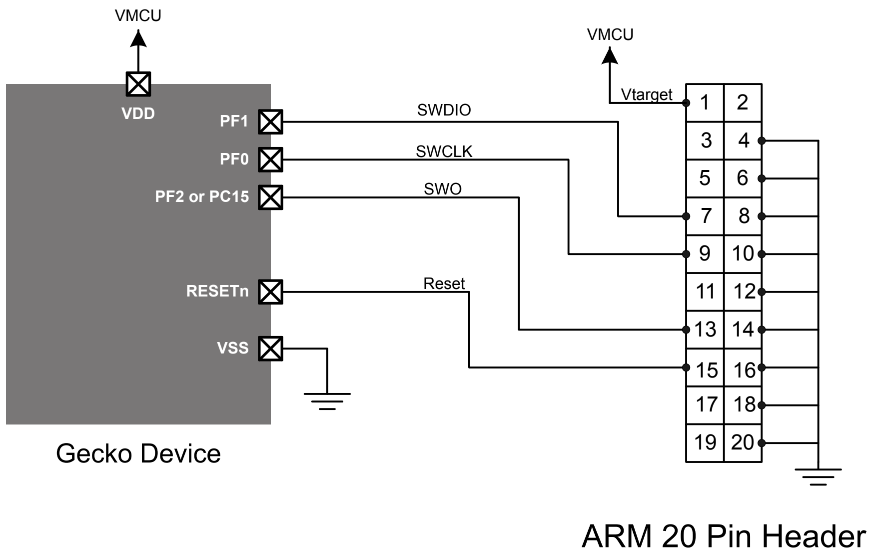


Figure 4.1. Connecting the Gecko Device to an ARM 20-pin Debug Header

Note: The V_{target} connection is not for supplying power. The debugger uses V_{target} as a reference voltage for the debugger's level translators.

4.2 External Reset Pin (RESETn)

Forcing the RESETn pin low generates a reset of the EFM32 and EZR32 Wireless MCU Series 0 device. The RESETn pin includes an internal pull-up resistor and can therefore be left unconnected if no external reset source is required. Also connected to the RESETn line is a low-pass filter which prevents noise glitches from causing unintended resets. The characteristics of the pullup and input filter is identical to the corresponding characteristic of a GPIO pin, which is found in the device data sheet.

Note: To apply an external reset source to this pin, drive this pin low during reset. The internal pull-up ensures that the reset is released. This pin should not be connected to an external pull-up or driven high while the device is unpowered, as this could damage the device. This is also important when using back-up power mode, as the internal pull-up automatically switches to the back-up power rail, which could end up back-powering the entire system through the external pull up.

5. External Clock Sources

5.1 Introduction

The EFM32 and EZR32 Wireless MCU Series 0 devices support different external clock sources to generate the low and high frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how the external clock sources should be connected.

For additional information on the external oscillators, refer to the application note *AN0016: Oscillator Design Considerations*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or in Simplicity Studio.

5.2 Low Frequency Clock Sources

The external low frequency clock can be generated from a crystal/ceramic resonator or from an external clock source.

5.2.1 Low Frequency Crystals and Ceramic Resonators

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 5.1 Low Frequency Crystal on page 13. The crystal is to be connected across the LFXTAL_N and LFXTAL_P pins of the EFM32 and EZR32 Wireless MCU Series 0 devices.

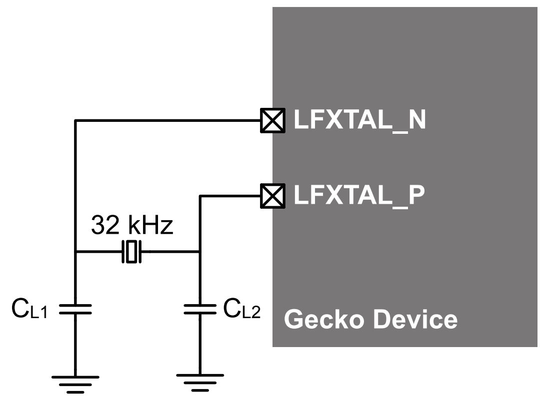


Figure 5.1. Low Frequency Crystal

The crystals/ceramic resonators oscillate mechanically and have an electrical equivalent circuit as shown in Figure 5.2 Equivalent Circuit of a Crystal/Ceramic Resonator on page 13. In the electrical circuit, C_S represents the motional capacitance, L_S the motional inductance, R_S the mechanical losses during oscillation, and C_0 the parasitic capacitance of the package and pins. C_{L1} and C_{L2} represent the load capacitance. This circuit is valid for both crystals and ceramic resonators.

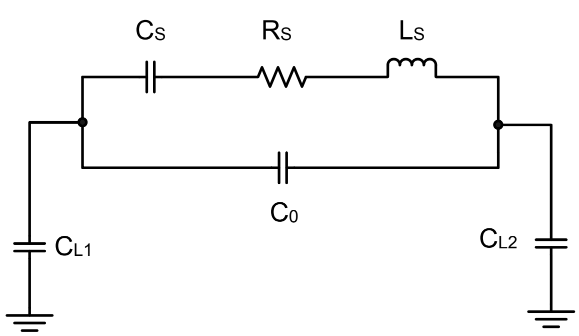


Figure 5.2. Equivalent Circuit of a Crystal/Ceramic Resonator

5.2.2 Low Frequency External Clocks

The EFM32 and EZR32 Wireless MCU Series 0 devices can also be clocked by an LF external clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can either be a square wave or sine signal with a frequency of 32.768 kHz. The external clock source must be connected as indicated in Figure 5.3 Low Frequency External Clock on page 14.

When a square wave source is used, the LFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%, as specified in the device data sheet. When a sine source is used, the amplitude must be in accordance with the device data sheet. The sine signal is buffered through the LFXO buffer, whose input is ac-coupled.

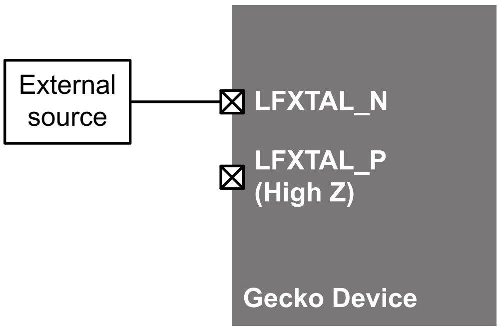


Figure 5.3. Low Frequency External Clock

5.3 High Frequency Clock Sources

The external high frequency clock can be generated from a crystal/ceramic resonator or from an external square or sine wave source.

5.3.1 High Frequency Crystals and Ceramic Resonators

The hardware configuration of the crystal and ceramic resonator is indicated in Figure 5.4 High Frequency Crystal Oscillator on page 14. The crystal should be connected across the HFXTAL_N and HFXTAL_P pins.

The electrical equivalent circuit of the HF crystal/ceramic resonators is equal to the one for LF crystals/ceramic resonators in the figure below.

Placement of C_L is important for proper operating frequency.

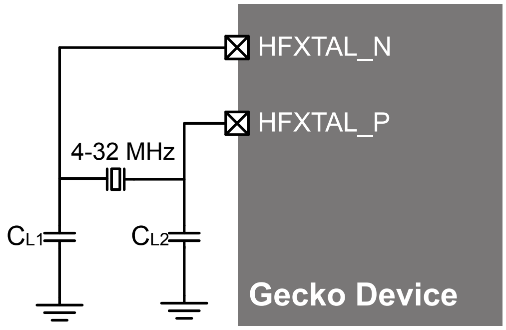


Figure 5.4. High Frequency Crystal Oscillator

5.3.2 High Frequency External Clocks

The EFM32 and EZR32 Wireless MCU Series 0 devices can also be clocked by an external HF clock source. To select a proper external oscillator, consider the specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle and signal levels. The external clock source must be connected as indicated in Figure 5.5 External High Frequency Clock on page 15.

The external clock signal should be either a square wave or a sine wave signal with a frequency in accordance with the device data sheet.

When an external square wave clock source is used, the HFXO buffer must be in bypass mode. The clock signal must toggle between 0 and V_{DD} and the duty cycle must be close to 50%. Refer to the device data sheet for further details.

When a sine source is used, the sine amplitude must be in accordance with what is specified in the device data sheet. The sine signal is buffered through the HFXO buffer, whose input is ac-coupled.

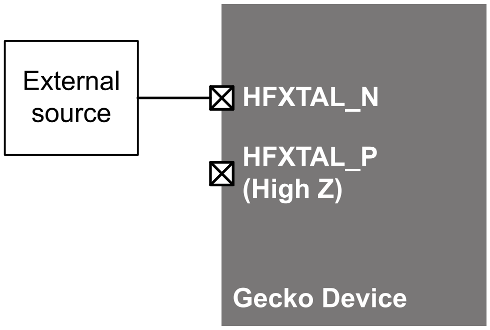


Figure 5.5. External High Frequency Clock

6. Reference Design

When starting a new design using EFM32 and EZR32 Wireless MCU Series 0 devices, some parts of the layout are almost always required regardless of the application. Attached to this application note are example schematics for power decoupling, reset, external clocks, and debug interface. Using this reference design as a template can improve development speed in the early stages of a new design. The reference design and included symbols are compatible with Cadence OrCAD 9.0 and later versions.

This application note does not include footprints for the devices, but these can be found in `*.bxl` format on http://www.silabs.com.

6.1 Contents

The application note folder includes several zip files with the following contents:

- CSV pin list files
- Edif symbols
- OrCAD OLB symbols
- OrCAD DSN example schematics
- PDF example schematics

The schematics and symbols are included for the following device families:

- EFM32ZG
- EFM32HG
- EFM32TG
- EFM32G
- EFM32LG
- EFM32WG
- EFM32GG

A generic symbol is included for the EZR32 Wireless MCU Series 0 family.

6.2 Comments on the Schematics

6.2.1 Power Supply Decoupling

The decouple pin uses a 1 µF capacitor to filter transients in the power domain for the internal voltage regulator.

Each power pin has a 10 nF decoupling capacitor in addition to the common 10 µF decoupling capacitor, as described in . The digital power supply is separated from the analog power supply to reduce EMI. To further improve the switching noise of the analog power, an EMI suppressor is put in series between V_{MCU} and the analog power pins.

The active low reset pin is connected to ground through a normally open switch, as well as to the debug interface connector.

6.2.2 Debug Interface

A standard ARM 20-pin debug connector is connected to the EFM32 and EZR32 Wireless MCU Series 0 device debug pins.

6.2.3 High/Low Frequency Clock

Both the high and low frequency clock pins are connected to crystal oscillators using two of the recommended crystals from the *AN0016: Oscillator Design Considerations* application note.

7. Revision History

7.1 Revision 1.48

2017-6-27

Moved the device compatibility information from the front page to 1. Device Compatibility.

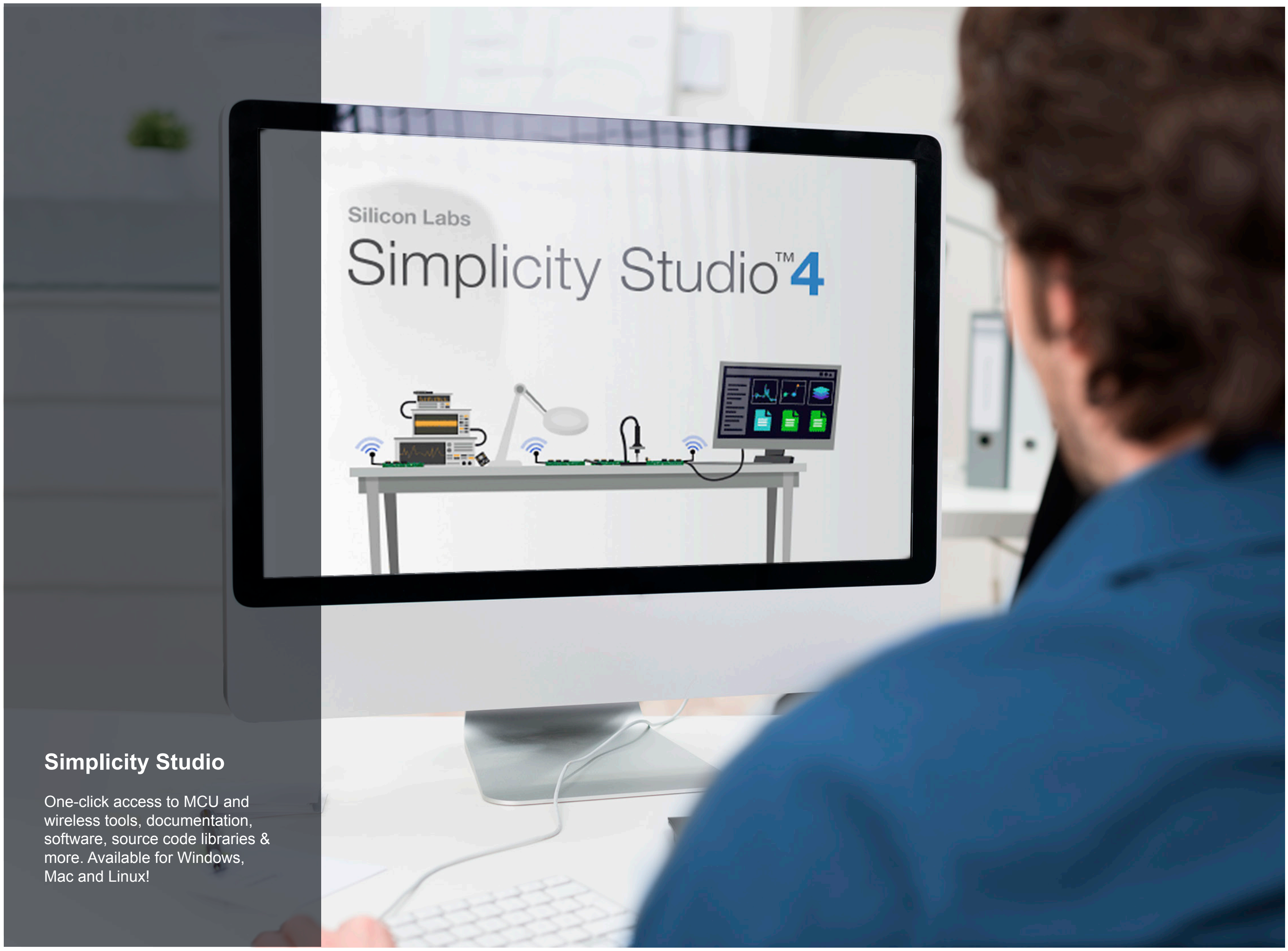
Made some small text changes to 2.2 Decoupling Capacitors.

7.2 Revision 1.47

2017-1-13

Split application note into multiple application notes based on series.

Added note advising the system designer to check the capacitance vs temperature characteristics for regulator output capacitors.



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