AN0002.2: EFR32 Wireless Gecko Series 2 Hardware Design Considerations

This application note details hardware design considerations for EFR32 Wireless Gecko Series 2 devices. For hardware design considerations for EFM32 and EZR32 Wireless MCU Series 0 and EFM32 and EFR32 Wireless Gecko Series 1 devices, refer to *AN0002.0: EFM32 and EZR32 Wireless MCU Series 0 Hardware Design Considerations* and *AN0002.1: EFM32 and EFR32 Wireless MCU Series 1 Hardware Design Considerations*, respectively.

Topics specifically covered are supported power supply configurations, supply filtering considerations, debug interface connections, and external clock sources.

For more information on hardware layout considerations for the radio portion of EFR32 Wireless Gecko Series 2 devices, see *AN930: EFR32 2.4 GHz Matching Guide* and *AN928: EFR32 Layout Design Guide*.

KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- The debug interface consists of two communication pins (SWCLK and SWDIO).
- External clock sources must be connected to the device correctly for proper operation.

1. Device Compatibility

This application note supports multiple device families, and some functionality may differ depending on the device.

EFR32 Wireless Gecko Series 2 consists of:

- EFR32 Blue Gecko (EFR32BG21)
- EFR32 Mighty Gecko (EFR32MG21)

2. Power Supply Overview

2.1 Introduction

Although the EFR32 Wireless Gecko Series 2 devices have very low average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses corresponding to the clock edges. Particularly when several I/O lines are switching simultaneously, transient current pulses on the power supply can be in the order of several hundred mA for a few nanoseconds, even though the average current consumption is quite small.

These kinds of transient currents cannot be properly delivered over high impedance power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, decoupling capacitors are employed to supplement the current during these short transients.

2.2 Decoupling Capacitors

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pins, ground pins, and PCB (Printed Circuit Board) ground planes.

All external decoupling capacitors should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 to +85 °C (standard temperature range devices) or -55 to +125 °C (extended temperature range devices).

For regulator output capacitors (e.g., DECOUPLE and DCDC, if available), the system designer should pay particular attention to the characteristics of the capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages or using cheaper dielectrics) can experience a dramatic reduction in capacitance value across temperature or as the DC bias voltage increases. Any change pushing the regulator output capacitance outside the data sheet specified limits may result in output instability on that supply.

2.3 Power Supply Requirements

An important consideration for all devices is the voltage requirements and dependencies between the power supply pins. The system designer needs to ensure that these power supply requirements are met, regardless of power configuration or topology. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Failure to observe the below constraints can result in damage to the device and/or increased current draw. Refer to the device data sheet for absolute maximum ratings and additional details regarding relative system voltage constraints.

EFR32 Wireless Gecko Series 2 Power Supply Requirements

- AVDD and IOVDD - No dependency with each other or any other supply pin
- DVDD >= DECOUPLE
- PAVDD >= RFVDD

Power Supply Pin Overview

Note that not all supply pins exist on all devices. The table below provides an overview of the available power supply pins.

Table 2.1. Power Supply Pin Overview

Pin Name	Product Family	Description
AVDD	All devices	Supply to analog peripherals
DECOUPLE	All devices	Output of the internal Digital LDO. Also, input for the Digital logic power supply
IOVDD	All devices	GPIO supply voltage
DVDD	All devices	Input to the internal Digital LDO
RFVDD	EFR32 Wireless Gecko Series 2 only	Supply to radio analog and HFXO.
PAVDD	EFR32 Wireless Gecko Series 2 only	Supply to 2.4 GHz radio power amplifier

2.4 DVDD and DECOUPLE

All EFR32 Wireless Gecko Series 2 devices include an internal linear regulator that powers the core and digital logic. The DECOUPLE pin is the the output of the Digital LDO, and requires a 1 μF capacitor.

As mentioned in section 2.2 Decoupling Capacitors, care should be taken in the selection of decoupling capacitors for regualtor output, such as DECOUPLE, to ensure that changes in system temperature and bias voltage do not cause capacitance changes that fall outside of the data sheet specified limits, which could destabilize the regulator output.

EFR32 Wireless Gecko Series 2 DECOUPLE Pin

On EFR32 Wireless Gecko Series 2 devices, the input supply to the Digital LDO is the DVDD pin and the DECOUPLE pin the output of the LDO. Proper decoupling of DVDD should include a 2.2 μF capacitor in parallel with a 0.1 μF capacitor.

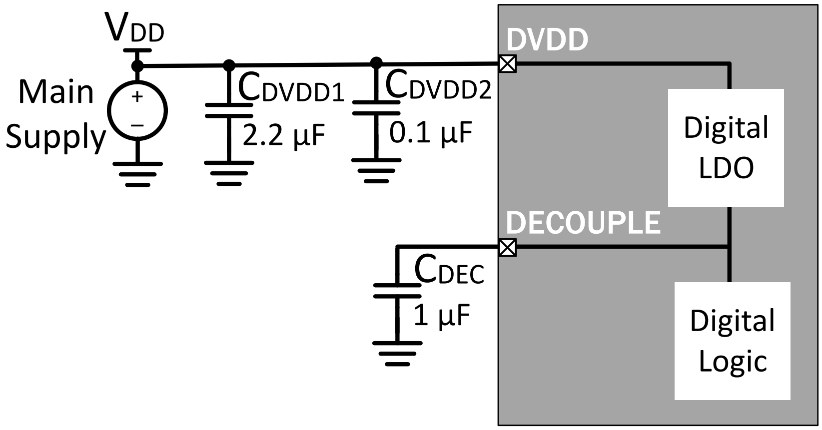


Figure 2.1. DVDD and DECOUPLE on EFR32 Wireless Gecko Series 2 Devices

Note: The DECOUPLE pin should not be used to power any external circuitry. Although DECOUPLE is connected to the output of the internal digital logic LDO, it is provided solely for the purposes of decoupling this supply and is not intended to power anything other than the internal digital logic of the device.

2.5 IOVDD

The IOVDD pin(s) provide decoupling for all of the GPIO pins on the device. A 0.1 μF capacitor per IOVDD pin is recommended, along with a 10 μF bulk capacitor. The bulk capacitor value may safely be reduced if there are other large bulk capacitors on the same supply (e.g., if IOVDD=AVDD=Main Supply, and there are multiple 10 μF capacitors already).

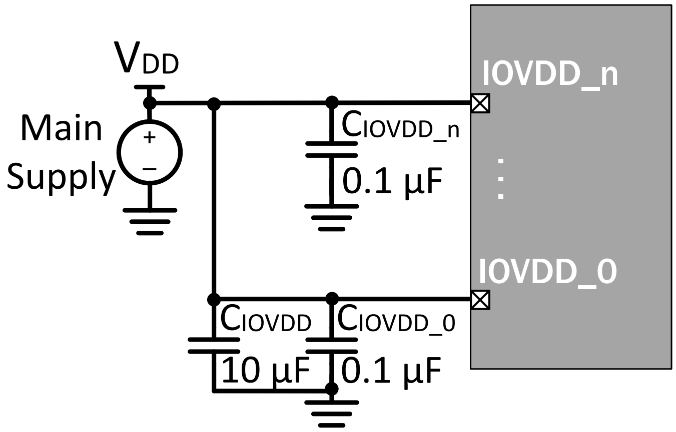


Figure 2.2. IOVDD Decoupling

2.6 AVDD

The analog peripheral performance of the device is impacted by the quality of the AVDD power supply. For applications with less demanding analog performance, a simpler decoupling scheme for AVDD may be acceptable. For applications requiring the highest quality analog performance, more robust decoupling and filtering is required.

Note that the number of AVDD analog power pins may vary by device and package.

2.6.1 AVDD Standard Decoupling

The figure below illustrates a standard approach for decoupling the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}).

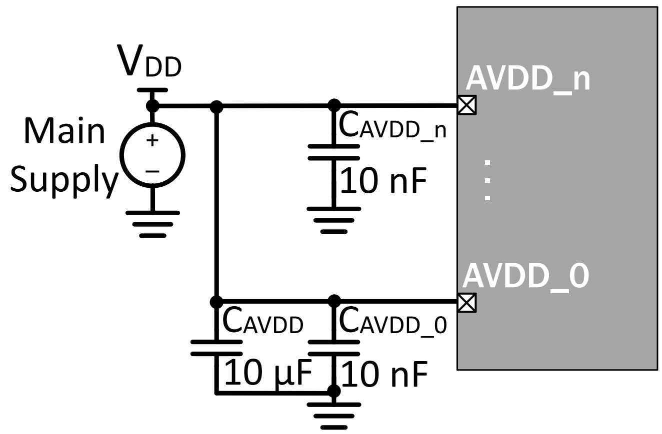


Figure 2.3. AVDD Standard Decoupling

2.6.2 AVDD Improved Decoupling

The figure below illustrates an improved approach for decoupling and filtering the AVDD pin(s). In general, the application should include one bulk capacitor (C_{AVDD}) of 10 µF, as well as one 10 nF capacitor per each AVDD pin (C_{AVDD_0} through C_{AVDD_n}). In addition, a ferrite bead and series 1 Ω resistor provide additional power supply filtering and isolation.

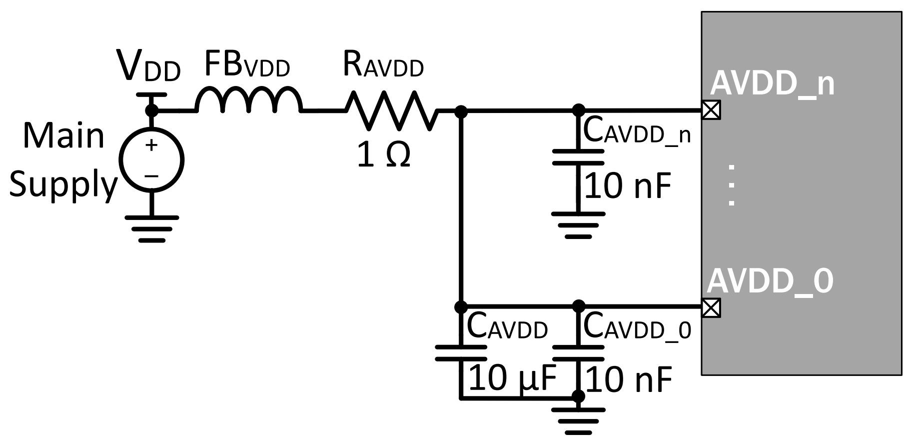


Figure 2.4. AVDD Improved Decoupling

The table below lists some recommended ferrite bead part numbers suitable for AVDD filtering.

Table 2.2. Recommended Ferrite Beads

Manufacturer	Part Number	Impedance	I_{MAX} (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Würth Electronics	74279266	1 kΩ @ 100 MHz	200	0.600	-55 to +125	0603/1608
Murata	BLM21BD102SN1D	1 kΩ @ 100 MHz	200	0.400	-55 to +125	0805/2012

2.7 Radio (RFVDD & PAVDD) — EFR32 Wireless Gecko Series 2

On EFR32 Wireless Gecko Series 2 devices, the radio power supplies (PAVDD and RFVDD) will typically be powered from the main supply, which requires few filtering components and supports > 13 dBm transmit power.

2.7.1 RFVDD and PAVDD — Powered from Main Supply

PAVDD and RFVDD should be powered directly from the main supply.

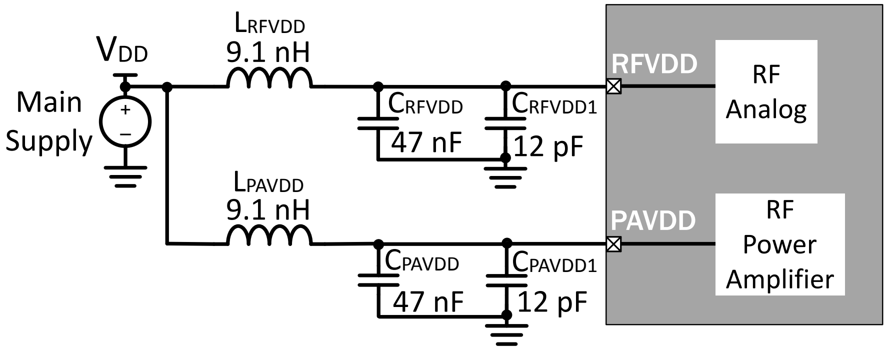


Figure 2.5. RFVDD and PAVDD Decoupling (2.4 GHz application, both supplies powered from main supply)

Table 2.3. RFVDD & PAVDD Decoupling Values, Powered from Main Supply

Application	L_{RFVDD}	C_{RFVDD}	C_{RFVDD1}	L_{PAVDD}	C_{PAVDD}	C_{PAVDD1}
2.4 GHz	9.1 nH	47 nF	12 pF	9.1 nH	47 nF	12 pF

3. Example Power Supply Configurations

3.1 EFR32 Wireless Gecko Series 2 — Standard Decoupling Example

The figure below illustrates a standard approach for decoupling a EFR32 Wireless Gecko Series 2 device.

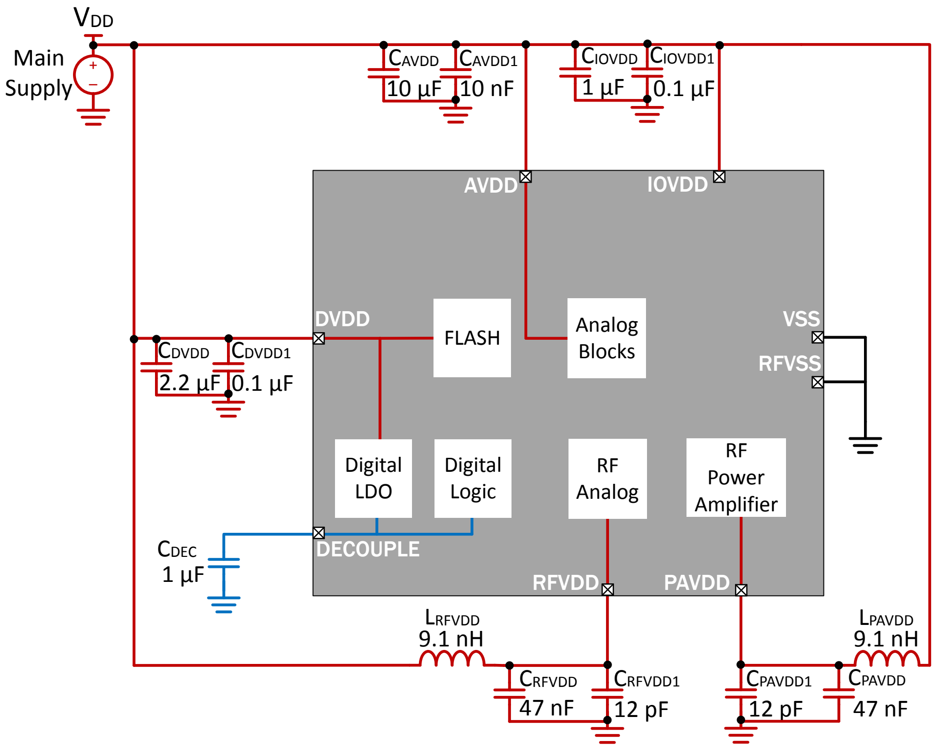


Figure 3.1. EFR32 Wireless Gecko Series 2 Standard Decoupling Example

3.2 EFR32 Wireless Gecko Series 2 — Improved AVDD Filtering Example

In the following figure, a decoupling approach providing better noise suppression and isolation between the digital and analog power pins using a ferrite bead and a resistor is illustrated. This configuration is preferred when higher ADC accuracy is required. Refer to Table 2.2 Recommended Ferrite Beads on page 6 for recommended ferrite bead part numbers.

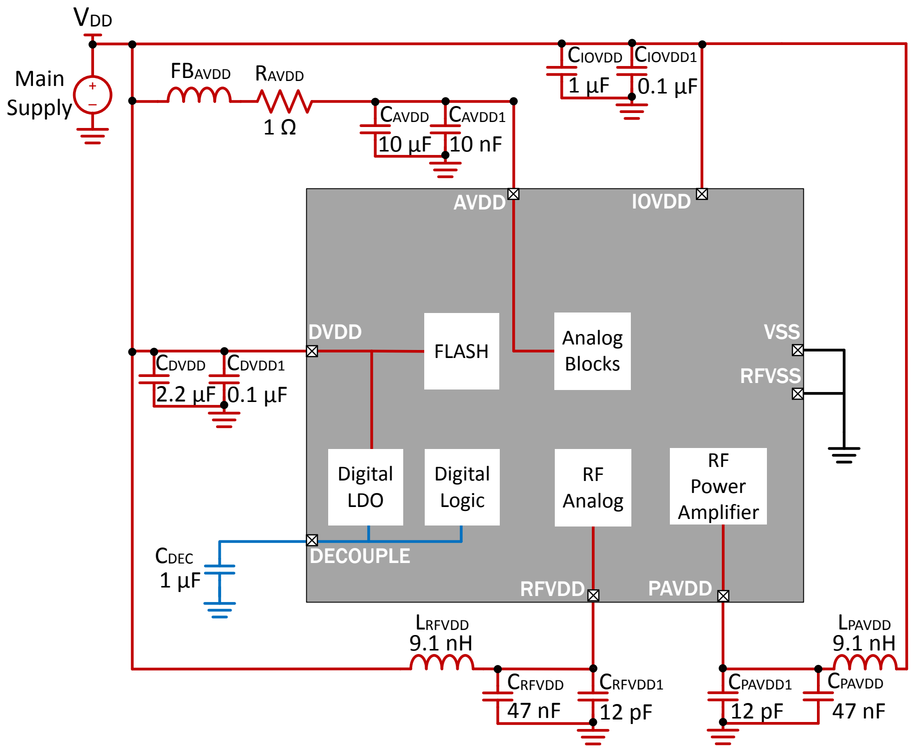


Figure 3.2. EFR32 Wireless Gecko Series 2 Improved AVDD Filtering Example

Note: Note that during power-on for EFR32 Wireless Gecko Series 2 devices, the AVDD_x pins must not be powered up after the IOVDD_x and DVDD pins. If the rise time of the power supply is short, the filter in the figure above can cause a significant delay on the AVDD_x pins.

4. Debug Interface and External Reset Pin

4.1 Serial Wire Debug

The Serial Wire Debug (SWD) interface is supported by all EFR32 Wireless Gecko Series 2 devices and consists of the SWCLK (clock input) and SWDIO (data in/out) lines, in addition to the optional serial wire output/serial wire viewer (SWO/SWV) signal. The SWO/SWV line is used for instrumentation trace and program counter sampling, and is not needed for flash programming and normal debugging. Nevertheless, it can be valuable in advanced debugging scenarios, and designers are strongly encouraged to include this along with the other SWD signals.

Connections to the standard ARM 20-pin debug header are shown in the following figure. Pins that are not connected to the microcontroller, power supply, or ground should be left unconnected.

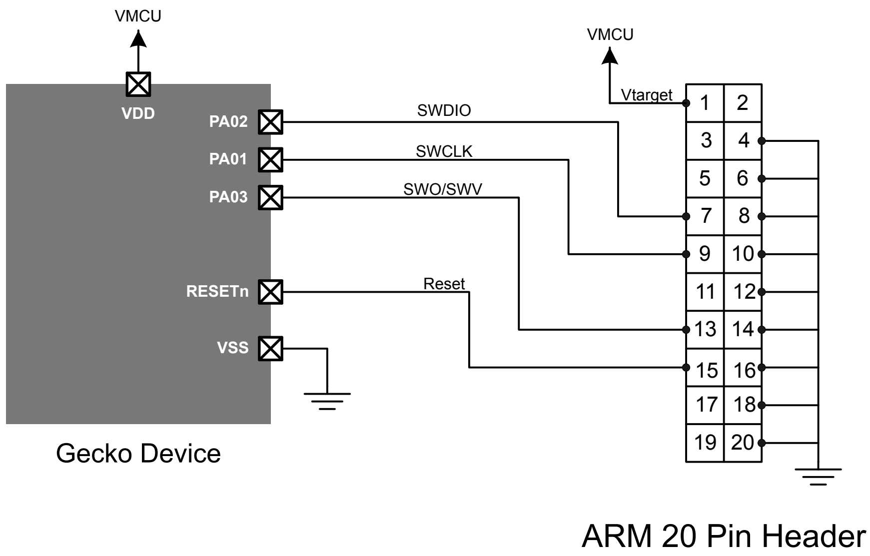


Figure 4.1. Connecting the Gecko Device to an ARM 20-pin Debug Header

Note:

1. The V_{target} connection does not supply power. The debugger uses V_{target} as a reference voltage for its level translators.

4.2 JTAG Debug

EFR32 Wireless Gecko Series 2 devices optionally support JTAG debug using the TCLK (clock), TDI (data input), TDO (data output), and TMS (input mode select) lines. TCLK is the JTAG interface clock. TDI carries input data, and is sampled on the rising edge of TCLK. TDO carries output data and is shifted out on the falling edge of TCLK. Finally, TMS is the input mode select signal, and is used to navigate through the Test Access Port (TAP) state machine.

Note: The JTAG implementation on EFR32 Wireless Gecko Series 2 devices does not support boundary scan testing. It can operate in pass-through mode and participate in a chain with other devices that do implement JTAG for firmware programming or boundary scan purposes.

The connection to an ARM 20-pin debug connector is shown in the following figure. Pins with no connection should be left unconnected.

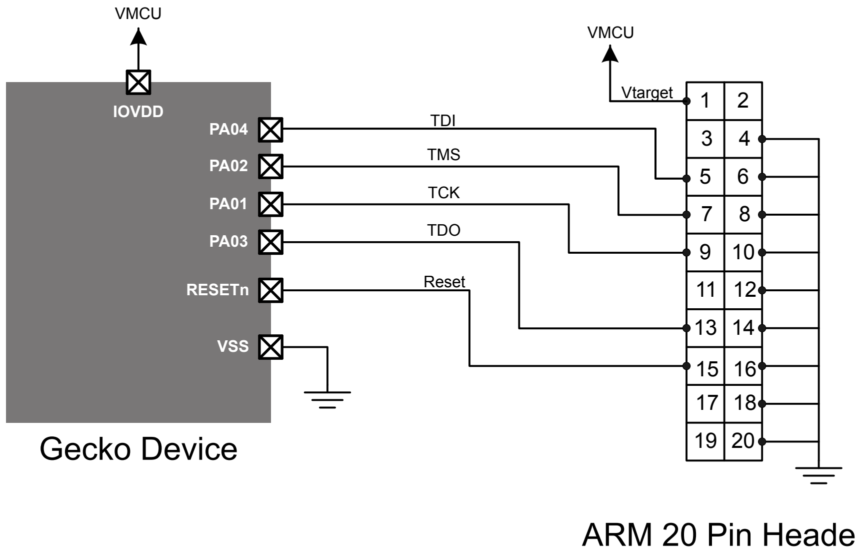


Figure 4.2. Connecting the EFR32 Wireless Gecko Series 2 Device to an ARM 20-pin Debug Header

Note: The V_{target} connection does not supply power. The debugger uses V_{target} as a reference voltage for its level translators.

4.3 External Reset Pin (RESETn)

EFR32 Wireless Gecko Series 2 processors can be reset by driving the RESETn pin low. A weak internal pull-up device holds the RESETn pin high, allowing it to be left unconnected if no external reset source is required. Also connected to RESETn is a low-pass filter to prevent noise glitches from causing unintended resets. The characteristics of the pull-up device and input filter are specified in the device data sheet.

Note: The internal pull-up ensures that the reset is released. When the device is not powered, RESETn must not be connected through an external pull-up to an active supply or otherwise driven high as this could damage the device.

Note: The RESETn pin is pulled up internally to DVDD. In the case where RESETn is connected to an external signal capable of driving the pin at a voltage different from V_{DVDD}, this internal pull up represents a possible current path, which could cause unwanted power consumption. Examples include connection of RESETn to an external supply/reset monitor, debugger, or coprocessor/multi-chip design. It is recommended that if RESETn is connected to an external device, it be connected only to open drain signals in order to avoid unwanted current consumption when RESETn is not being driven low.

5. External Clock Sources

5.1 Introduction

EFR32 Wireless Gecko Series 2 devices support different external clock sources to generate the high and low frequency clocks in addition to the internal LF and HF RC oscillators. The possible external clock sources for both the LF and HF domains are external oscillators (square or sine wave) or crystals/ceramic resonators. This section describes how external clock sources should be connected.

For additional information on the external oscillators, refer to the application note, AN0016.2: Oscillator Design Considerations. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or in Simplicity Studio.

5.2 Low Frequency Clock Sources

An external low frequency clock can be supplied from a crystal/ceramic resonator or from an external clock source.

5.2.1 Low Frequency Crystals and Ceramic Resonators

A crystal or ceramic resonator is connected as shown in the figure below across the LFXTAL_I and LFXTAL_O pins on EFR32 Wireless Gecko Series 2 devices. This circuit is valid for both crystals and ceramic resonators.

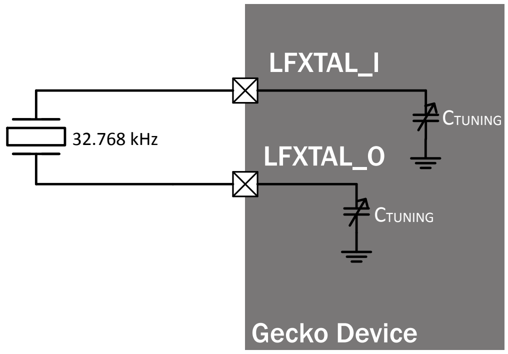


Figure 5.1. Low Frequency Crystal

Low frequency crystals connected to EFR32 Wireless Gecko Series 2 devices do not require external load capacitors, as these load capacitors are included on-chip and can be tuned by register bit fields under software control, thus reducing BOM cost and saving space in the PCB footprint. The EFR32 Wireless Gecko Series 2 LFXO supports 32.768 kHz crystals. Check device-specific data sheets for supported crystal load capacitance and ESR values and refer to device-specific reference manuals for on-chip load capacitor tuning instructions.

5.2.2 Low Frequency External Clocks

EFR32 Wireless Gecko Series 2 devices can source a low-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can either be a square wave or sine wave with a frequency of 32.768 kHz. The external clock source must be connected as shown in Figure 5.2 Low Frequency External Clock on page 12.

When a CMOS square wave source is used, the LFXO buffer must be placed in DIGEXTCLK bypass mode (LFXO_CFG.MODE = DIGEXTCLK). The clock signal must toggle between 0 V and V_{IOVDD} and the duty cycle must be 50%. When an external sine wave source is used, the LFXO buffer must be placed in BUFEXTCLK bypass mode (LFXO_CFG.MODE = BUFEXTCLK). The external sine source should have a minimum amplitude of 100 mV (zero-to-peak) and a maximum amplitude of 500 mV (zero-to-peak) and should be connected in series with the LFXTAL_I pin. The minimum voltage should be higher than ground and the maximum voltage less than V_{IOVDD}. The sine source does not need to be AC coupled externally as it is AC coupled inside the LFXO.

When using either DIGEXTCLK or BUFEXTCLK mode, the LFXTAL_O pin is free to be used as a general purpose GPIO.

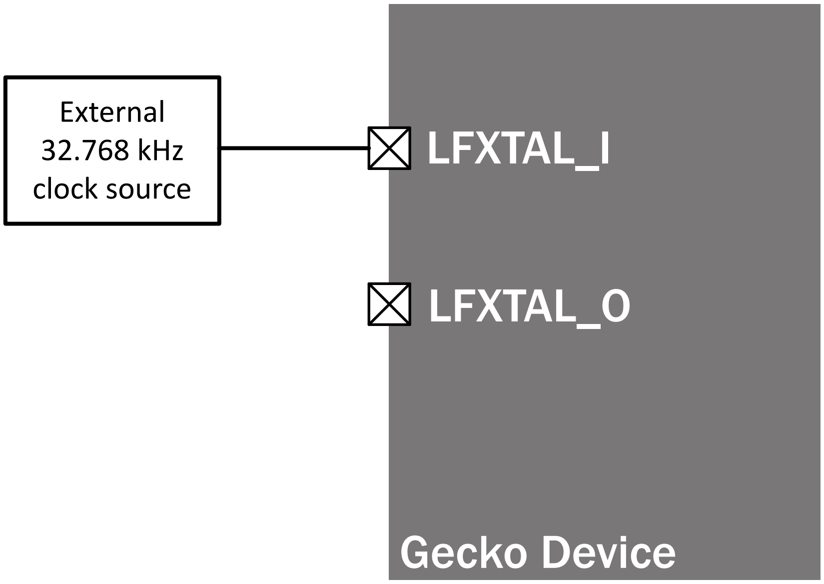


Figure 5.2. Low Frequency External Clock

5.3 High Frequency Clock Sources

The high frequency clock can be sourced from a crystal or ceramic resonator or from an external square or sine wave source.

5.3.1 High Frequency Crystals and Ceramic Resonators

A crystal or ceramic resonator is connected as shown in Figure 5.3 High Frequency Crystal Oscillator on page 13 across the HFXTAL_I and HFXTAL_O pins on EFR32 Wireless Gecko Series 2 devices. This circuit is valid for both crystals and ceramic resonators.

High frequency crystals connected to EFR32 Wireless Gecko Series 2 devices do not require external load capacitors, as these load capacitors are included on-chip and can be tuned by register bit fields under software control, thus reducing BOM cost and saving space in the PCB footprint. Although the EFR32 Wireless Gecko Series 2 HFXO can technically operate with crystal frequencies from 38.0 MHz - 40.0 MHz, any crystal frequency other than 38.4 MHz is expressly **not** supported by the radio, software, and protocol stacks. Check device specific data sheets for supported crystal load capacitance and ESR values and refer to device specific reference manuals for on-chip load capacitor tuning instructions

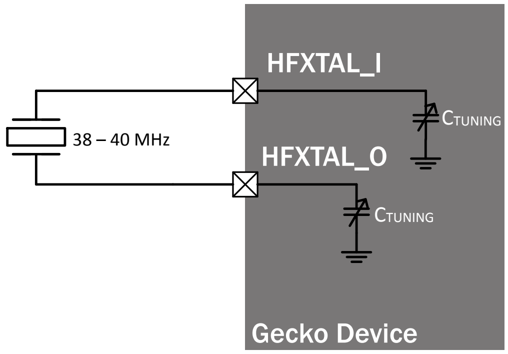


Figure 5.3. High Frequency Crystal Oscillator

5.3.2 High Frequency External Clocks

EFR32 Wireless Gecko Series 2 devices can source a high-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels.

Unlike the LFXO, which has specific modes for a buffered or digital external clock, the HFXO has more limited external clock input flexibility. The external clock signal should be a sine wave with a frequency in the range specified by the data sheet for the HFXO on the device in question, and should be connected to the HFXTAL_I pin. Although the EFR32 Wireless Gecko Series 2 HFXO can technically operate with external oscillator frequencies from 38.0 MHz - 40.0 MHz, any frequency other than 38.4 MHz is expressly **not** supported by the radio, software, and protocol stacks. Refer to the device-specific data sheet and reference manual for the options and requirements when sourcing an external high-frequency clock.

When an external high-frequency clock is sourced via the HFXO, it must be connected as shown in the figure below.

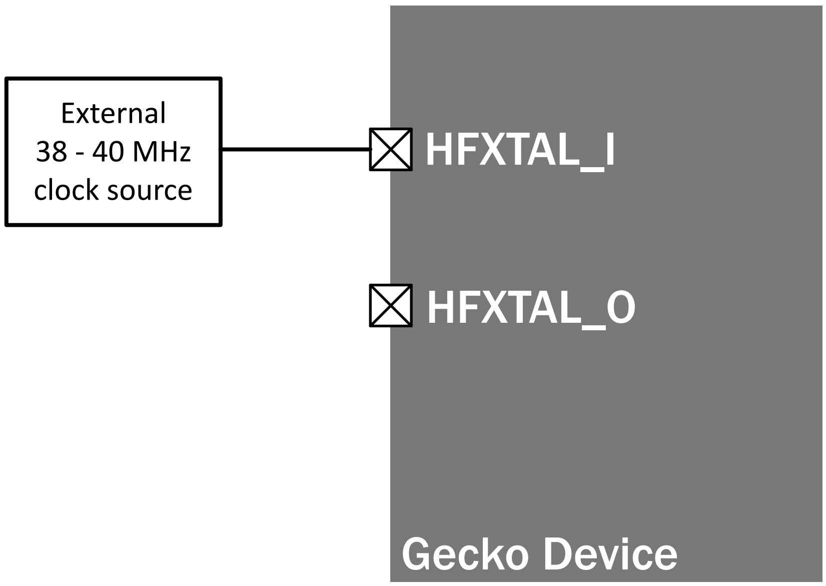


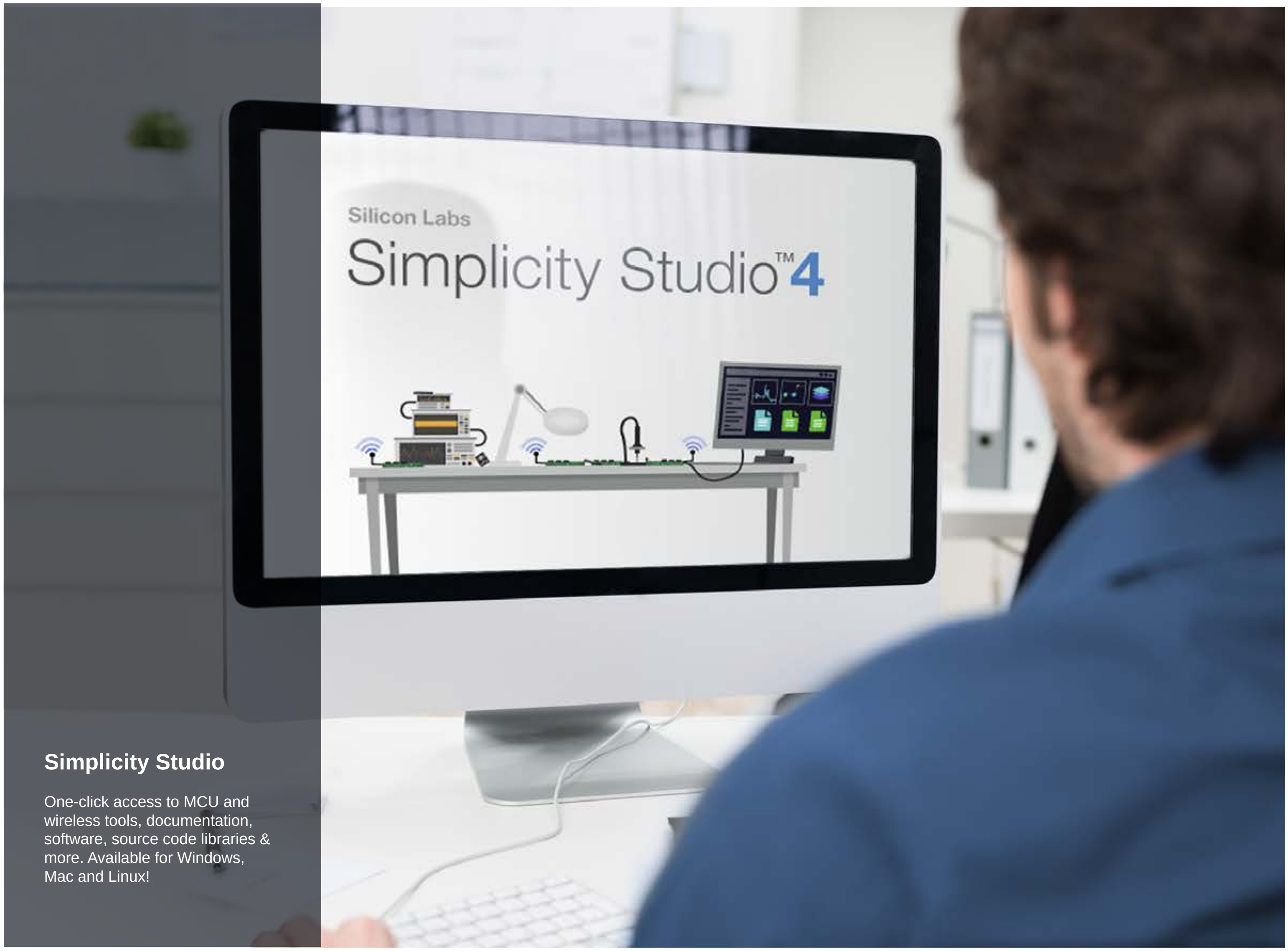
Figure 5.4. External High Frequency Clock

6. Revision History

6.1 Revision 0.1

February, 2019

- Initial revision.



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