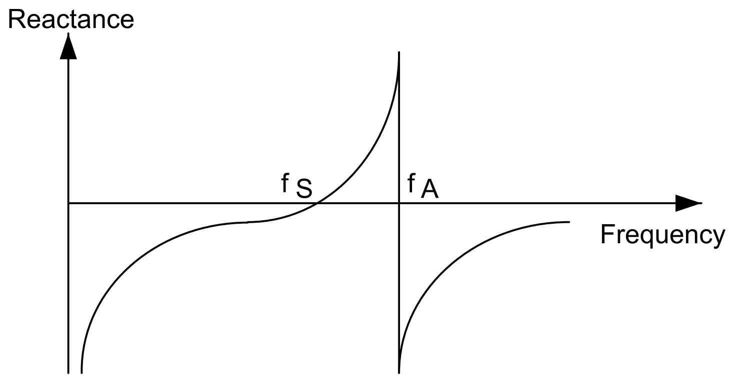
AN0016.2: Oscillator Design Considerations

This application note provides an introduction to the oscillators in Wireless SoC Series 2 devices and provides guidelines in selecting correct components for their oscillator circuits.

The Wireless SoC Series 2 devices contain two crystal oscillators: one low frequency (32.768 kHz) and one high frequency (38.4 MHz). Topics covered include oscillator theory and some recommended crystals for these devices.

KEY POINTS

- Learn which parameters are important when selecting an oscillator.
- Learn how to properly configure a crystal oscillator for use with Wireless SoC Series 2 devices.



1. Device Compatibility

This application note supports multiple device families, and some functionality is different depending on the device.

Wireless SoC Series 2 consists of:

- EFR32BG21
- EFR32MG21
- EFR32BG22
- EFR32MG22

2. Oscillator Theory

2.1 What is an Oscillator?

An oscillator is an electronic circuit which generates a repetitive, or periodic, time-varying signal. In the context of Wireless SoC Series 2 devices, this oscillator signal is used to clock execution of instructions and peripherals in the device. For radio communication the oscillator also provides an accurate and low noise frequency reference to the transciever. There are multiple ways of generating such a signal, each with different properties that influence project cost, board size, and stability of the clock signal.

RC oscillators

RC oscillators are built from resistors, capacitors, and an inverting amplifier. They come at a low cost and have a shorter startup time than the crystal oscillator, but are generally less accurate and produce more noise. The Wireless SoC Series 2 devices provide multiple internal RC-oscillators including one high frequency RC oscillator (HFRCO) and one low frequency RC oscillator (LFRCO). While the internal RC-oscillators will ensure proper operation of the Wireless SoC Series 2 device, they are inadequate for applications such as radio communication.

Crystal oscillators

Crystal oscillators use the mechanical vibration of a crystal to generate the clock signal. Due to the molecular composition of the crystal matter and the angle of which the crystal is cut, this type of oscillator is very precise and stable over a wide temperature range. The most commonly used crystal is the quartz crystal. Producing quartz crystals requires very stable temperature and pressure conditions over a few weeks. This makes crystal oscillators more expensive than RC oscillators.

2.1.1 Piezoelectricity

Quartz crystals hold the direct piezoelectric property. This means an applied electric field will cause the crystal to deform. Conversely, a deformation of the crystal will cause a voltage across the terminals. Once the oscillator has started, the changing voltage on the terminals of the vibrating crystal is used as the clock signal.

2.2 Basic Principle of Oscillators

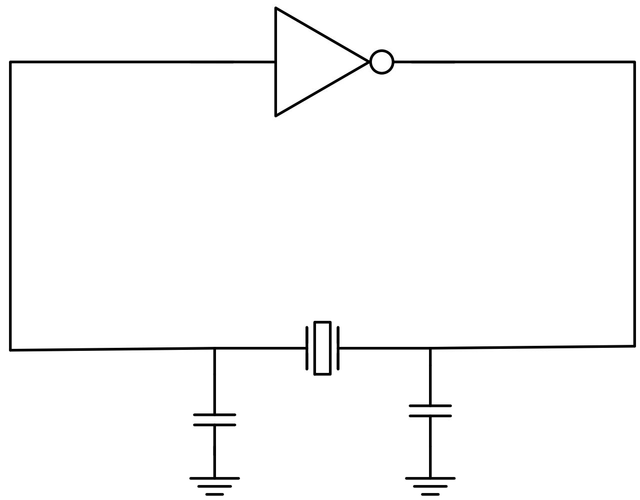


Figure 2.1. Simplified Feedback Oscillator Loop

The principle behind the oscillator is a positive feedback loop satisfying the Barkhausen condition: If the closed-loop gain is larger than unity and the total phase lag is 360°, the resulting closed-loop system is unstable and will self-reinforce. This is a necessary, but not sufficient, condition for oscillations to be present. When the necessary conditions are met, any disturbance (noise) in the oscillator will cause oscillations to start. The frequency that fulfills the Barkhausen condition is amplified the most, because it is in phase with the original signal.

The initial oscillations are very weak and it takes time to amplify the signal to the desired magnitude. When oscillations are established, only a small amount of energy is needed to compensate for losses in the circuit. Mathematically, a closed-loop gain of one is required to maintain steady state oscillations. The Wireless SoC Series 2 relies on an adjustable current source controlled by automatic gain controller to achieve and maintain the desired amplitude.

Figure 2.1 Simplified Feedback Oscillator Loop on page 4 shows that the oscillator circuitry consists of two parts: an amplification stage and a filter that decides which frequency experiences a 360° phase lag. In the case of a crystal oscillator, the filter consists of the crystal and external load capacitors.

2.2.1 Startup time

The magnitude of the closed-loop gain has great influence on the startup time. Low gain can cause excessively long startup time or failure, and too high gain can startup to fail altogether. The ideal gain is dependent on the negative resistance of the oscillator circuit, which is defined in Negative Resistance.

For the same reason, the oscillation frequency influences the startup time. A crystal in the kHz range would have a considerably longer startup time than a crystal in the MHz range because the time it takes to circulate the loop is longer. Typical startup times for the Wireless SoC Series 2 are 63 ms for the low frequency oscillator and 159 μs for the high frequency oscillator.

2.3 Modeling the Crystal

The crystal can be described by the electrical equivalent circuit in Figure 2.2 The Electrical Equivalent Circuit of a Crystal on page 5.

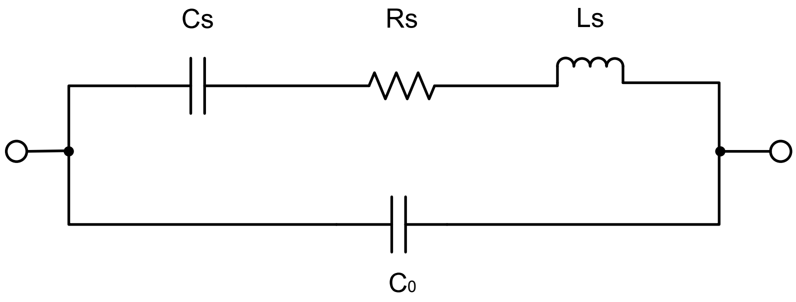


Figure 2.2. The Electrical Equivalent Circuit of a Crystal

- C_S is the motional capacitance. It represents the piezoelectric charge gained from a displacement in the crystal.
- R_S is the motional resistance. It represents the mechanical losses in the crystal.
- L_S is the motional inductance. It represents the moving mass in the crystal.
- C_0 is the shunt capacitance between the electrodes and stray capacitance from the casing.

For low frequencies, the electrical equivalent circuit will exhibit capacitive behavior as depicted in Figure 2.3 Reactance vs. Frequency on page 5. The presence of the inductor becomes more noticeable as the frequency, and thus the reactance, increases. Ignoring the shunt capacitance C_0, the series resonant frequency is defined where the reactance of the inductor and capacitor cancels. At this frequency the crystal appears only resistive with no shift in phase. The series resonance frequency, f_S, therefore determines the relationship between C_S and L_S. This can be calculated with the equation below. The series resonance frequency is the natural resonance frequency where the energy transformation between mechanical and electrical energy is most effective.

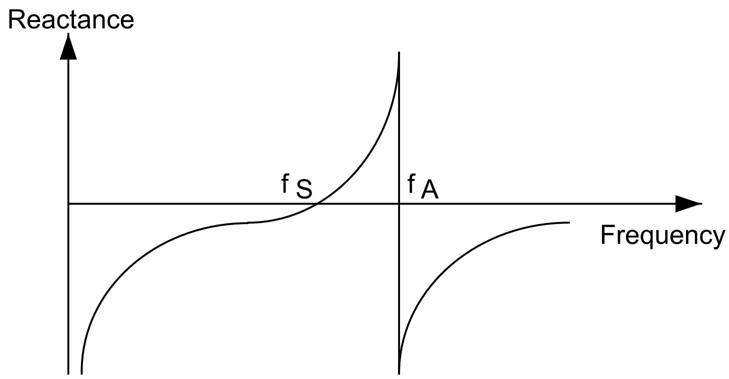


Figure 2.3. Reactance vs. Frequency

$$f_S = \frac{1}{\left(2 \times \pi \times \left(L_S \times C_S\right)^{\frac{1}{2}}\right)}$$

At higher frequencies, the equivalent circuit will appear inductive, which implies higher impedance. When the inductive reactance from the crystal cancels the capacitive reactance from shunt capacitance C_0, another resonance frequency with zero phase shift exists. This frequency is called the anti-resonant frequency, f_A. At this frequency, the impedance is 0.

$$f_A = \frac{1}{\left(2 \times \pi \times \left(L_S \times \frac{C_S \times C_0}{C_S + C_0}\right)^{\frac{1}{2}}\right)}$$

The range of frequencies between f_S and f_A is called the area of parallel resonance and is where the crystal will normally oscillate. At the resonant frequency, the phase lag in the feedback loop is provided by an amplifier with 180° phase lag and two capacitors with a combined 180° phase lag. In practice, the amplifier provides a little more than 180° phase shift, which means the crystal has to appear slightly inductive to fulfill the Barkhausen criterion.

2.3.1 Series and Parallel Resonant Crystals

Physically there is no difference between series and parallel resonant crystals. Series resonant crystals are specified to oscillate at the series resonant frequency where the crystal appears with no reactance. Because of this, no external capacitance should be present as this would lower the oscillating frequency to below the natural resonance frequency. These crystals are intended for use in circuits with no external capacitors where the oscillator circuit provides 360° phase shift.

Parallel resonant crystals require a capacitive load to oscillate at the specified frequency and this is the resonance mode required for Wireless SoC Series 2 devices. On Wireless SoC Series 2 devices, the load capacitors are located on-chip, and their values can be controlled by firmware. Thus, Wireless SoC Series 2 devices do not require external load capacitors, reducing BOM cost and saving PCB space. The exact oscillation frequency for a parallel resonant crystal can be calculated with the equation below, where C_L is the load capacitance seen by the crystal. C_L is therefore an important design parameter and is given in the data sheet for parallel resonant crystals.

$$f_P = f_S\left(1 + \frac{C_S}{2 \times C_L}\right)$$

3. Wireless SoC Series 2 Crystal Oscillators

The Wireless SoC Series 2 devices include two crystal oscillators, the Low Frequency Crystal Oscillator (LFXO) and the High Frequency Crystal Oscillator (HFXO). These oscillators require an external clock or crystal connected to the crystal oscillator pins of the device, however, no external crystal load capacitors are required as they contain on-chip tunable load capacitors. The LFXO supports crystals with a nominal frequency of 32.768 kHz, while the HFXO supports 38.4 MHz. External oscillators which provide sine waves are also supported. Both the high and low frequency clock sources can be used simultaneously.

In the Wireless SoC Series 2 oscillator circuits are designed as a Pierce oscillator as shown in Figure 3.1 The Pierce Oscillator in the Wireless SoC Series 2 on page 7.

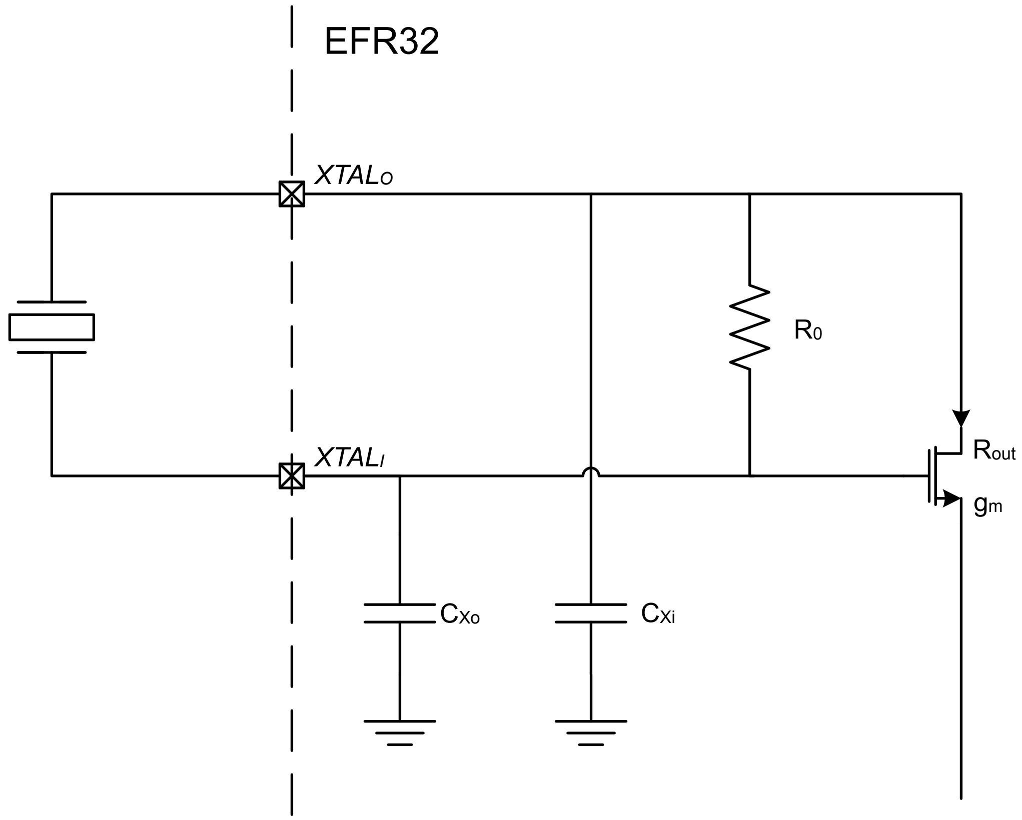


Figure 3.1. The Pierce Oscillator in the Wireless SoC Series 2

The Pierce oscillator is known to be stable for a wide range of frequencies and for its low power consumption.

The Wireless SoC Series 2 crystal oscillators use a relatively low oscillation amplitude, which can lead to a lower oscillation frequency than stated as the nominal value in the crystal's data sheet. More information on this effect is given in 6.4 Frequency Pulling.

3.1 Timeout

To ensure that the XO clock signals are not used internally in the Wireless SoC Series 2 before they are stable, both the HFXO and the LFXO include a configurable timeout. When the XO starts up, the timeout counter will count to the configured number of cycles before the clock signal propagates to the internal clock trees and the digital logic.

3.2 Software Configuration

The LFXO/HFXO can be easily configured by leveraging the em_lib library. The library contains oscillator initialization structures and functions which abstract the software options available for each oscillator. The included 7. Software Examples showcase using the library to initialize the oscillators.

At the register level, the HFXO and LFXO oscillation start-up are controlled by the HFXO_XTALCTRL, HFXO_XTALCFG, LFXO_CFG registers. See the reference manual for detailed register level descriptions of the configuration options available for the external oscillators.

Starting up the HFXO in crystal mode

When configuring the HFXO for proper crystal startup, most fields such as the bias currents and timeout durations should adhere to the em_lib defaults (`CMU_HFXOINIT_DEFAULT` in `em_cmu.h`). The tuning capacitor values should be customized by setting the `ctuneXoAna` and `ctuneXiAna` fields of the HFXO initialization struct. The tuning capacitor values can be determined via the following methods.

- For parts on a starter or development kit, the calibrated tuning values can be read from the the `DEVINFO_MODXOCAL` register the Device information page (see 7. Software Examples for details).
- For oscillators on our Recommended Oscillators list, use the emlib defaults.
- For other oscillators, the setting should be determined based on the oscillator load capacitance, and the tuning capacitor range and step size values from the Wireless SoC Series 2 device datasheet.

For any of these methods, the tuning values should be trimmed or calibrated for optimal accuracy. See the Tuning Strategies section for details.

Starting up the LFXO in crystal mode

When configuring the LFXO for proper crystal startup, the gain and tuning values may need to be modified from the em_lib defaults (`CMU_LFXOINIT_DEFAULT` in `em_cmu.h`). These correspond to the `ctune` and `gain` fields of the em_lib LFXO initialization struct. The tuning values can be determined via the following methods

- For parts on a starter or development kit, the calibrated tuning values can be read from the the `DEVINFO_MODXOCAL` register the Device information page (see 7. Software Examples for details).
- For other oscillators, the setting should be determined based on the oscillator load capacitance, and the tuning capacitor range and step size values from the Wireless SoC Series 2 device datasheet.

The gain value should be set according to the load capacitance of the crystal.

- For 12.5 pF ≤ CL ≤ 18 pF, set GAIN = 3
- For 8 pF ≤ CL ≤ 12.5 pF, set GAIN = 2
- For 6 pF ≤ CL ≤ 8 pF, set GAIN = 1
- For CL ≤ 6 pF, set GAIN = 0

3.3 PCB Layout

To minimize noise sensitivity caused by parasitic antenna and spurious coupling phenomena, the distance between the crystal, and the Wireless SoC Series 2 oscillator pins should be as short as possible. If it is not possible to place the external oscillator components close to the oscillator pins, care should be taken when routing these signals. Avoid long traces underneath the Wireless SoC Series 2 package and other circuitry that could create spurious coupling with logic activity. Also avoid routing any other signals through the crystal area.

Ensure that the ground plane underneath the oscillator is of good quality. Do not use a separate ground plane under the oscillator with a narrow connection to the reference ground as this can act as an antenna. To avoid coupling from surrounding signal traces, it is a good practice to place a grounded guard ring around the oscillator and its components.

4. Considerations for Radio Applications with the Wireless SoC Series 2 Portfolio

4.1 General Notes

This section adds a few details about specific requirements related to wireless applications.

On Wireless SoC Series 2 devices the recommended frequency value is 38.4 MHz. Transceiver electrical specifications are based on these frequencies, and Silicon Labs protocol stacks use these as the default.

The crystal frequency tolerance is determined by various aspects of the design:

Required frequency tolerance of the protocol

For example, 802.15.4 applications require ±40 ppm accuracy under all conditions.

Temperature range

The S-shaped temperature characteristic of AT-cut crystals becomes steeply negative at low temperatures, steeply positive at high temperatures. A larger temperature range requires a specific cut angle of the crystal to bound the absolute accuracy. Most crystals are specified from -40 °C to +85 °C, but some applications may require operation up to 105 °C or 125 °C ambient temperature.

Manufacturing accuracy

Individual crystals have a frequency error at 25 °C. This is typically specified as ±10 ppm "manufacturing tolerance" or "make tolerance". This error adds to the temperature error.

Aging tolerance

Crystals drift over time, typically 1-2 ppm per year. Excessive heat during assembly or from hand soldering may also prematurely age a crystal.

The allowable frequency error of the crystal is the sum of temperature, board-to-board, and crystal-to-crystal variations.

4.2 Crystal Loading and Production Tuning

The load capacitance, C_L, is implemented on-chip by two tunable capacitors. External capacitors are neither required nor recommended.

The load capacitor tuning range in pF is given in the data sheet by C_{HFXO_T} with a resolution of SS_{HFXO} per step. The resulting frequency per step depends on the crystal's pulling sensitivity and the shunt capacitance of the oscillator circuit.

4.2.1 Tuning Strategies

The on-chip variable load capacitor may be used in one of two ways.

- A fixed value may be used for all units. During design a number of units should be characterized and an average center CTUNE value determined. Some crystal vendors may provide characterized samples to help tune to the center of the crystal distribution. In corner cases the remaining error should be in the order of a few ppm only, depending on manufacturing spread (PCB parasitics, component variation, etc.).
- Each unit may also be calibrated in production. A unique value of CTUNE is determined per unit and stored in flash memory. This calibrates out the manufacturing error of the crystal, leaving only the temperature error and aging components. This may allow the system to operate across a broader temperature range or with a less accurate crystal at the expense of production calibration time.

The variable on-chip loading capacitor can theoretically be used to offset temperature-induced errors as well. While simple in concept, this is difficult in practice primarily due to temperature characteristic differences from crystal to crystal.

Crystal ppm error can be measured by outputing a clock signal to a GPIO pin. This process, along with example code demonstrating oscillator calibration, is described in *AN0004.2: EFR32 Series 2 Wireless MCU Clock Management Unit (CMU)*

4.3 External Tuning Capacitance

All required crystal loading capacitance is on-chip, therefore, external loading capacitors are not recommended.

4.4 External Oscillator Operation

For narrowband applications the system reference frequency may be provided by an external oscillator such as a Temperature Compensated Crystal Oscillator (TCXO). To use a TCXO, the output should be connected to the HFXTAL_I pin and the `CMU_HFXOINIT_EXTERNAL_SINE` struct definitions should be used for HFXO initialization in software using the `em_cmu` library.

Sine and clipped sine waveforms are supported by the HFXO in this mode. The external waveform should adhere to the following limitations for ideal performance.

	Min (V)	Max (V)
Input Voltage	0.0	1.2
Peak-to-Peak Amplitude	0.3	0.6

See Recommended Oscillators for a list of recommended TCXOs.

4.5 Reducing Power Consumption

The power consumption of the crystal oscillator is mostly determined by the drive level of the oscillator. This equals the power dissipated in the crystal as given in the equation below.

$$DL = \frac{1}{2} \times ESR \times \left(2 \times \pi \times f \times V_{pp} \times \left(C_0 + C_L\right)\right)^2$$

V_{pp} is the peak to peak voltage across the crystal at the resonance frequency. In Wireless SoC Series 2 devices the target Vpp varies, but for a safe estimate to check the maximum drive level for a given crystal, calculate the above formula with a 500mV V_{pp} value.

During startup the current consumption is higher than after oscillations have stabilized. A short startup time reduces the period in which the current consumption of the oscillator is high and is therefore essential if the oscillator is frequently switched on and off. In general one would like the circuit to be operational as fast as possible and a fast startup time is therefore favorable. Crystals with low ESR and load capacitance typically have the shortest startup time and consume the least amount of power.

On Wireless SoC Series 2 devices, the oscillators can be configured to be "on-demand". This means that the oscillator will be automatically enabled as requested by the clock management unit and then automatically disabled when not in use. This can help save power at the cost of incurring repeated startup delays whenever the oscillator is needed. Alternatively the oscillator can be enabled in software and forced to stay on, consuming extra current in exchange for no recurring startup delays. This option is showcased in the included Software Examples.

5. Recommended Crystals

5.1 General Notes for Crystal Selection

When deciding upon which crystal to employ, the following considerations could be helpful to ensure a proper functioning oscillator.

Operating environment

Temperature, humidity, and mechanical vibration affect the stability properties. For crystals, define what crystal cut is most appropriate for the application. For most applications, AT cut is an excellent choice due to good temperature stability over a wide temperature range. SC cut has good stability when exposed to mechanical vibrations, but suffers from humidity and temperature changes. Many more cuts with different properties exists.

Package

Surface mount or through-hole. If size is critical, define maximum package dimensions.

Match load capacitors

Ensure that C_L is within range specified by the Wireless SoC Series 2 data sheet. Generally lower load capacitance crystals have better startup and current consumption performance, see 4.5 Reducing Power Consumption for details.

Match ESR

Ensure that ESR is within range specified by the Wireless SoC Series 2 data sheet. Generally lower ESR crystals have better startup and current consumption performance, see 4.5 Reducing Power Consumption for details.

The recommended crystals are chosen from a selection of popular crystals with different ESR, cost, frequency stability, and tolerance. By examining the list of considerations above, one should be able to find a suitable crystal.

All the recommended crystals are fundamental mode, as is required for Wireless SoC Series 2.

5.2 Crystal Specifications for Wireless SoC Series 2

The following crystals have been tested for use with Wireless SoC Series 2. Suitability for a particular application should be verified. Different frequency tolerance / temperature ranges may be available. Contact the crystal vendor for details.

Table 5.1. 38.4 MHz Crystals

Mfg	Part	Spec.	ESR (Ω)	C_0 (max) (pF)	Temp (°C)	Temp Tolerance (ppm)	Mfg Tolerance (ppm)	C_L (pF)	Foot-print (mm)
Tai-Saw	TZ2205E		40	3	-40 to +125	± 30	± 10	10	1.60 x 2.00
Tai-Saw	TZ3398B		40	3	-40 to +105	± 20	± 10	10	1.65 x 2.05
NDK	NX2520SA	EXS00A-CS08361	40	1.26	-40 to +125	± 32	± 10	10	2.50 x 2.00
Murata	XRCGB-F-S	XRCGB38M400F1S2AR0	40	3	-40 to +105	20	10	10	2.00 x 1.60

Table 5.2. 38.4 MHz TCXOs

Mfg	Part	Supply Voltage (V)	Output Voltage (V_{pk-pk})	Temp (°C)	Current Consumption (mA)	Frequency Tolerance (ppm)	Footprint (mm)
NDK	NT2016SA-38.4MHz-END5109A	1.8 to 3.6	0.8	-40 to +105	1.7	± 2	1.6 x 2.0

Table 5.3. 32768 Hz Crystals

Mfg	Part	Spec.	ESR (kΩ)	C_0 (typ) (pF)	Temp (°C)	Tolerance (ppm)	C_L (pF)	Footprint (mm)
MCS	MS3V-T1R		65	0.9	-40 to +85	20	12.5	Tuning Fork
KDS	DST1610A	1TJH070DN1A0153	70	1.3	-40 to +85	20	7.0	1.6 x 1.0
KDS	DST210AC	1TJG070DN1AC001	70	1.3	-40 to +85	20	7.0	2.0 x 1.2

6. Crystal Parameters

6.1 Quality Factor

The quality factor Q is a measure of the efficiency or the relative storage of energy to dissipation of energy in the crystal. For the electrical-equivalent circuit, the equation below states the relation between R, C and Q. In practice, crystals with higher Q-values are more accurate, but have a smaller bandwidth for which they oscillate. Therefore, high Q-factor crystals will start slower than crystals with higher frequency tolerance.

$$Q = \frac{X_{LS}}{R_S} = \frac{1}{(X_{CS} \times R_S)} = \frac{1}{(2 \times \pi \times f \times C_S \times R_S)} = \frac{2 \times \pi \times f \times L_S}{R_S}$$

X_{L_S} and X_{C_S} are the reactance of L_S and C_S, respectively, at the operating frequency of the crystal.

6.2 Load Capacitance

As seen in the equation below, the two capacitors C_{L1} and C_{L2} provide capacitive load for the crystal. The effective load capacitance, C_L, as seen from the HFXTAL_I and HFXTAL_O pins on the Wireless SoC Series 2 is the series combination of C_{L1} and C_{L2} through ground.

$$C_L = \frac{(C_{L1} \times C_{L2})}{(C_{L1} + C_{L2})} + C_{stray}$$

Where C_{stray} is the pin capacitance of the microcontroller and any parasitic capacitance, and can often be assumed in the range 2-5 pF. Right choice of C_L is important for proper operating frequency. Crystals with small load capacitance would typically start faster than crystals requiring a large C_L. Large load capacitors also increase power consumption. It is recommended to use a crystal with C_L as specified in 5. Recommended Crystals. The Wireless SoC Series 2 device data sheets also contain more information on the allowed load capacitance range.

Note: The Wireless SoC Series 2 devices have internal loading capacitors and do not need external capacitors connected to the crystal. See the device data sheet or reference manual for more information.

6.3 Equivalent Series Resistance

The Equivalent Series Resistance is the resistance in the crystal during oscillation and varies with the resonance frequency. ESR, given by the equation below, will typically decrease with increasing oscillation frequency.

$$\text{ESR} = R_S\left(1 + \frac{C_0}{C_L}\right)^2$$

The HFXO/LFXO circuits of the Wireless SoC Series 2 cannot guarantee startup of crystals with ESR larger than a certain limit. Please refer to the device data sheet for further details. The smaller the ESR, compared to this maximum value, the better gain margin for startup of the crystal which in turn reduces the startup time. Additionally, a small ESR value gives lower power consumption during oscillation.

Note that HF crystals have ESR of a few tens of Ohms as compared to the LF crystals, which have ESR values normally measured in kΩ. Therefore, a few Ohms of series resistance has more influence on the startup margin in the MHz range as compared to the kHz range.

6.4 Frequency Pulling

As the crystal oscillators in the Wireless SoC Series 2 use a relatively low oscillation amplitude, the oscillation frequency can be lower than stated in the data sheet when using the suggested load capacitance. This offset is best found by measuring the resulting frequency when using the suggested load capacitance. The offset will be stable and not affected by temperature, voltage or aging. If it is desirable to achieve the nominal frequency given for the crystal, there are two options:

- Option A — Order a crystal from the crystal vendor that has a nominal frequency equal to the frequency you want to achieve plus the measured offset frequency.
- Option B — It is possible to slightly alter the oscillation frequency of a crystal by adjusting the load capacitance (C_{L1} and C_{L2}). The pullability of the oscillation system refers to which extent it is possible to tune the resonance frequency of the crystal by changing these values. The crystal sees these capacitors in series through ground, parallel to the closed loop. They will therefore slightly alter the anti-resonance frequency of the crystal. The equation below shows the pullability in terms of frequency change in ppm per change in combined load capacitance in pF.

$$\text{Average pullability (ppm/pF)} = \frac{C_S \times 10^6}{2 \times \left(C_0 + C_L\right)^2}$$

6.5 Drive Level

Drive level is a measure of the power dissipated in the crystal. The crystal manufacturer should specify the maximum power dissipation value tolerated by the crystal in the crystal data sheet. Exceeding this value can damage the crystal.

$$\text{DL} = \text{ESR} \times I^2$$

Here, I is the RMS current flowing through the crystal.

6.6 Minimum Negative Resistance

A critical condition for oscillations to build up requires the energy supplied to exceed the energy dissipated in the circuit. In other words, the negative resistance of the amplifier has to exceed the equivalent series resistance in the crystal. An approximate formula for negative resistance is given in the equation below.

$$R_{\text{neg}} = \frac{-g_m}{\left((2 \times \pi \times f)^2 \times C_{L1} \times C_{L2}\right)}$$

Where g_m is the transconductance of the oscillator circuitry. To ensure safe operation over all voltage and temperature variations, ensure that the ESR does not exceed the device data sheet maximum. This maximum value corresponds to the oscillator circuit's realizable negative resistance.

If the crystal ESR does not satisfy this criterion, another crystal with lower ESR should be chosen. The equation above shows an approximate formula for this calculation which excludes shunt capacitance and internal loss.

6.7 Frequency Stability

Frequency stability is the maximum frequency deviation from the specified oscillating frequency over the given operating temperature range.

6.8 Frequency Tolerance

Frequency tolerance is the maximum frequency deviation from the specified oscillating frequency at 25 °C. This parameter gives an indication of variations between individual crystals.

7. Software Examples

The software example project and source code is available through the Silicon Labs technical resource search: https://www.silabs.com/support/resources.ct-example-code?query=an0016%202. The software example is run on the EFR32xG21 Radio Board and Wireless Starter Kit, but is easily ported to other Wireless SoC Series 2 devices on custom boards.

8. Revision History

Revision 1.2

July, 2020

- Added the Murata XRCGB-F-S HFXO to the recommended crystals list
- Updated diagram for Figure 3.1, corrected pin names

Revision 1.1

June, 2020

- Updated supported frequencies for radio operation in 4.1 General Notes
- Updated External Sine Operation section to provide recommendations for input waveforms
- Added recommended TCXO list

Revision 1.0

March, 2020

- Added device compatibility for EFR32BG22 and EFR32MG22
- Added DST1610A and DST210AC specifications to the Recommended Crystals section
- Added drive level calculation and additional information to the Recommended Crystals section

Revision 0.3

July, 2019

- Added TZ3398B, fixed NX2520SA specifications, and removed the unpopulated Crystal Configuration table from the Recommended Crystals section
- Removed references to crystal configuration table in the Software Configuration section
- Corrected minor wording and grammar issues

Revision 0.2

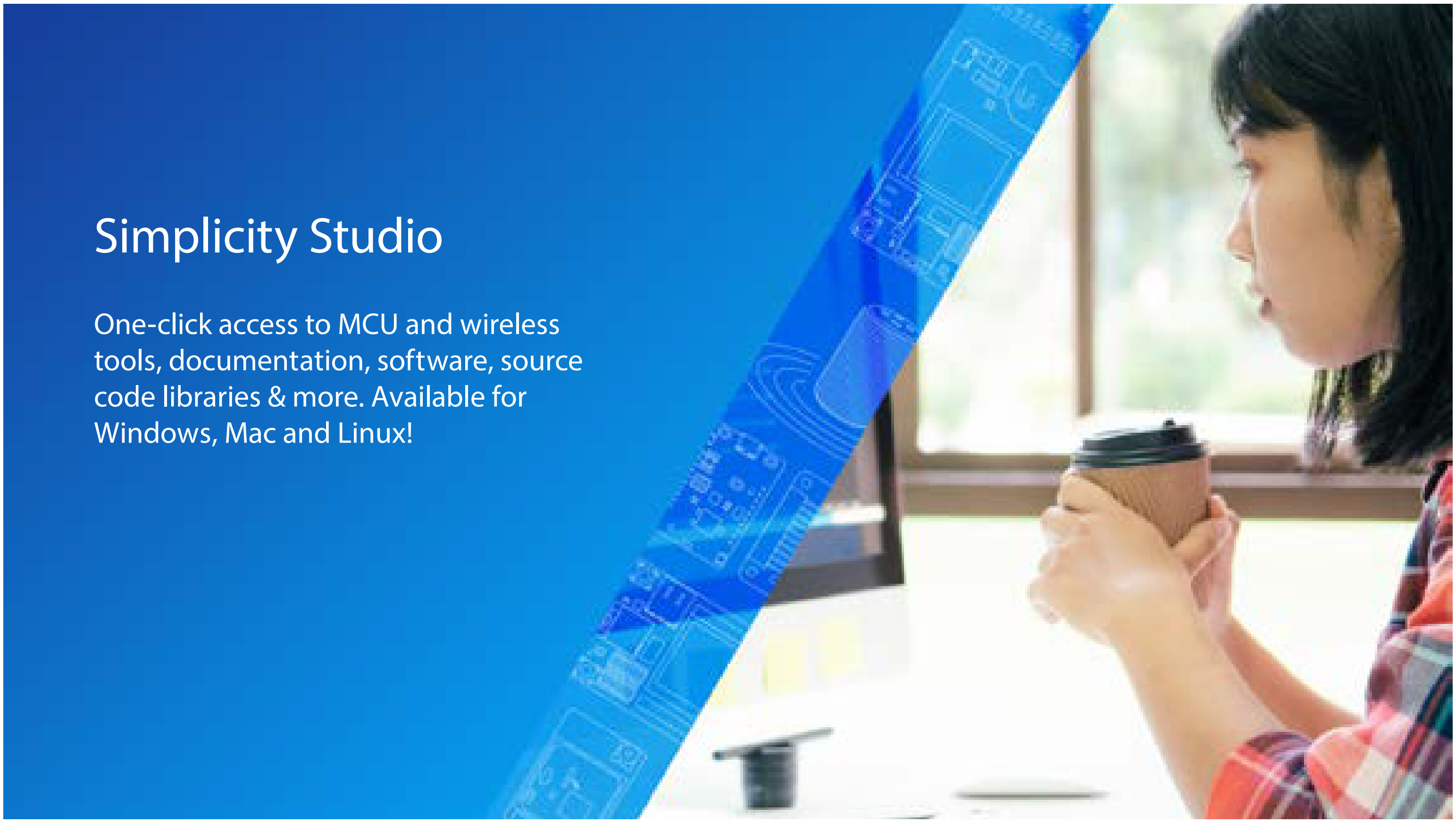
May, 2019

- Added oscillator recommendations

Revision 0.1

April, 2019

- Initial revision



IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support & Community
www.silabs.com/community

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com