AN0018.2: Supply Voltage Monitoring

This application note will demonstrate how to use the EFR32 Series 2 EMU's Reset Management Unit to determine if a brown-out reset has occurred and will also demonstrate the supply voltage monitoring functionality using ACMP, IADC and DCDC.

For Supply Voltage Monitoring example projects, see: https://github.com/SiliconLabs/peripheral_examples

KEY POINTS

- Observe RMU to determine reset cause.
- Monitor power rails for low voltage conditions with ACMP
- Monitor power rails for low voltage conditions with IADC.
- Monitor power rails for low voltage conditions with DCDC.

1. Device Compatibility

This application note supports multiple device families, and some functionality is different depending on the device.

EFR32 Wireless Gecko Series 2 consists of:

- EFR32BG21
- EFR32MG21
- EFR32BG22
- EFR32BG22L
- EFR32FG22
- EFR32MG22
- EFR32FG23
- EFR32SG23
- EFR32ZG23
- EFR32BG24
- EFR32BG24L
- EFR32MG24
- EFR32FG25
- EFR32BG27
- EFR32MG27
- EFR32FG28
- EFR32SG28
- EFR32ZG28

EFM32 Series 2 consists of:

- EFM32PG22
- EFM32PG23
- EFM32PG28

2. Reset Management Unit

The Reset Management Unit (RMU) monitors the reset lines and ensures reliable operation by resetting the microcontroller if any of the supply voltages are insufficient or if certain events occur. Such events are activation of the external reset pin, watchdog timeout, kernel lockup or a system reset request. In addition, the RMU sets the reset cause register which can be used to determine the cause of the last reset at startup.

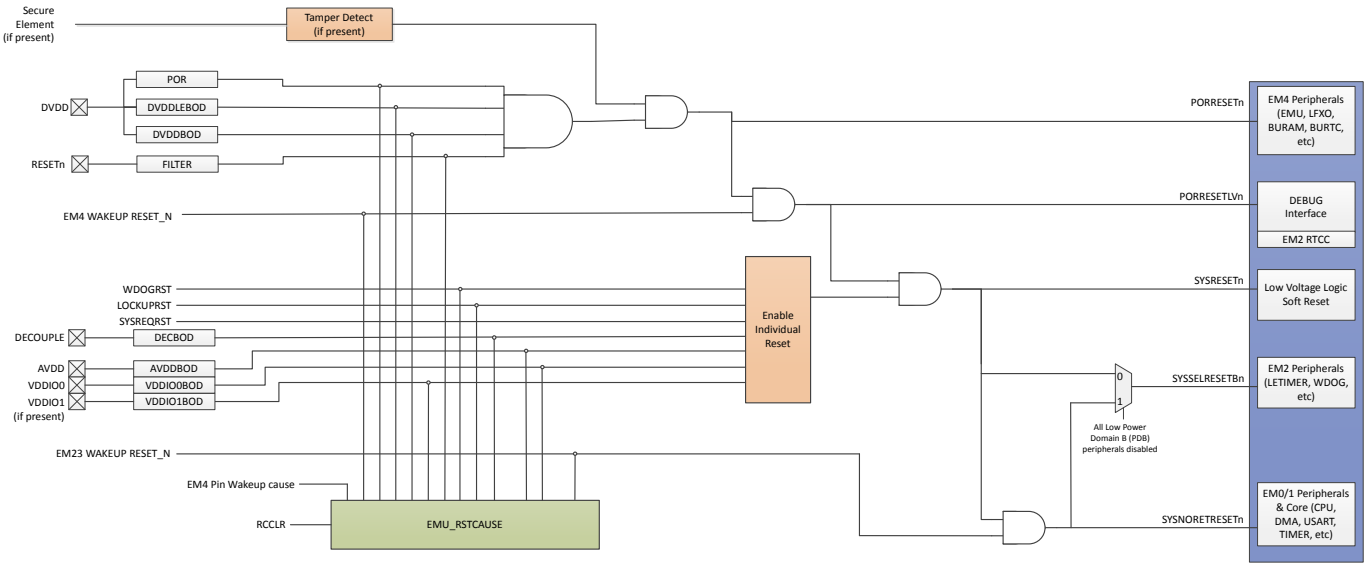


Figure 2.1. Reset Tree

2.1 Power-on Reset (POR) and Brown-out Detection

The POR ensures that the device does not start up before the DVDD supply voltage has reached the threshold voltage $VPOR_{thr}$. Before the POR threshold voltage is reached, the device is kept in reset state. Once the POR threshold is reached, the device's Brown Out Detectors engage, keeping the device in reset until their thresholds are met.

If, during device operation, the supply voltage falls below the one of the brown-out detector threshold voltages, a "brown-out" has occurred. The brown-out detector that has had its threshold crossed will pull the microcontroller into reset to prevent unexpected program execution and data corruption. EFR32 Series 2 devices have several reset sources noted in the following section.

Once the RMU initiates a reset, the reset cause register is written to specify the reset source. If the supply voltage has fallen below the BOD threshold, but not below the POR threshold, the RMU will report the corresponding brown-out reset cause. If the supply voltage has fallen below the POR threshold, a POR reset cause will be reported.

2.2 Reading the Reset Cause Register

The reset cause register indicates which reset source triggered the last reset. Because several bits can be set at once and multiple reset causes can occur simultaneously, it is important to look for the reset cause in the following order to discover the main cause of reset:

- Power-on reset
- RESET pin reset
- EM4 wakeup
- Watchdog reset
- Core lockup condition
- Software triggered reset
- Brown-Out Detection (BOD)

When following this list from the smallest to largest number, the first indicated reset cause will be the actual reset cause. The reset cause register needs to be cleared after it has been read, otherwise it may indicate a wrong cause of reset at the next startup. To clear the reset cause register a 1 has to be written to the RSTCAUSECLR bit in EMU_CMD.

The EFR32 software library contains functions to read and clear the reset cause register.

3. Supply Voltage Monitoring using ACMP

All devices except EFx32xG22 and EFR32xG27 feature two Analog Comparators (ACMP) which are operational down to EM3. EFR32xG27 features one Analog Comparator which are operational down to EM3. The ACMP is configured and controlled through three registers: ACMP_CFG, ACMP_CTRL, and ACMP_INPUTCTRL.

Configuration through ACMP_CFG needs to happen before the ACMP is enabled. The control registers ACMP_CTRL and ACMP_INPUTCTRL can only be updated after the ACMP is enabled. The following sources are available for the ACMP:

- AVDD Supply voltage[1]
- 1.25V and 2.5V References[1]
- VSENSE0[2], VSENSE1[2]
- GPIO Analog Bus
- Ground
- VDAC auxiliary outputs

Notes:

1. VREF sources have a 64-Level Divider.
2. VSENSE has a fixed ¼ Divider.

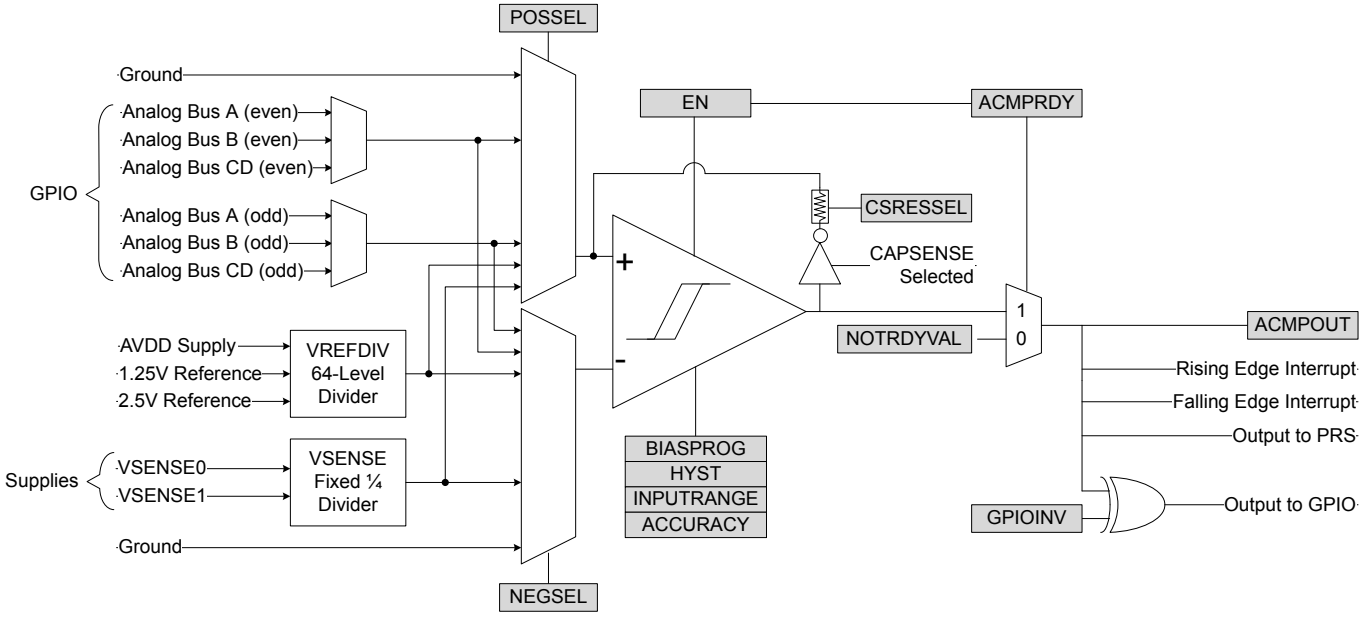


Figure 3.1. ACMP Overview

The ACMP provides an easy way to warn if the supply voltage reaches a critical level. While the RMU automatically initiates a reset if the voltage level is too low, the ACMP using VSENSE compares the supply voltage to an internal production-calibrated bandgap reference. By adjusting the trigger level it is possible to take action before the microcontroller enters a brown-out reset or to verify that the supply voltage is within a specified range. The connections between VSENSE0 and VSENSE1 to power supplies are summarized in the table below:

Table 3.1. VSENSE Connections for all devices except EFR32xG22 and EFR32xG27

ACMP Instance	VSENSE0	VSENSE1
ACMP0	AVDD	AVDDIO0
ACMP1	DVDD	Not connected

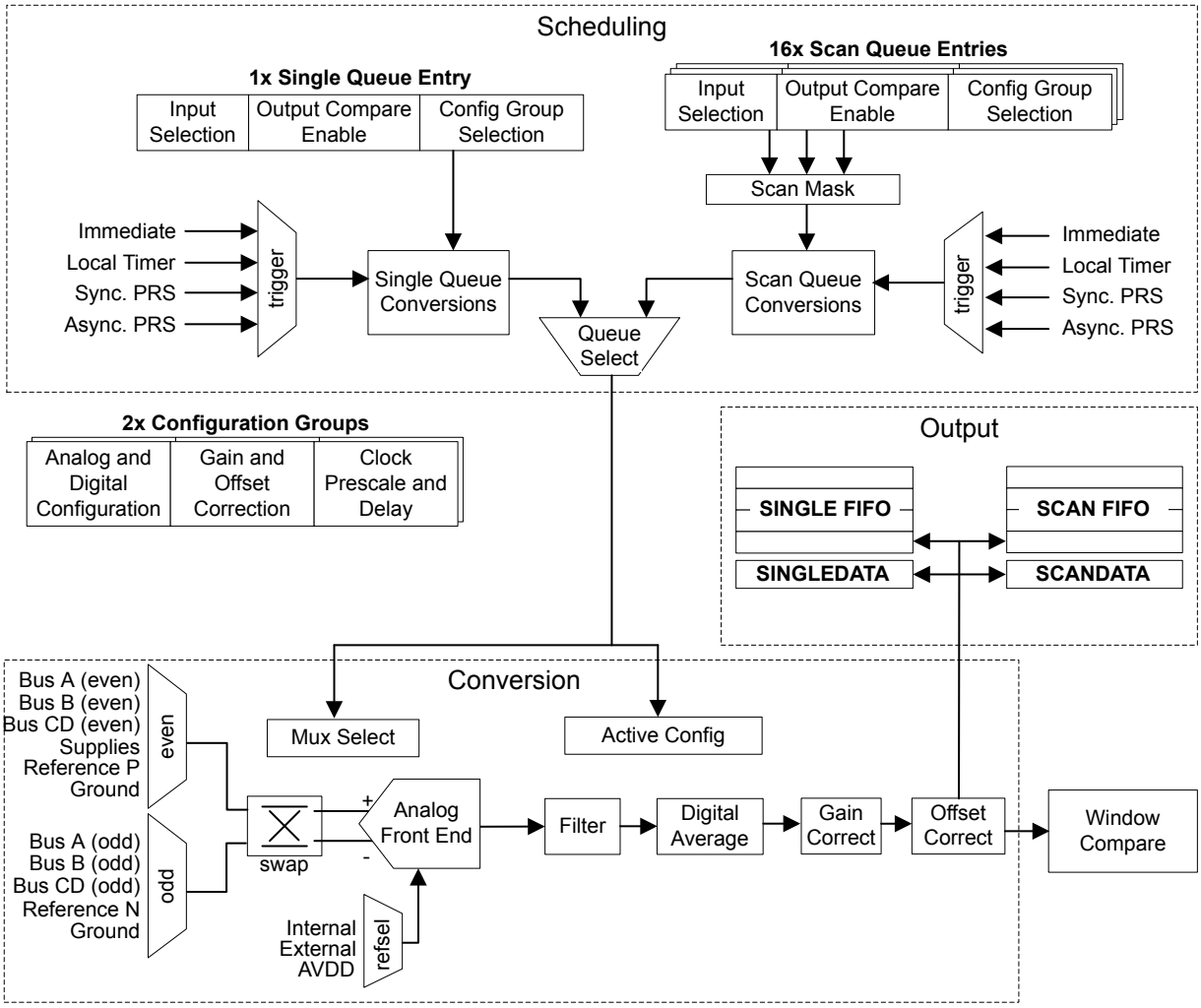
Table 3.2. VSENSE Connections for EFR32xG27

ACMP Instance	VSENSE0	VSENSE1
ACMP0	AVDD	VBAT

The ACMP also has a sample/hold circuit to reduce energy consumption. This can be enabled by selecting VSENSE01DIV4LP or VSENSE11DIV4LP for either POSSEL or NEGSEL, and the input to the comparator core will be divided by 4, as illustrated in Figure 3.1 ACMP Overview on page 4. Please note, the sample/hold feature is non-continuous so there will be an increase in response time and reduction in accuracy. Accuracy settings are set to LOW by default, which conserves power. A high accuracy setting is generally used for high-frequency changes on the inputs, such as scanning through channels or using the capacitive sense feature.

4. Supply Voltage Monitoring using IADC

The IADC is capable of routing several voltage supply rails as its input source. The IADC has an internal 1.2V bandgap reference voltage that is independent of the chip's voltage supplies and the IADC is capable of attenuating supply voltage input by a factor of 4, allowing the user to monitor full range of the supply voltage using the bandgap reference voltage. The IADC can run all the way down to EM3.



The IADC is capable of routing the following voltage rails as input source:

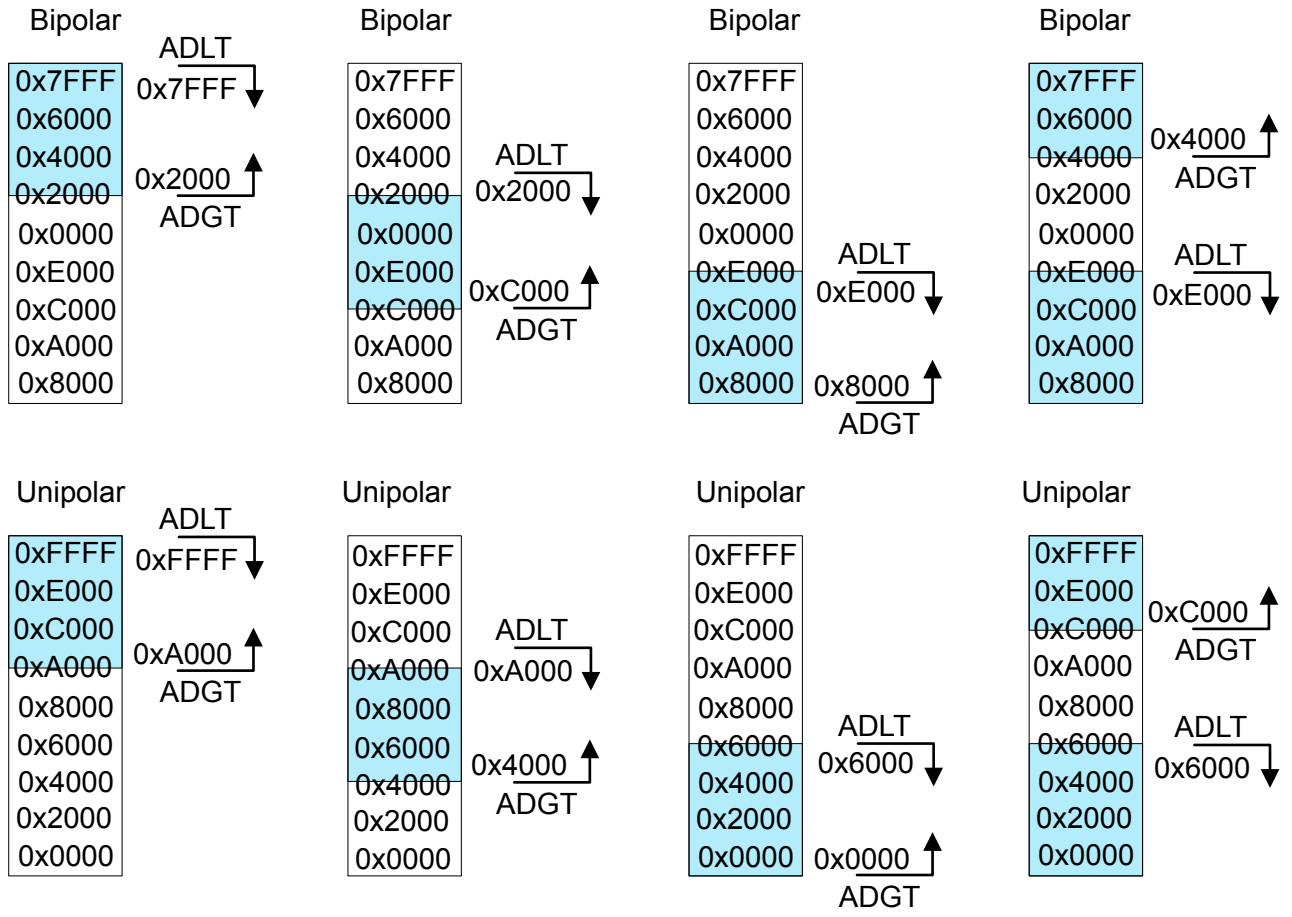
- AVDD
- IOVDD
- DVDD
- DECOUPLE

4.1 Window Comparison Unit for Supply Voltage Monitoring

The IADC window comparator feature provides an easy way to warn if the supply voltage rails reach a critical level. The IADC has an internal 1.2V bandgap reference voltage that is independent of the voltage supplies and it is capable of attenuating supply voltage input by a factor of 4, allowing the user to monitor full range of the supply voltage using the bandgap reference voltage. While the RMU automatically initiates a reset if the voltage level is too low, the IADC uses window comparator to compare the supply voltage rails to the upper and lower threshold of the window comparator. By adjusting the threshold levels it is possible to take action before the microcontroller enters a brown-out reset or to verify that the supply voltage is within a specific range.

The IADC window comparison unit has two thresholds - greater than or equal (ADGT), and less than or equal (ADLT), which are programmable through the IADC_CMPTHR register. The ADGT and ADLT thresholds always uses a 16-bit, left-justifed format, regardless of the format specified by the FIFO. The 12-bit conversion result will be compared against the upper 12 bits of the window comparator.

The triggering condition of the IADC window comparator can either be inside or outside a specified window. When ADLT is greater than or equal to ADGT, the comparator will trigger on an "inside" condition. When ADLT is less than ADGT, the comparator will trigger on an "outside" condition. For more information regarding window comparator, please refer to the IADC application note: *AN1189: Incremental Analog to Digital Converter (IADC)*.



A software example demonstrating the IADC window comparison unit as a supply voltage monitor is provided in the peripheral examples.

5. Supply Voltage Monitoring using DCDC

DCDC Overview

All devices except EFR32xG21 feature a DC-DC buck converter which requires a single external inductor and a single external capacitor. The converter takes a VREGVDD input voltage from 2.2 to 3.3V, and produces a nominal 1.8V output at the DVDD pin to power radio and MCU functions. The DC-DC converter is an efficient PFM (Pulse Frequency Modulation) architecture, delivering up to 60 mA of current. In addition, the DC-DC converter supports an unregulated bypass mode, in which the input voltage is directly shorted to the DC-DC output. An integrated supply monitor with a programmable threshold and dedicated interrupt allows softare to enable the bypass switch when the VREGVDD supply voltage is lower than 2.2V.

5.1 DCDC VREGVDD Comparator

The buck DCDC converter has a dedicated supply comparator circuit to help software determine when the VREGVDD supply is high enough to enable DC-DC regulation or when to change to bypass mode. The VREGVDD comparator threshold programming field (THRESSEL) in the EMU_VREGVDDCMPCTRL register sets the comparator threshold between 2.0 and 2.3V, and the VREGVDD comparator enable bit (VREGINCMPEN) is used to enable the supply comparator. When the VREGVDD comparator is used, the VREGVDD comparator status bit (DCDC_STATUS_VREGIN) can be read by software to determine whether VREGVDD is above or below the established threshold.

The VREGVDD comparator can also generate interrupt events when the input supply is above or below the specified threshold. The VREGINHIGHIEN and VREGINLOWIEN bits in DCDC_IEN are used to enable the above/below threshold interrupts, respectively. The VREGVDD comparator will be active and generate interrupts in EM0 and EM1 only.

The VREGVDD Comparator status is always captured and stored in RMURSTCAUSE.VREGIN on any reset event, even if the reset is not caused by VREGVDD being too low. At startup, the firmware should determine if the last reset was caused by a low VREGVDD condition by checking the following:

```
EMU_RSTCAUSE_VREGIN & (EMU_RMURSTCAUSE_DVDDBOD | EMU_RMURSTCAUSE_DVDDLEBOD)
```

If true, the part should remain in bypass mode with the DCDC disabled.

A software example demonstrating the DCDC VREGVDD Comparator is provided in the peripheral examples.

6. Software Examples

The following examples show how to monitor the supply voltage using different peripherals.

- For Supply Voltage Monitoring via ACMP example project, see: https://github.com/SiliconLabs/peripheral_examples/tree/master/series2/acmp/acmp_vmon
- For Supply Voltage Monitoring via IADC example project, see: https://github.com/SiliconLabs/peripheral_examples/tree/master/series2/iadc/iadc_vmon
- For Supply Voltage Monitoring via DCDC example project, see: https://github.com/SiliconLabs/peripheral_examples/tree/master/series2/emu/dcdc_vmon

7. Revision History

Revision 1.2

April, 2025

- Added EFR32BG22L and EFR32BG24L to 1. Device Compatibility

Revision 1.1

October, 2023

- Removed inavlid devices from 1. Device Compatibility

Revision 1.0

September, 2023

- Added EFx32xG23, EFR32xG24, EFR32xG25, EFR32xG27 and EFx32xG28 to the supported parts list.
- Added URLs to the supply voltage monitoring examples in the peripheral examples repository.
- Removed information regarding the deprecated examples.
- Updated all sections for EFx32xG23, EFR32xG24, EFR32xG25, EFR32xG27 and EFx32xG28 devices.

Revision 0.2

Feburary, 2020

- Moved Figure 2.1 Reset Tree on page 3 to 2. Reset Management Unit section.
- Moved Figure 3.1 ACMP Overview on page 4 to 3. Supply Voltage Monitoring using ACMP section.
- Added 4. Supply Voltage Monitoring using IADC, 5. Supply Voltage Monitoring using DCDC, and sections.
- Added software support for EFR32xG22.

Revision 0.1

February, 2019

- Initial revision for EFR32 Series 2.

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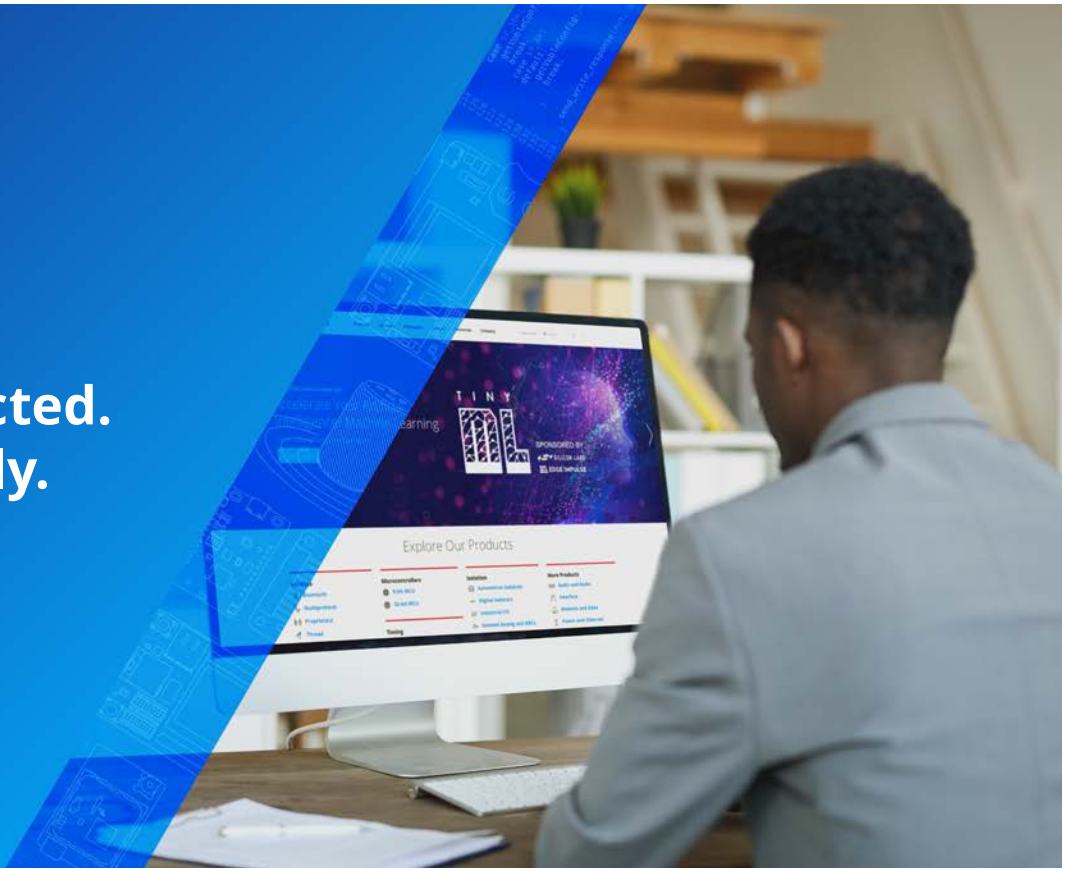

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