AN0878: Methods of Reducing Light Sensitivity in CSP Packages

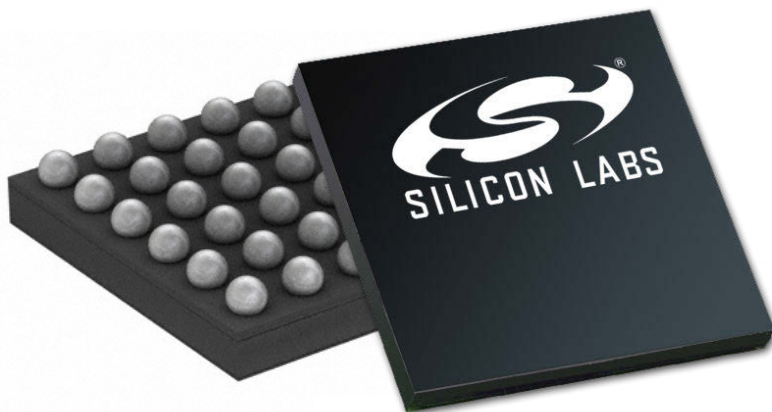
Chip Scale Packages (CSP) provide a very small footprint and cost-effective solution for many applications. Small wearable devices and small form factor Internet of Things (IoT) products often require a small form factor PCB.

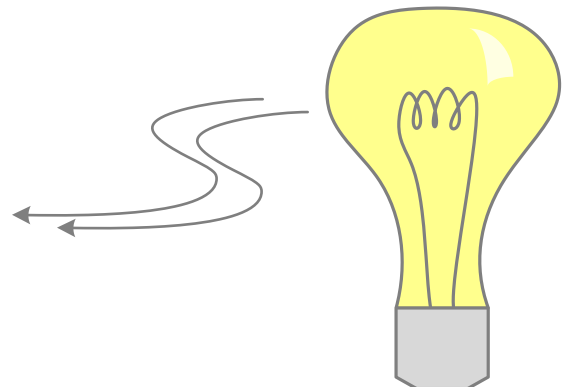
While these packages are excellent for saving space and reducing cost, they expose the IC die to light, which can cause extra current draw. This becomes especially important in low-energy applications where power consumption is a key design parameter of the system.

This document discusses the effects of light with EFM32 and EFR32 devices in CSP packages and methods to address these concerns.

KEY POINTS

- CSP packages are not fully encapsulated as other packages are, and the internal chip may be exposed to light.
- Light on an IC die can cause extra leakage current.
- Two ways of address CSP light issues are as follows:
  - Designing with a light-blocking enclosure in mind.
  - Covering the package with Glob Top epoxy.





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1. Introduction to the CSP Package

A CSP package is essentially a piece of bare silicon. In contrast, most semiconductor packages fully encapsulate the silicon in a hermetically-sealed glass-filled epoxy material. Normally, the package material is an opaque black epoxy material that blocks all light from reaching the die. The exception of course is optoelectronic semiconductor devices, which might use a clear molded material to intentionally expose the silicon to light.

Any diodes or reverse biased PN junctions on a silicon integrated circuit are subject to the photo-electric effect. When a photon strikes the semiconductor, it will create an electron-hole pair. This results in an increase in leakage current. While this effect is essential for photo-diodes, it is generally undesirable for a CMOS integrated circuit.

A CMOS inverter has two reverse biased PN junctions—the body diode of the NMOS transistor and the P-substrate to N-well junction for the PMOS transistor. Normally, the leakage of a CMOS integrated circuit may be dominated by the sub-threshold leakage. However, when exposed to light, the photocurrent will increase greatly and dominate the leakage current. Also, the additional minority carriers in the substrate and n-well may alter the behavior of the MOSFETs by shifting the threshold voltage.

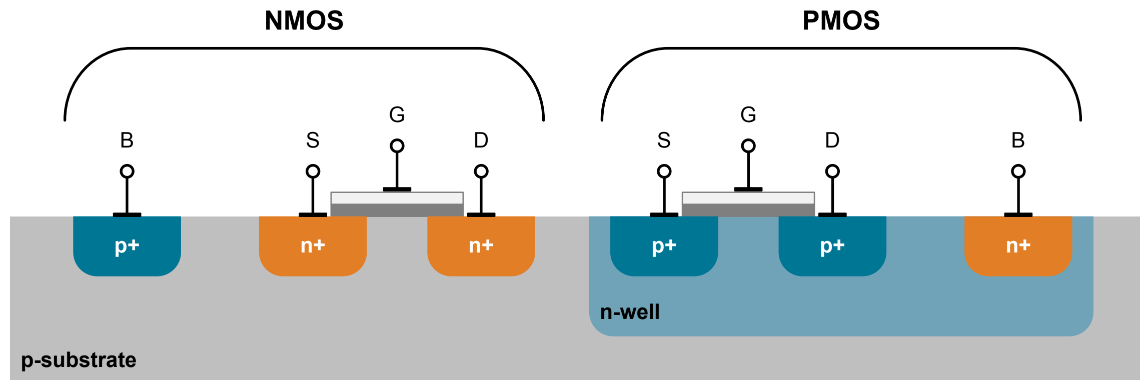

Figure 1.1. NMOS and PMOS

The effect of light on a digital CMOS IC might only result in increased leakage current. This may not be a problem for digital ICs where the leakage is not an issue. However, the increased leakage is undesirable for low-energy microcontrollers or for precision analog ICs.

2. CSP Packages and Light

Devices in CSP packaging have opaque black coating on the top of the package, covering the backside of the die. The other side has a redistribution layer and solder balls which are used to attach the die to the PCB.

Experiments with EFM32WG360F256-A-CSP81 show that when the device is exposed to bright light, the EM2 leakage current will increase to several µA and the Brown Out Detector (BOD) will reset the MCU. The ultra-low power regulator uses a low-power voltage reference which is susceptible to bright light. Setting the EMVREG bit in the EMU_CTRL register will increase the voltage regulator bias in EM2 and will prevent the BOD from resetting the device:

```
EMU->CTRL |= EMU_CTRL_EMVREG;
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In this setting, the EM2 current in full bias mode will increase to approximately 400 µA, which is not a good solution for a low-power application. The better solution is to block all light from reaching the CSP package.

3. Blocking Light from CSP Packages

3.1 Using a Light-Blocking Enclosure

There are many ways to block light from the CSP package. In most products, the bare PCB is enclosed in some type of enclosure to protect the board from dust, dirt, and mechanical damage. When using CSP packages, light blocking is a consideration that should also be designed into the enclosure. Most cell phones and products using similar technologies use CSP packages in a light-free environment.

However, light blocking is easily overlooked in many low cost products. In some cases, LEDs, proximity sensors, or opto-electronics are used in conjunction with energy friendly micro-controllers. When designing a product using opto-electronics, the enclosure must pass light to the optoelectronics and also block light where needed. When using a proximity sensor, the enclosure should pass the reflected light and block the direct path light between the LED and sensor. The enclosure design should also be designed to block light from reaching any CSP-packaged semiconductors.

The opaque backside material on top of the CSP package blocks most of the light. However, it is a thin layer of material and does not block all light. While your fingers may be opaque, a light that is bright enough will also pass through flesh.

Experiments with EFM32WG360F256-A-CSP81 using a bright halogen light show that an irradiance of 30 mW/cm^2 directly on the top of the EFM32WG360F256-A-CSP81 will cause it to reset. In comparison, bright sunlight is about 100 mW/cm^2. The device is most sensitive to a light source at a 45° angle to the left side of the die, which is the side with the voltage regulator decouple (DEC_0) ball. A light level of about 4 mW/cm^2 at this angle will cause a reset, which indicates that the edges of the die and the underside of the package are more susceptible to light than the top with the black coating.

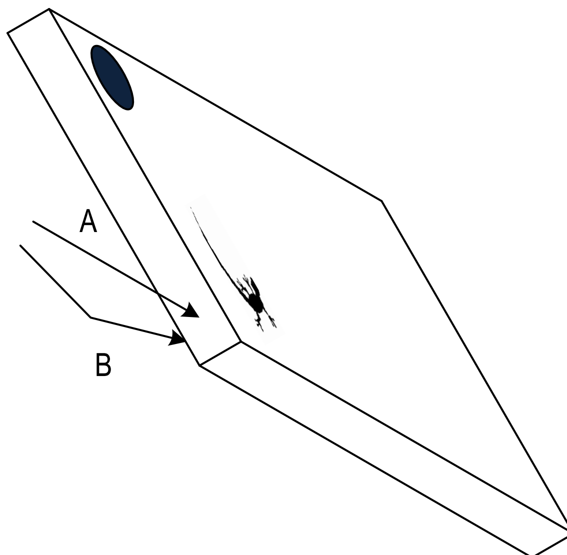

Figure 3.1. EFM32WG CSP Area of Light Sensitivity

CSP packages are also shown to be sensitive to regular 100 W incandescent light bulbs and mobile phone LED lights at a distance of 15 cm or closer.

3.2 Using Glob Top Epoxy

If it is not possible to use an enclosure to block the light, another solution is to use a semiconductor-grade Glob Top epoxy to completely cover the CSP package. This type of material is commonly used for chip-on-board assembly.

An underfill material or covering just the four sides of the package will not provide adequate light blocking from bright light. Using just an underfill material, the irradiance required to reset the EFM32 was unchanged at 4 mW/cm^2. Underfill materials are designed to provide a compliant layer underneath the package, so they have a lower viscosity and finer fill material than glob top epoxy, rendering them not as opaque. They are not necessarily designed to block light.

Covering the entire package with a glob-top material, such as Namics Chipcoat G8345-6, provides the best light blocking. When using a glob-top material, it is important to use sufficient material to completely cover the corners of the package.

Proper glob top covering for a CSP package

Improper glob top covering for a CSP package

Figure 3.2. EFM32WG Devices Covered with Glob-Top Epoxy

The board on the left has sufficient material and the corners are completely covered, forming a smooth dome over the package. The board on the right has insufficient material and the corners of the CSP are susceptible to light. The corners are clearly visible and can be felt by touch. The CSP on the right board reset at an irradiance of 30 mW/cm^2, while the CSP device on the left did not reset at an irradiance of 100 mW/cm^2.

3.3 Additional Guidelines for Matching Networks

Epoxy material in close proximity to a matching network can cause detuning. Therefore, it is best to use glob top epoxy coating only if exposure to a prominent light source is unavoidable (e.g., there is no plastic casing around the end device). An alternative solution is to account for the nearby expoxy material when designing the matching network. However, the amount of epoxy on the CSP packages between different lots of the manufactured units can vary and therefore, still have a detuning effect to a small extent.

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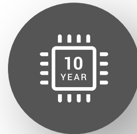

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