AN0948.2: EFR32 Series 2 Power Configurations and DC-DC

This application note provides an overview of the integrated dc-to-dc converter (DCDC) on the EFR32 Series 2 devices. In addition, it describes the available hardware configurations and programming steps for each.

Wireless SoC Series 2 with DCDC consists of the following:

- EFR32BG22
- EFR32FG22
- EFR32MG22

KEY POINTS

- DC-DC converters can improve overall system efficiency.
- EFR32 Series 2 devices integrate a dc-dc converter with flexible configuration options.
- EMLIB functions fully support the dc-dc converter and provide the optimal configuration for most cases.

1. DC-DC Buck Converter Theory

A dc-dc buck converter is a type of switching regulator that efficiently converts a high input voltage to a lower output voltage. A dc-dc converter is generally much more efficient than a low-dropout (LDO) regulator. For an LDO regulator, the input current generally equals the output current. As the difference between the input voltage and output voltage increases, the power efficiency decreases as more power is dissipated as heat. For the dc-dc converter, power output is proportional to power input based on an efficiency rating determined by the load current and switching losses. A dc-dc converter's efficiency may typically reach 90% under normal operating conditions, whereas the LDO peak efficiency is directly proportional to the output voltage over the input voltage (i.e., if the input is 3.3 V and output is 1.8 V, then the LDO efficiency is approximately 1.8 V/ 3.3 V, or 54%).

A basic block diagram of a generic dc-dc buck converter is shown below:

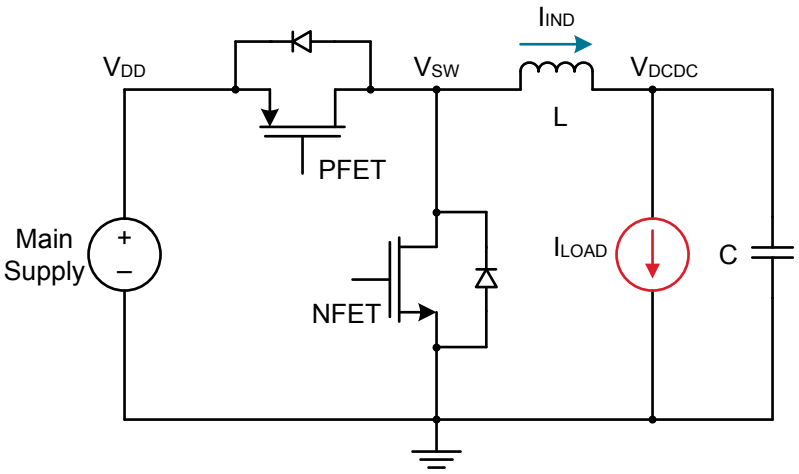


Figure 1.1. Basic DC-DC Buck Converter Block Diagram

DC-DC converters typically use one of two modulation schemes: PWM (pulse width modulation) or PFM (pulse frequency modulation). A PWM dc-dc converter modulates the on-time of the PFET switch with a constant switching frequency. This method concentrates the noise from the dc-dc converter into a single, filterable band. However, due to its constant frequency, the number of switching operations remains the same regardless of the load, and the switching current loss remains constant. A PFM dc-dc converter modulates the switching frequency, with increased switching frequency for heavy load currents and decreased switching frequency for light load currents. Due to the variable number of switching operations, the PFM method ensures high efficiency even under light load operation, as less switching results in less switching loss. Though this method is often more efficient, one drawback is that it spreads out the noise spectrum, making it more challenging to filter.

Continuous Conduction Mode (CCM)

Continuous Conduction Mode (CCM) occurs when the dc-dc converter's PFET and NFET switches are turned on complimentarily. In this mode, the power transfer occurs in two phases by, first, storing energy in the inductor, and, then, transferring the stored energy to the load.

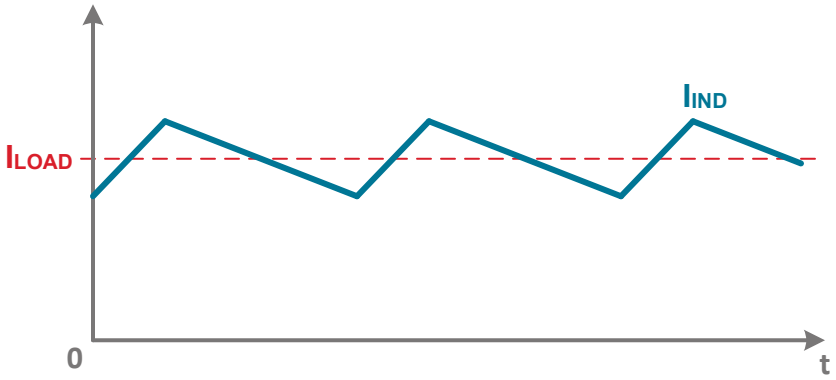


Figure 1.2. DC-DC Converter Current in Continuous Conduction Mode (CCM)

Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode (DCM) is similar to CCM except the charge stored in the inductor is allowed to be depleted. A third phase of operation occurs when the inductor current is depleted before the next switching cycle starts. DCM can occur when the peak-to-peak inductor-current ripple (I_{IND_pp}) exceeds twice the average load current (I_{LOAD}):

$$I_{IND\_pp} > 2 \times I_{LOAD}$$

$$I_{IND\_pp} = \left(1 - \frac{V_{DCDC}}{V_{DD}}\right) \times \frac{V_{DCDC}}{f_{SW} \times L}$$

Where f_{SW} is the controller's switching frequency.

To ensure that the current to the load remains positive or zero, the hardware uses a comparator on the output to turn off the NFET switch when the current to the load starts to go negative. This ensures that charge is not being pushed back into the main supply (e.g., battery), as some supplies cannot tolerate this condition.

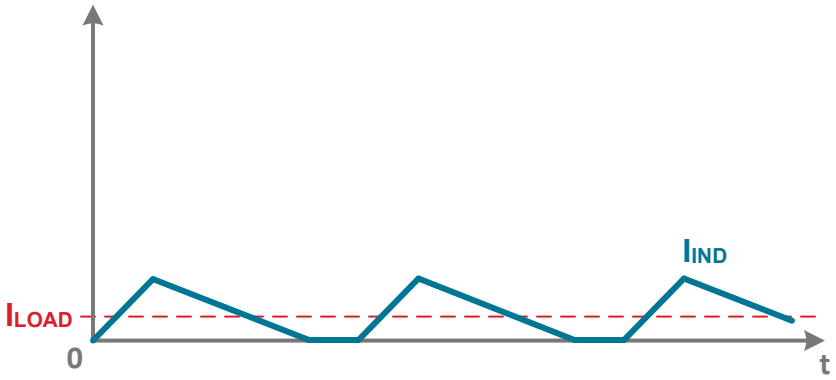


Figure 1.3. DC-DC Converter Current in Discontinuous Conduction Mode (DCM)

2. DC-DC Converter Module Overview

The EFR32 Series 2 devices feature a dc-dc buck converter which requires a single external inductor and a single external capacitor. The input supply is the VREGVDD pin, and the dc-dc converter will produce a nominal 1.8 V output at the DVDD pin to power radio and MCU functions. The dc-dc converter is an efficient PFM (Pulse Frequency Modulation) architecture, delivering up to 60 mA of current. In addition, the dc-dc converter supports an unregulated bypass mode, in which the input voltage is directly shorted to the dc-dc output. An integrated programmable supply monitor and dedicated interrupt allows software to enable the bypass switch when the VREGVDD supply voltage is below the minimum allowable voltage for the output current load.

The input supply VREGVDD has a maximum range between 1.8 and 3.8 V, but is limited by application parameters, including transient current load, operating junction temperature, and the lifetime average current load.

Refer to the device datasheet for more details on the input supply voltage range.

2.1 PFM Buck Converter

The Pulse Frequency Modulation (PFM) dc-dc design in EFR32 Series 2 devices features an entirely new architecture from the dc-dc in EFM32 and EFR32 Series 1 devices. The dc-dc buck converter utilizes a fixed-peak-current, comparator based feedback regulation method. The PFM switching cycle consists of three phases with two periods in which the dc-dc converter's PFET and NFET switches are turned on complimentary to one another and a third period in which both the PFET and NFET switches are turned off to ensure that the current to the load remains positive or zero.

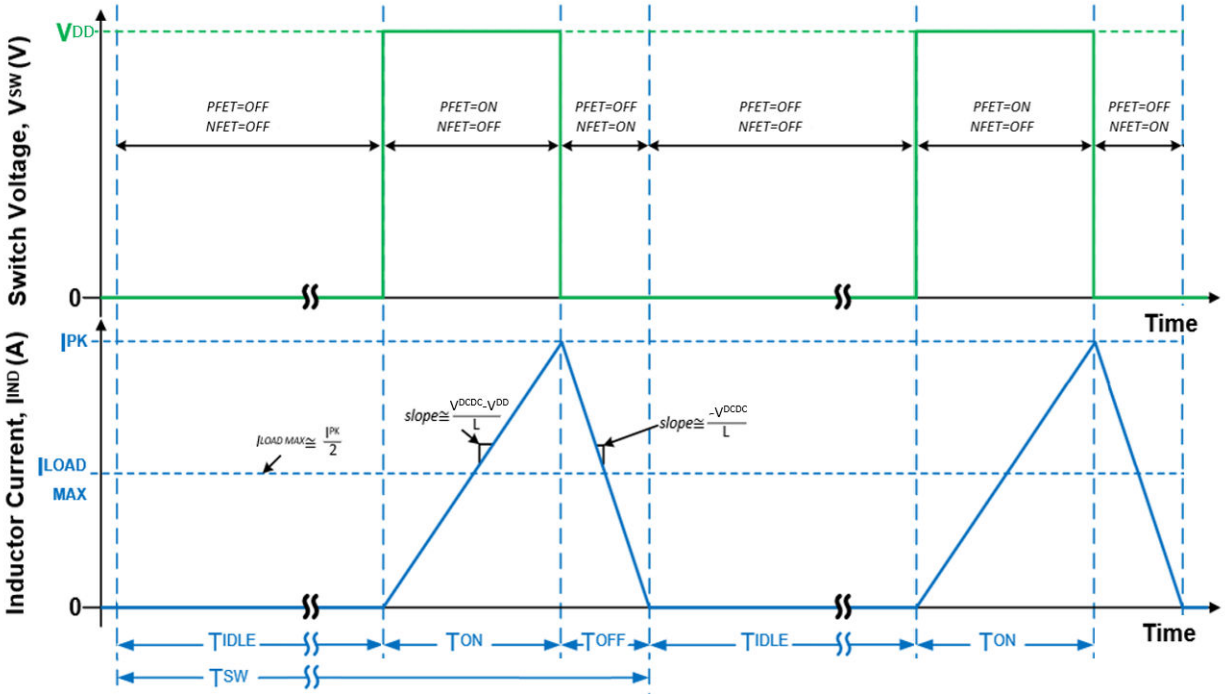


Figure 2.1. DC-DC Converter Switch Voltage and Inductor Current during switching cycle

A switching cycle is initiated when the dc-dc voltage comparator detects that the output voltage is less than the reference voltage. The PFET switch is closed and begins to conduct, charging the inductor current until it reaches the fixed IPK current limit. When the peak current detector triggers, the PFET is switched off, and the NFET is switched on, which discharges the inductor current to zero. When the zero-crossing detector triggers, it turns off the NFET, and the cycle repeats again, waiting for the voltage comparator trigger.

2.2 Bypass Mode and VREGVDD Comparator

In bypass mode, the VREGVDD input voltage is directly shorted to the dc-dc converter output through an internal switch. Bypass mode is enabled automatically during a power-on-reset. Bypass mode can also be enabled and disabled through software, using the DCDC_CTRL_MODE field. When set to BYPASS, the bypass switch is enabled and dc-dc regulation will be disabled. Consult the data-sheet for the bypass switch impedance specification.

The EFR32xG22 includes a supply comparator circuit to help software determine when the VREGVDD supply is high enough to enable dc-dc regulation or when to change to bypass mode. Before enabling the dc-dc , the supply comparator should be configured and enabled. The THRESSEL field in the EMU_VREGVDDCMPCTRL register sets the comparator threshold between 2.0 and 2.3 V, and the VREGINCMPEN bit is used to enable the supply comparator. When the VREGVDD comparator is used, DCDC_STATUS_VREGIN can be read by software to determine whether VREGVDD is above or below the established threshold. If this is currently low, indicating that VREGIN below threshold, the dc-dc should not be enabled and software should wait until the comparator indicates VREGIN above threshold.

The VREGVDD comparator can also generate interrupt events when the input supply is above or below the specified threshold. The VREGINHIGHIEN and VREGINLOWIEN bits in DCDC_IEN are used to enable the above / below threshold interrupts, respectively. The VREGVDD comparator will be active and generate interrupts in EM0 and EM1 only.

The VREGVDD Comparator status is always captured and stored in RMURSTCAUSE.VREGIN on any reset event, even if the reset is not caused by VREGVDD being too low. At startup, the firmware should determine if the last reset was caused by a low VREGVDD condition by checking the following:

EMU_RSTCAUSE_VREGIN & (EMU_RMURSTCAUSE_DVDDBOD | EMU_RMURSTCAUSE_DVDDLEBOD)

If the above logic is true, device software should keep the device in bypass mode with the DCDC disabled.

2.3 DC-DC Startup

Out of power-on-reset (POR), the dc-dc converter defaults to bypass mode and the dc-dc block is disabled. Before enabling the dc-dc , software should first configure and enable the VREGVDD comparator. Once the thresholds for the VREGVDD comparator have been configured and the comparator enabled, the DCDC_STATUS_VREGIN bit should be checked to ensure that the input supply is above the threshold. When the input supply is sufficient, the dc-dc may be configured and enabled. The following steps outline this procedure:

1. Set VREGVDD comparator threshold with EMU_VREGVDDCMPCTRL_THRESSEL
2. Enable VREGVDD comparator with EMU_VREGVDDCMPCTRL_VREGINCMPEN
3. Check DCDC_STATUS_VREGIN:
   - If low, VREGIN is above the programmed threshold and it is safe to enter dc-dc mode
   - If high, VREGIN is below the programmed threshold and firmware should remain in bypass mode
4. Enable the dc-dc module with DCDC_EN_EN = 1
5. Configure the IPKVAL and DRVSPEED settings in DCDC_EM01CTRL0 and DCDC_EM23CTRL0.
6. Enable any required interrupts via DCDC_IEN.
7. Start the dc-dc by setting DCDC_CTRL_MODE to DCDCREGULATION.

The dc-dc will enter a warmup phase for approximately 100 us, then disable the bypass switch and begin using the dc-dc core to regulate the output voltage. The DCDC_IF_RUNNINGIF interrupt flag will indicate when the switch from bypass to dc-dc is complete, however this does not indicate that the output is regulated. Until the output capacitor discharges due to normal current draw from the system, the voltage may be higher than 1.8 V. The DCDC_IF_REGULATIONIF interrupt flag will indicate when the dc-dc has reached regulation and is providing the desired output voltage.

If the VREGINLOWIF interrupt occurs, software should immediately switch back to bypass mode by clearing DCDC_CTRL_MODE to BYPASS.

2.4 Recommended Configuration Settings

Certain dc-dc parameters are adjustable for fine-tuning of performance, but the majority of applications will not need to use any other than the recommended settings. All datasheet parameters are specified using the recommended settings detailed in this section. The configuration settings must be set before dc-dc regulation is started, and must not be changed while the dc-dc is active.

The DCDC_EM01CTRL0 and DCDC_EM23CTRL0 registers each have an IPKVAL field to adjust the maximum peak / load current, and a DRVSPEED field to adjust the driver speed. DCDC_EM01CTRL0 sets the configuration for EM0 and EM1 operation while DCDC_EM23CTRL0 sets the configuration for EM2 and EM3 operation. The DCDC_CTRL_IPKTMAXCTRL field adjusts the maximum time for peak current detection, which impacts the voltage ripple at the dc-dc output. The recommended settings are shown in Table 2.1 DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings on page 6.

Table 2.1. DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings

Bit Field	Recommended Setting
EM01CTRL0_IPKVAL	9 (LOAD60MA)
EM01CTRL0_DRVSPEED	1 (DEFAULT_SETTING)
EM23CTRL0_IPKVAL	3 (LOAD5MA)
EM23CTRL0_DRVSPEED	3 (BEST_EFFICIENCY)
DCDC_CTRL_IPKTMAXCTRL	4 (TMAX_1P19US)

The DCDC_CTRL_DCMONLYEN field can be used to select between DCM and CCM mode. The default setting (1) is to use DCM mode, and should not be changed for most applications.

2.5 EM4 Entry

The dc-dc is available in all energy modes except for EM4. If the system wants to enter EM4, the dc-dc converter must first be turned off and switched over to bypass mode. The system will not enter EM4 if the dc-dc is active. If an attempt is made to go into EM4 with dc-dc active, it will be blocked, and the DCDC_IF_EM4ERR flag will be set.

3. Power Configurations

In order to provide the lowest power solutions, the EFR32xG22 comes with a dc-dc module to power internal circuits. The EFR32xG22 may be operated with or without the DC-DC. When used, the dc-dc requires an external inductor and capacitor (refer to the data sheet for recommended values).

The EFR32xG22 has multiple power supply rails: a dc-dc regulator input (VREGVDD), IO Supply (IOVDD), Analog (AVDD), RF Analog Supply (RFVDD), RF Power Amplifier Supply (PAVDD), Digital LDO and flash (DVDD), and Low Voltage Digital Supply (DECOUPLE). Additional detail for each configuration and option is given in the following sections.

Due to on-chip circuitry (e.g., diodes), some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD >= DVDD

  Note: In systems not using the dc-dc converter, VREGVDD must be shorted to DVDD external to the device.

- PAVDD >= RFVDD
- DVDD >= DECOUPLE
- AVDD, IOVDD: No dependency with other supply pins.

Additionally, there are other system-level considerations when assigning power supplies.

- The usable range for analog signals connected to GPIO (such as IADC inputs) will be limited to the lower of AVDD and IOVDD.
- The RESETn pin has an internal pullup to the DVDD supply. If RESETn is driven by external circuitry above DVDD, additional current may flow into the pin due to this pullup.

3.1 "Startup" or "Unconfigured" Configuration

Upon power-on reset (POR), the system is configured in a safe Startup Configuration that supports all of the available Power Configurations. The Startup Configuration is shown in the simplified diagram below.

In the Startup configuration the dc-dc converter's Bypass switch is ON (i.e., the VREGVDD pin is shorted internally to the DVDD pin).

After power on, firmware can elect to turn on the dc-dc if the external hardware configuration supports it.

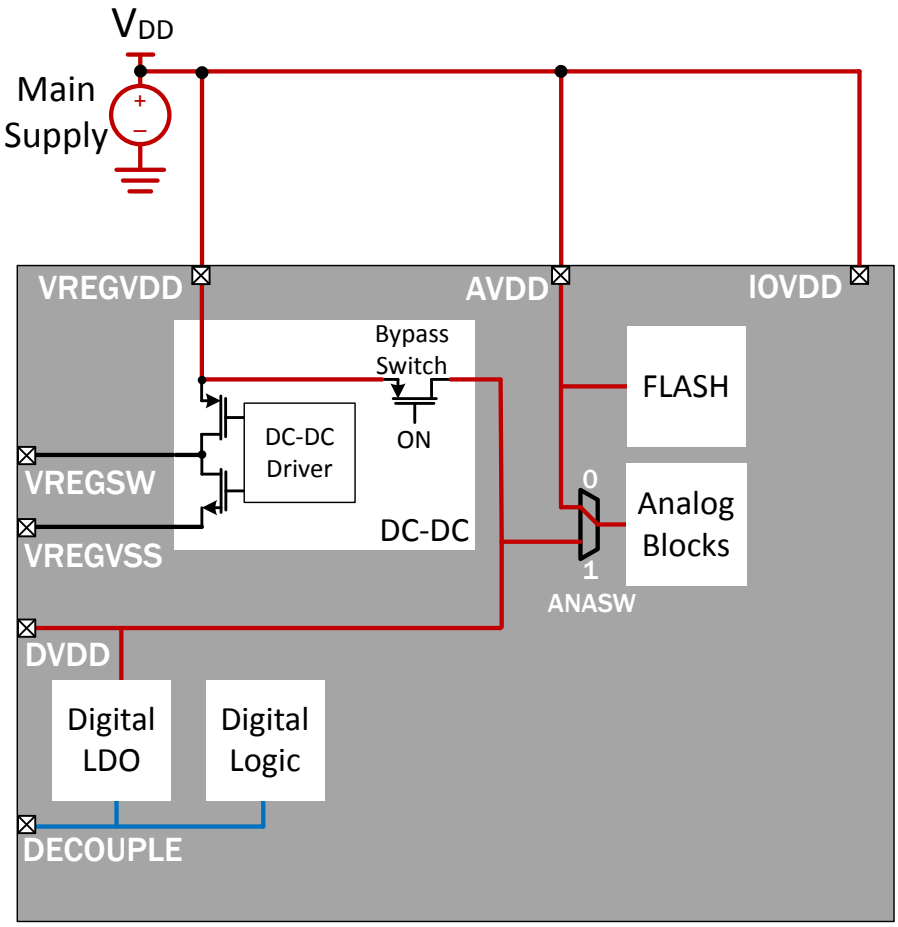


Figure 3.1. Startup Power Configuration

3.2 Power Configuration 1: No DC-DC

In Power Configuration 1, the dc-dc converter is unused, and all power is supplied by external sources. The DVDD pin must be shorted to VREGVDD.

IOVDD, AVDD, RFVDD and PAVDD may be supplied by the same supply as VREGIN and DVDD (as shown in Figure 3.2 DC-DC Off Power Configuration on page 9), or they may be powered from a separate source.

VREGSW must be left disconnected in this configuration.

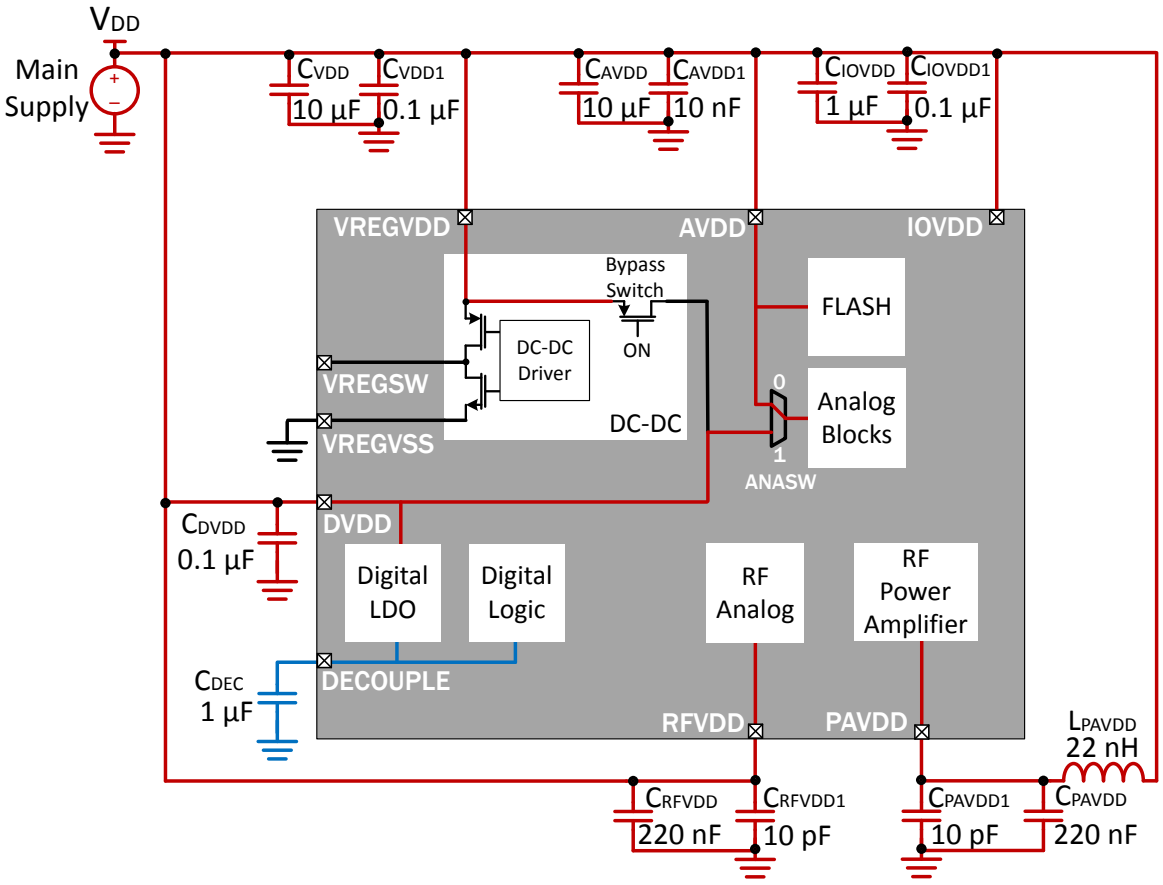


Figure 3.2. DC-DC Off Power Configuration

3.3 Power Configuration 2: DC-DC

For the lowest power applications, the dc-dc converter can be used to power the rest of the supplies on the device. When the dc-dc converter is used to regulate the voltage at DVDD, the maximum supply voltage may be limited by the operating temperature and/or the average lifetime load conditions. Refer to the device datasheet for additional details.

In Power Configuration 2, the dc-dc Output (V_{DCDC}) is connected to DVDD and optionally, to all the other supplies on the chip. In the configuration shown in Figure 3.3 DC-DC Power Configuration on page 10, the AVDD and IOVDD supplies are connected to the main supply to support higher voltage external interfaces.

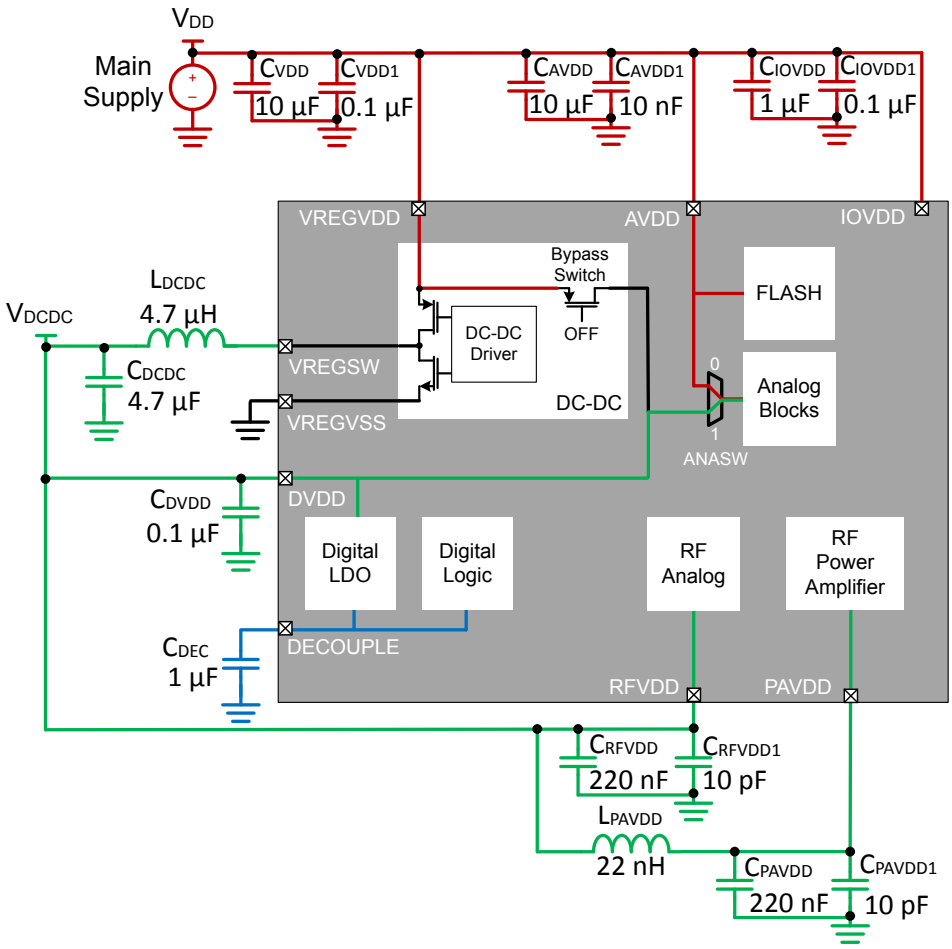


Figure 3.3. DC-DC Power Configuration

As the Main Supply voltage approaches the dc-dc output voltage, it eventually reaches a point where becomes inefficient (or impossible) for the dc-dc module to regulate V_{DCDC}. At this point, firmware can enable bypass mode, which effectively disables the dc-dc and shorts the Main Supply voltage directly to the dc-dc output. If and when sufficient voltage margin on the Main Supply returns, the system can be switched back into dc-dc regulation mode.

4. DC-DC Programming Using EMLIB

To simplify use of the dc-dc converter, EMLIB contains functions which will properly configure the dc-dc for efficient operation. It is strongly recommended to take advantage of these functions. These EMLIB functions will also avoid or workaround any errata issues affecting the dc-dc converter. More information on the EMU EMLIB library can be found using the [**Gecko HAL and Driver API Reference Guide**] tile in Simplicity Studio.

4.1 To Initialize the DC-DC Converter to Regulation or Bypass Mode

1. Declare a structure of type `EMU_DCDCInit_TypeDef`.

```
typedef struct
{
        EMU_DcdcMode_TypeDef            mode;
        EMU_VreginCmpThreshold_TypeDef  cmpThreshold;
        EMU_DcdcTonMaxTimeout_TypeDef   tonMax;
        bool                            dcmOnlyEn;
        EMU_DcdcDriveSpeed_TypeDef      driveSpeedEM01;
        EMU_DcdcDriveSpeed_TypeDef      driveSpeedEM23;
        EMU_DcdcPeakCurrent_TypeDef     peakCurrentEM01;
        EMU_DcdcPeakCurrent_TypeDef     peakCurrentEM23;
} EMU_DCDCInit_TypeDef;
```

Description of parameters:

- `mode`: DC-DC mode of operation. May be set to
  - `emuDcdcMode_Bypass` — Enables Bypass mode (i.e., the dc-dc is not switching and the VREGVDD pin is shorted internally to the DVDD pin)
  - `emuDcdcMode_Regulation` — Requests dc-dc regulation and disables the bypass switch
- `cmpThreshold`: VREGIN comparator threshold determines the voltage at which the regulator input will indicate through status bits or interrupt if configured that themay be set to
  - `emuVreginCmpThreshold_2v0`— regulator input threshold voltage set to 2.0V
  - `emuVreginCmpThreshold_2v1`— regulator input threshold voltage set to 2.1V
  - `emuVreginCmpThreshold_2v2`— regulator input threshold voltage set to 2.2V
  - `emuVreginCmpThreshold_2v3`— regulator input threshold voltage set to 2.3V
- `tonMax`: Specifies the timeout duration when attempting to hit the programmed peak current. The TMAX interrupt flag will be set if the timeout was hit before reaching peak current. May be set to:
  - `emuDcdcTonMaxTimeout_Off`— timeout disabled
  - `emuDcdcTonMaxTimeout_0P35us`— 0.35µs timeout
  - `emuDcdcTonMaxTimeout_0P63us`— 0.63µs timeout
  - `emuDcdcTonMaxTimeout_0P91us`— 0.91µs timeout
  - `emuDcdcTonMaxTimeout_1P19us`— 1.19µs timeout
  - `emuDcdcTonMaxTimeout_1P47us`— 1.47µs timeout
  - `emuDcdcTonMaxTimeout_1P75us`— 1.75µs timeout
  - `emuDcdcTonMaxTimeout_2P03us`— 2.03µs timeout
- `dcmOnlyEn`: boolean setting for DCM only mode enable defined as follows:
  - false — DUALMODE — support a higher current load at a lower input voltage by regulating in CCM mode
  - true — DCMONLYEN — DCM only mode used for normal regulator operation; this mode is the default mode of operation
- `driveSpeedEM01` and `driveSpeedEM23`: Drive speed settings used in EM01 and EM23 respectively. Configures drive speed for tradeoff between EMI and regulator efficiency. This parameter is defined as follows:
  - `emuDcdcDriveSpeed_BestEmi` — Lowest efficiency, lowest EMI; small decrease in efficiency from default setting
  - `emuDcdcDriveSpeed_Default` — Default efficiency, acceptable EMI level
  - `emuDcdcDriveSpeed_Intermediate` — Small increase in efficiency from the default setting
  - `emuDcdcDriveSpeed_BestEfficiency` — Highest efficiency, highest EMI; small increase in efficiency from INTERMEDIATE
- `peakCurrentEM01` and `peakCurrentEM23`: Peak current setting used to configure the required peak and load current when operating in EM01 and EM23 respectively. This parameter is defined as follows:
  - `emuDcdcPeakCurrent_Load36mA` — Load current 36mA in EM01, 5mA in EM23; peak current 90mA
  - `emuDcdcPeakCurrent_Load40mA` — Load current 40mA; peak current 100mA (setting valid for `peakCurrentEM01` only)
  - `emuDcdcPeakCurrent_Load44mA` — Load current 44mA; peak current 110mA (setting valid for `peakCurrentEM01` only)
  - `emuDcdcPeakCurrent_Load48mA` — Load current 48mA; peak current 120mA (setting valid for `peakCurrentEM01` only)
  - `emuDcdcPeakCurrent_Load52mA` — Load current 52mA; peak current 130mA (setting valid for `peakCurrentEM01` only)
  - `emuDcdcPeakCurrent_Load56mA` — Load current 56mA; peak current 140mA (setting valid for `peakCurrentEM01` only)
  - `emuDcdcPeakCurrent_Load60mA` — Load current 60mA in EM01, 10mA in EM23; peak current 150mA

2. Call `EMU_DCDCInit()` passing the `EMU_DCDCInit_TypeDef` structure, created in step 1, as an argument. Alternately, there is a default `EMU_DCDCInit_TypeDef` structure provided that can be used. See ● Initialization Programming Examples on page 13 section below for examples using the default structure. At the completion of this function call, the dc-dc should be in regulation. This function does the following:
   - Enables the DCDC clock tree in order to modify the DCDC module registers.
   - Enables the DCDC module.
   - Unlocks access to all DCDC registers.
   - Configures the VREGIN comparator threshold based on the `cmpThreshold` value.
   - Configures the CTRL register using values from `tonMax` and `dcmOnlyEn`.
   - Loads the EM01CTRL0 and EM23CTRL0 registers with the respective drive speed and peak current settings.
   - Configures the DCDC regulator mode of operation. If enabling the DCDC regulator,
   - Relocks DCDC registers if previously locked.

Initialization Programming Examples

Initialization example using the dc-dc default configuration:

```
EMU_DCDCInit_TypeDef dcdcInit = EMU_DCDCINIT_DEFAULT;
EMU_DCDCInit(&dcdcInit);
```

4.2 Turn DC-DC Converter OFF

To power off the dc-dc and turn on the internal Bypass switch, call the `EMU_DCDCPowerOff()` function. This function should be used when VREGIN drops below the low threshold or when entering EM4.

4.3 To Enter EM2, EM3, or EM4 Low Energy Modes

To enter the low energy modes, call `EMU_EnterEM2()`, `EMU_EnterEM3()`, or `EMU_EnterEM4()`. The `EMU_EnterEM4()` function switches the dc-dc converter to bypass mode before entering EM4.

5. DC-DC Configuration Reference

Note: EMLIB contains functions which properly configure the dc-dc for an efficient operation. It is strongly recommended to take advantage of these functions. These EMLIB functions also avoid or work around any errata issues affecting this block.

5.1 DC-DC Module Register Locks

The dc-dc module has several locks that can be used to prevent accidental changes to the EMU and dc-dc configuration registers. Note that these locks are unlocked by default and are not used by any of the EMLIB dc-dc configuration functions.

1. EMU_LOCK — All non-dc-dc , EMU, registers may be unlocked by writing 0xADE8 to LOCKKEY or locked by writing any other value to LOCKKEY.
2. DCDC_LOCK — All dc-dc registers may be unlocked by writing 0xABCD to LOCKKEY or locked by writing any other value to LOCKKEY.

6. DC-DC Components Selection Guide

6.1 DC-DC Output Capacitor

The Samsung CL10B475KQ8NQNC 4.7µF capacitor was used for all of the dc-dc validation and characterization testing for EFR32 Series 2 devices. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.

The output capacitor should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 °C – +85°C (standard temperature range devices) or -55 °C – +125°C (extended temperature range devices).

The system designer should pay particular attention to the characteristics of the output capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages) can experience a dramatic reduction in capacitance value as the temperature or bias voltage increases. A change pushing the dc-dc output capacitance outside the datasheet specified limits may result in output instability.

Table 6.1. Recommended DC-DC Output Capacitor

Manufacturer	Part Number	Value (µF)	Voltage Rating (V)	Dielectric	Operating Temperature (°C)	Package
Samsung	CL10B475KQ8NQNC	4.7±10%	6.3	X7R	-55 to +125	0603/1608

6.2 DC-DC Inductor

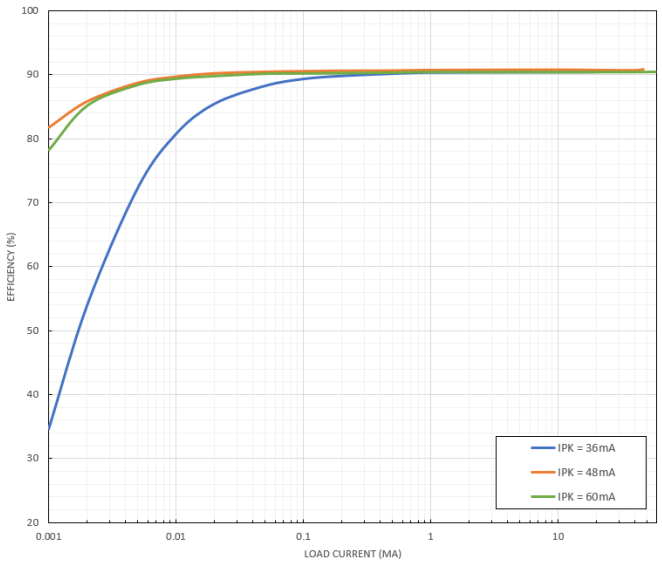
The Samsung CIG22H2R2MNE inductor was used for all of the dc-dc validation and characterization testing.

The following inductors listed may be suitable as well, but only EM0 efficiency was measured.

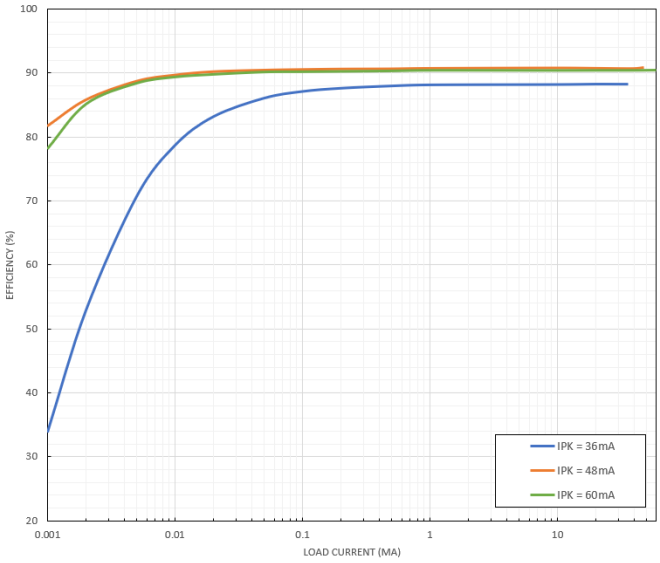
Table 6.2. DC-DC Inductors

Manufacturer	Part Number	Value (µH)	$I_{saturation}$ (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Samsung	CIG22H2R2MNE	2.2±20%	1800	0.12±20%	-40 to +125	1008/2520
TDK	MLZ2012N2R2LT000	2.2±20%	170	0.12±20%	-55 to +125	0805/2012
Murata	LQM18PZ2R2MDH	2.2±20%	250	0.47±20%	-55 to +125	0603/1608
Murata	LQM18PZ2R2MFH	2.2±20%	300	0.47±30%	-55 to +125	0603/1608
Murata	LQM18PZ2R2MCH	2.2±20%	200	0.48±30%	-55 to +125	0603/1608
Murata	LQM18PN2R2MGH	2.2±20%	250	0.25±20%	-40 to +85	0603/1608
TDK	MLZ1608A2R2WT000	2.2±20%	130	0.25±20%	-55 to +125	0603/1608
Murata	LQM18PH2R2MFRL	2.2±20%	150	0.37±20%	-55 to +150	0603/1608
TDK	MLZ1005M2R2WT000	2.2±20%	60	0.55±20%	-55 to +125	0402/1005
Samsung	CIG22L2R2MNE	2.2±20%	Unspecified	0.08±20%	-40 to +125	1008/2520
Samsung	CIGT201610LH2R2MNE	2.2±20%	2300	0.14±20%	-40 to +125	0806/2016
TDK	KLZ2012MHR2R2HTD25	2.2±20%	400	0.20±20%	-55 to +150	0805/2012

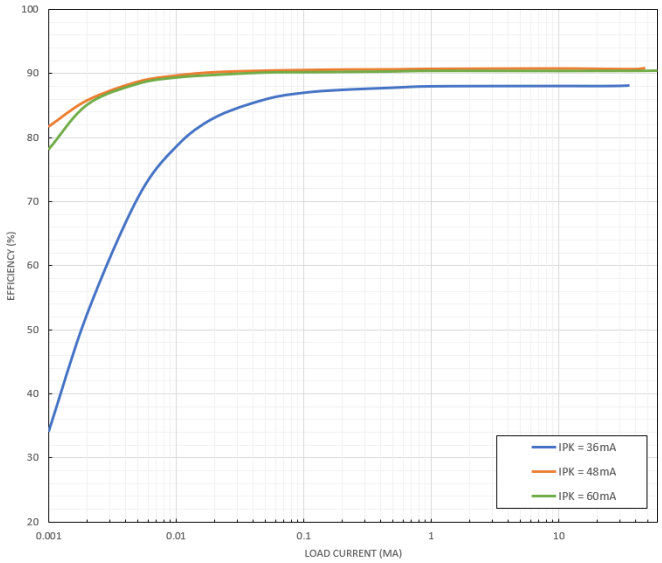
Samsung CIG22H2R2MNE



TDK MLZ2012N2R2LT000



Murata LQM18PZ2R2MDH



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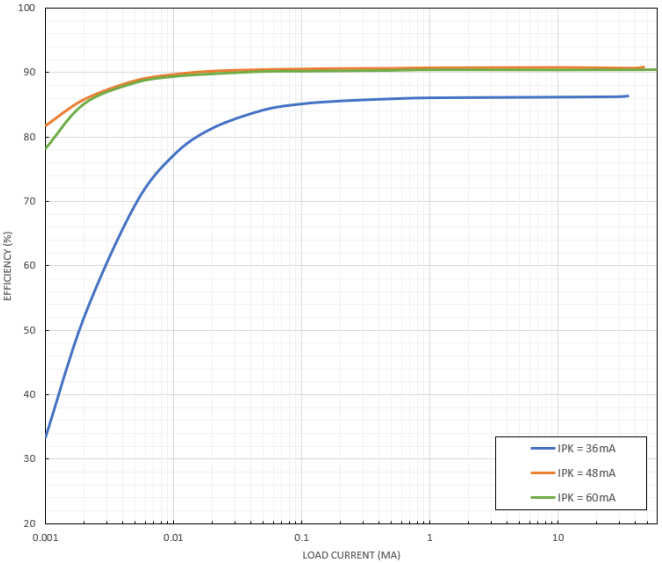

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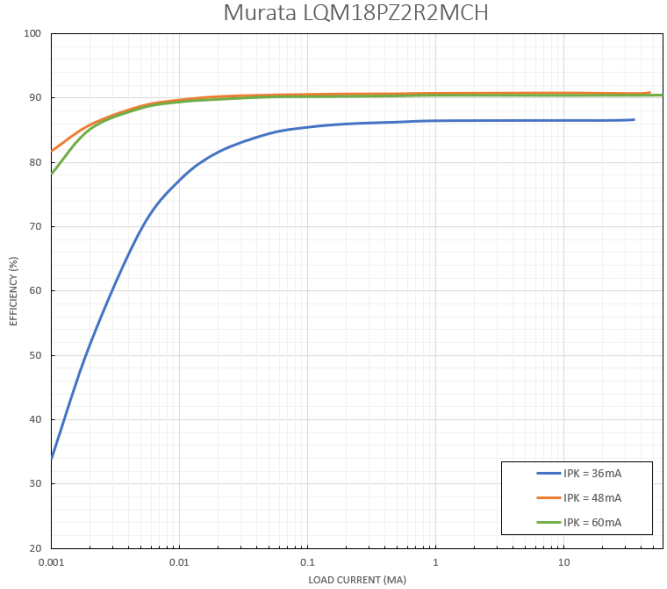

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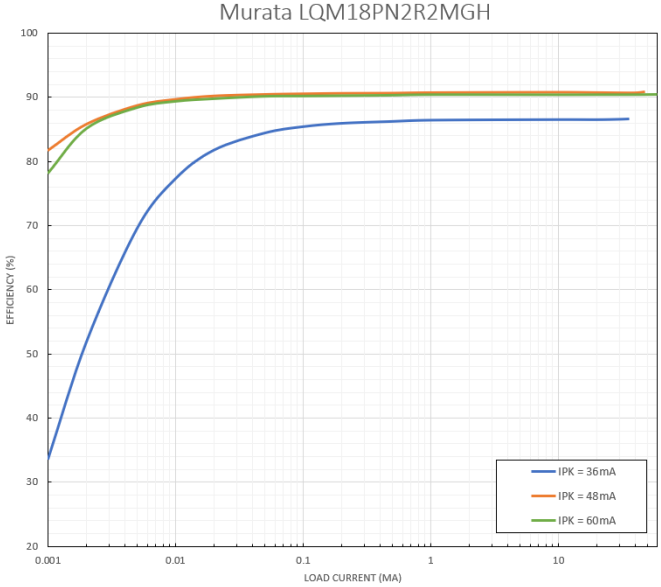


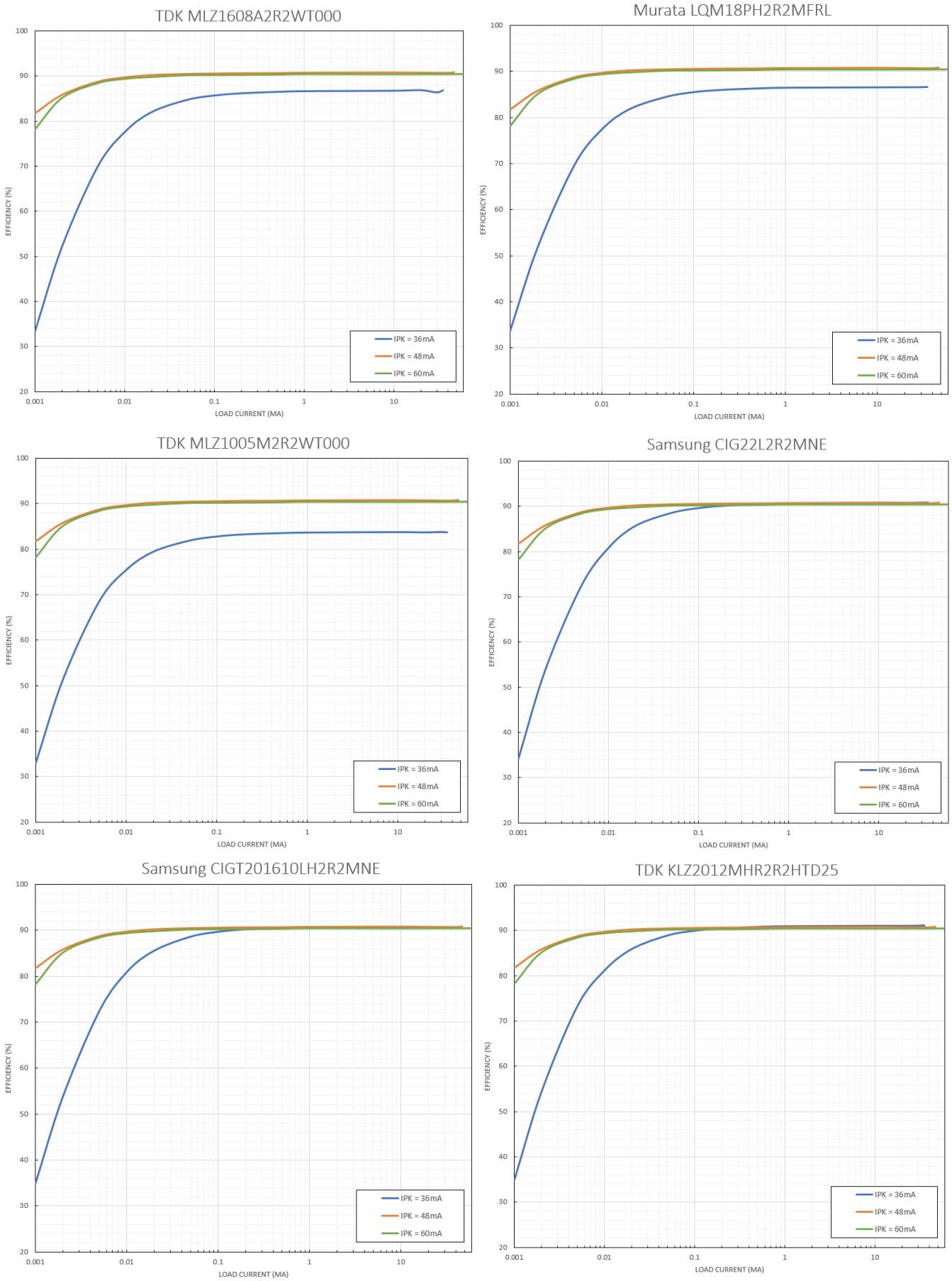


Figure 6.1. Inductor Efficiency Curves, L_{DCDC}=2.2 µH, VREGVDD=3.3 V, V_{DCDC}=1.8 V

7. DC-DC Layout Considerations

Because the dc-dc converter is a high-frequency, high-current module, some special layout considerations are required for optimal operation:

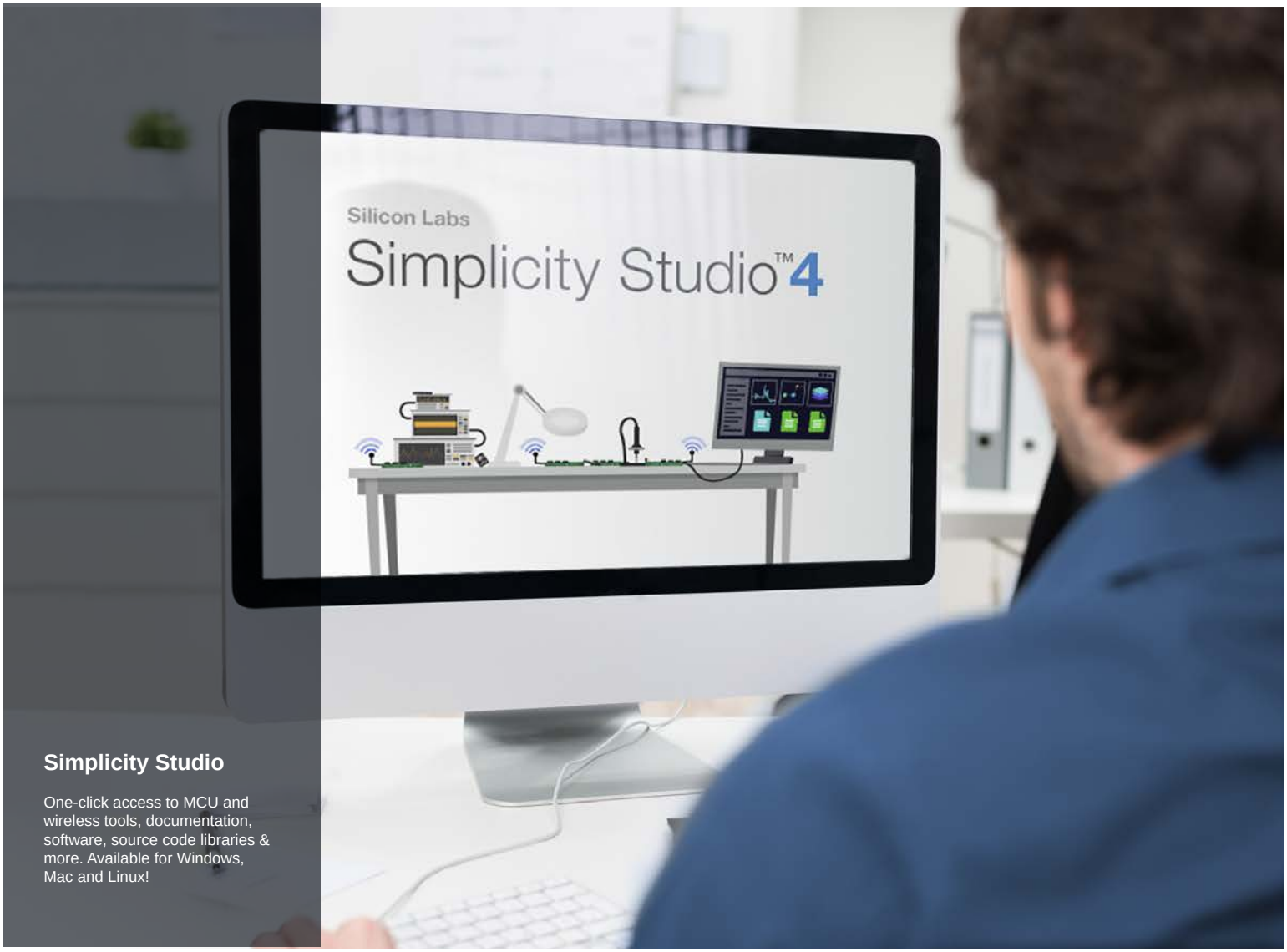
- The following connections should be made on the PCB using minimum trace length and resistance
- - Between the VREGSW pin and the L_{DCDC} inductor
  - Between the L_{DCDC} inductor and the C_{DCDC} capacitor
  - Between the C_{DCDC} capacitor and the DVDD pin
  - Between the Main Supply and the VREGVDD pin
  - Between the VREGVSS pin and ground
- The L_{DCDC} inductor should be placed far away from any noise-sensitive circuitry (e.g., a radio antenna). The inductor should ideally be on the opposite side of the PCB, so that there is a solid ground plane shielding the noisy inductor from the sensitive circuitry.
- For more detailed radio-specific layout guidelines, see *AN928.2: EFR32 Series 2 Layout Design Guide* .

8. Revision History

Revision 0.1

April, 2020

- Initial Revision



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