AN0948.2: EFM32 and EFR32 Series 2 DC-to-DC Converter

This application note provides an overview of the integrated DC-to-DC converter (DC-DC) on EFM32 and EFR32 Series 2 devices. Hardware configuration and software initialization are discussed along with external component recommendations and PCB layout guidance.

Series 2 devices with a Buck DC-DC:

- EFR32BG22
- EFR32FG22
- EFR32MG22
- EFM32PG22
- EFR32FG23
- EFM32PG23
- EFR32ZG23
- EFR32BG24
- EFR32MG24
- EFR32FG25
- EFR32BG27
- EFR32MG27

Series 2 devices with a Boost DC-DC:

- EFR32BG27
- EFR32MG27

KEY POINTS

- A DC-to-DC converter can improve overall system energy efficiency.
- EFM32 and EFR32 Series 2 devices integrate a DC-to-DC converter with flexible configuration options.
- Emlib functions fully support the DC-to-DC converter and provide the optimal configuration for the majority of use cases.

1. DC-DC Overview

A DC-to-DC converter (DC-DC) is a type of switching regulator that efficiently converts a source of direct current (DC) from one voltage level to another. A DC-DC is generally much more efficient than a low-dropout (LDO) regulator. For an LDO regulator, the input current generally equals the output current. As the difference between the input voltage and output voltage increases, the power efficiency decreases as more power is dissipated as heat. For a DC-DC, power output is proportional to power input based on an efficiency rating determined by the load current and switching losses. A DC-DC's efficiency may typically reach 90% under normal operating conditions, whereas LDO regulator peak efficiency is directly proportional to the output voltage over the input voltage (i.e., if the input is 3.3 V and the output is 1.8 V, then the LDO efficiency is approximately 1.8 V/3.3 V or 54%).

DC-DCs typically use one of two modulation schemes: PWM (pulse width modulation) or PFM (pulse frequency modulation). A PWM DC-DC modulates the on-time of the PFET switch with a constant switching frequency. This method concentrates the noise from the DC-DC into a single, filterable band. However, due to its constant frequency, the number of switching operations remains the same regardless of the load, and the switching current loss remains constant. A PFM DC-DC modulates the switching frequency, with increased switching frequency for heavy load currents and decreased switching frequency for light load currents. Due to the variable number of switching operations, the PFM method ensures high efficiency even under light load operation, as less switching results in less switching loss. Though this method is often more efficient, one drawback is that it spreads out the noise spectrum, making it more challenging to filter.

2. Buck DC-DC Module Overview

The EFM32 and EFR32 Series 2 devices feature a DC-to-DC buck converter (buck DC-DC) which requires a single external inductor and a single external capacitor. The input supply is the VREGVDD pin, and the buck DC-DC produces a nominal 1.8 V output at the V_{DCDC} node to power radio and MCU functions. The buck DC-DC is an efficient pulse frequency modulation architecture, delivering up to 120 mA of current (see the device data sheet for specific limits). In addition, the buck DC-DC supports an unregulated bypass mode in which the input voltage is directly shorted to the buck DC-DC output. An integrated programmable supply monitor and dedicated interrupt allows software to enable the bypass switch when the VREGVDD supply voltage is below the minimum allowable voltage for the output current load.

The input supply VREGVDD has a maximum range between 1.8 and 3.8 V but is limited by application parameters, including transient current load, operating junction temperature, and the lifetime average current load.

Refer to the device data sheet for more details on the input supply voltage range.

2.1 Basic Buck DC-DC

A buck DC-DC is a type of switching regulator that efficiently converts a high input voltage to a lower output voltage. A basic block diagram of a generic buck DC-DC is shown below:

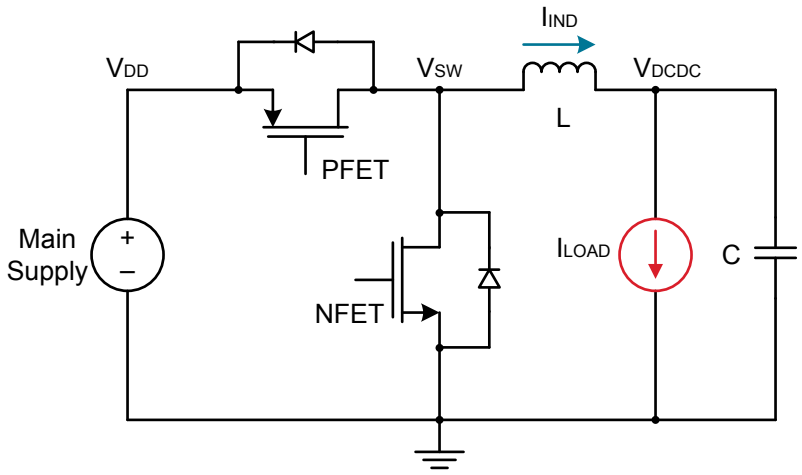


Figure 2.1. Basic Buck DC-DC Block Diagram

2.2 PFM Buck DC-DC

The pulse frequency modulation (PFM) buck DC-DC design in EFM32 and EFR32 Series 2 devices features an entirely new architecture relative to the buck DC-DC on EFM32 and EFR32 Series 1 devices. This new design utilizes a fixed peak-current, comparator-based feedback regulation method. The PFM switching cycle consists of three phases with two periods in which the buck DC-DC's PFET and NFET switches are turned on in a complimentary fashion and a third period in which both the PFET and NFET switches are turned off to ensure that the current to the load remains positive or zero.

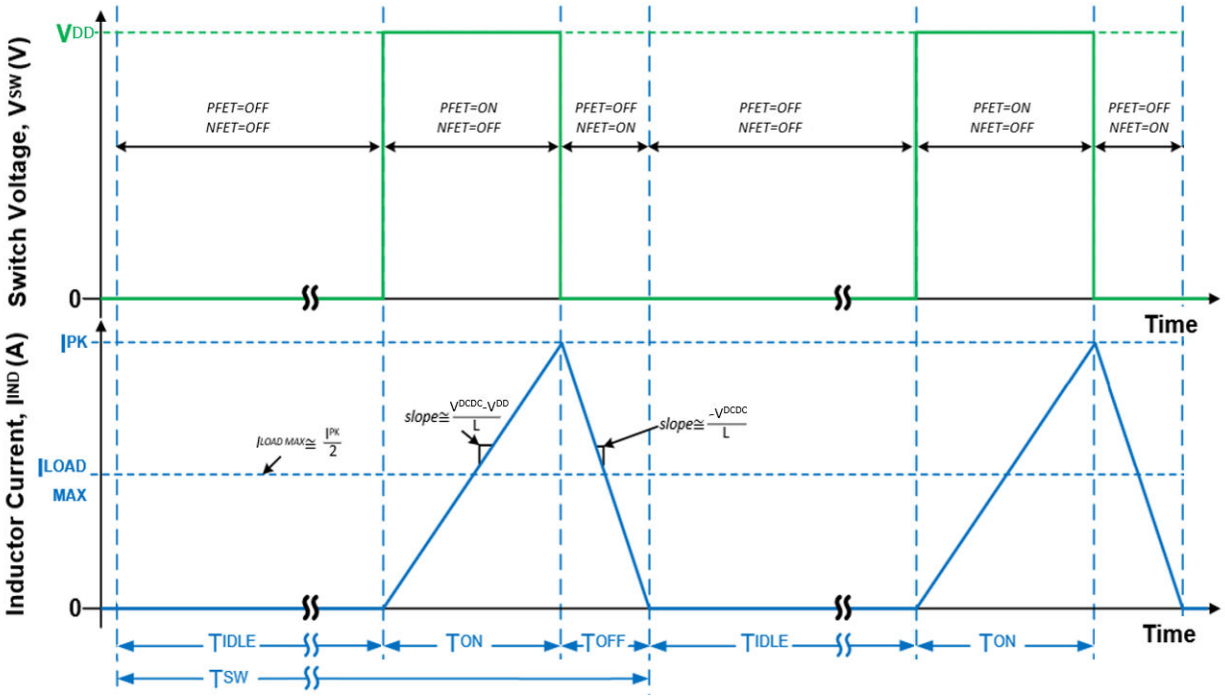


Figure 2.2. Buck DC-DC Switch Voltage and Inductor Current during Switching Cycle

A switching cycle is initiated when the buck DC-DC voltage comparator detects that the output voltage is less than the reference voltage. The PFET switch is closed and begins to conduct, charging the inductor until it reaches the fixed IPK current limit. When the peak current detector triggers, the PFET is switched off, and the NFET is switched on, which discharges the inductor current to zero. When the zero-crossing detector triggers, it turns off the NFET, and the cycle repeats again, waiting for the voltage comparator trigger.

2.3 Bypass Mode and VREGVDD Comparator

In bypass mode, the VREGVDD input voltage is directly shorted to the DC-DC output through an internal switch. Bypass mode is enabled automatically during a power-on-reset. Bypass mode can also be enabled and disabled through software, using the DCDC_CTRL_MODE field. When set to BYPASS, the bypass switch is enabled and DC-to-DC regulation is disabled. Consult the datasheet for the bypass switch impedance specification.

The buck DC-DC includes a supply comparator circuit to help software determine when the VREGVDD supply is high enough to enable DC-to-DC regulation or when to change to bypass mode. Before enabling the buck DC-DC, the supply comparator must be configured and enabled. The THRESSEL field in the EMU_VREGVDDCMPCTRL register sets the comparator threshold between 2.0 and 2.3 V, and the VREGINCMPEN bit enables the supply comparator. When the comparator is used, DCDC_STATUS_VREGIN can be read by software to determine whether VREGVDD is above or below the established threshold. When this bit is high, indicating that VREGIN is below threshold, the buck DC-DC should not be enabled and software should wait until the comparator indicates that VREGIN is above threshold.

The VREGVDD comparator can also generate interrupt requests when the input supply is above or below the specified threshold. The VREGINHIGH and VREGINLOW bits in the DCDC_IEN register enable the above and below threshold interrupt requests, respectively. The VREGVDD comparator is active and can request interrupts in EM0 and EM1 only.

Upon any reset event, the status of VREGVDD comparator status is always captured and stored in the VREGIN bit of the EMU_RSTCAUSE register, even if the reset is not caused by VREGVDD being too low. At startup, software should determine if a low VREGVDD condition caused the last reset using logic similar to this:

```
if (RMU_ResetCauseGet() == (EMU_RSTCAUSE_VREGIN & (EMU_RSTCAUSE_DVDDBOD | EMU_RSTCAUSE_DVDDLEBOD)))
  handleBrownOutDetectionReset();
else
  initializeNormally();
```

If the reset condition above is true, software should keep the device in bypass mode with the buck DC-DC disabled.

2.4 Buck DC-DC Startup

Out of power-on-reset (POR), the bypass switch is enabled, and the DC-DC is disabled. Before enabling the buck DC-DC, software should first configure and enable the VREGVDD comparator. Once the thresholds for the VREGVDD comparator have been configured and the comparator enabled, the VREGIN bit of the DCDC_STATUS register should be checked to ensure that the input supply is above the threshold, at which point the buck DC-DC can be configured and enabled. The following steps outline this procedure:

1. Set the VREGVDD comparator threshold in EMU_VREGVDDCMPCTRL.
2. Enable the VREGVDD comparator by setting the VREGINCMPEN bit in the EMU_VREGVDDCMPCTRL register.
3. Check the VREGVDD threshold comparator status by reading the VREGIN bit in the DCDC_STATUS register:
   - If low, VREGIN is above the programmed threshold, and it is safe to enable the buck DC-DC.
   - If high, VREGIN is below the programmed threshold and software should leave the bypass switch enabled (MODE = 0 in the DCDC_CTRL register).
4. For EFx32xG22, enable the DC-DC module by writing 1 to the EN bit in the DCDC_EN register.
5. Configure the IPKVAL and DRVSPEED settings in the DCDC_EM01CTRL0 and the DCDC_EM23CTRL0 registers.
6. Enable any required interrupts via the DCDC_IEN register.
7. Enable the buck DC-DC by writing 1 to the MODE bit in the DCDC_CTRL register.

When enabled, the buck DC-DC enters a warmup phase for approximately 100 µs, then disables the bypass switch and begins using the buck DC-DC core to regulate the output voltage. The RUNNING bit in the DCDC_IF register indicates when the switch from bypass mode to DC-to-DC regulation is complete, however this does not yet indicate that the output is regulated. Until the output load capacitor discharges due to normal current draw from the system, the voltage may be higher than 1.8 V. The REGULATION bit in the DCDC_IF register indicates when the buck DC-DC has reached regulation and is providing the desired output voltage.

If the VREGINLOW interrupt occurs, software should immediately return to bypass mode by writing 0 to the MODE bit in the DCDC_CTRL register.

2.5 Recommended Configuration Settings

Certain DC-DC parameters can be adjusted to fine-tune performance, but the majority of applications do not need to use anything other than the default/recommended settings. All data sheet parameters are specified using the recommended settings detailed in this section. These settings must be in place before the DC-DC is enabled and must not be changed while the DC-DC is active.

The DCDC_EM01CTRL0 and DCDC_EM23CTRL0 registers each have an IPKVAL field to adjust the peak/maximum load current and a DRVSPEED field to adjust the driver speed. DCDC_EM01CTRL0 configures these parameters for operation in EM0 and EM1 while the DCDC_EM23CTRL0 settings apply to EM2 and EM3. The IPKTMAXCTRL field in the DCDC_CTRL register sets the timeout interval for peak current detection, which impacts the voltage ripple at the buck DC-DC output. The recommended settings are shown in Table 2.1 DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for Buck DC-DC on page 6.

Table 2.1. DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for Buck DC-DC

Bit Field	Recommended Setting
EM01CTRL0_IPKVAL	9 (LOAD60MA)
EM01CTRL0_DRVSPEED	1 (DEFAULT_SETTING)
EM23CTRL0_IPKVAL	3 (LOAD5MA)
EM23CTRL0_DRVSPEED	1 (DEFAULT_SETTING)
DCDC_CTRL_IPKTMAXCTRL	4 (TMAX_1P19US) for EFx32xG22 and EFR32xG27 16 (TMAX_1P19US) for all other devices

On supported devices, the DCMONLYEN bit in the DCDC_CTRL register selects between DCM and CCM mode. The default setting (DCMONLYEN = 1) is to use DCM mode, and should not be changed for most applications.

2.6 EM4 Entry

The buck DC-DC is available in all energy modes except EM4. To enter EM4, the buck DC-DC must be switched to bypass mode. The system will not enter EM4 if the buck DC-DC is active; any attempt to do so will be blocked, and the EM4ERR bit in the DCDC_IF register will be set.

3. Boost DC-DC Module Overview

Select EFM32 and EFR32 Series 2 devices feature a DC-to-DC boost converter (boost DC-DC) which requires a single external inductor and a single external capacitor. The input supply to the boost startup circuitry is the VBAT pin, the boost DC-DC will produce a nominal 1.8 V output at the DVDD pin to power radio and MCU functions. The boost startup circuit uses an internal charge pump to temporarily power the boost DC-DC output, until the output voltage is at a valid level to support powering on the regular boost converter circuitry. Once the startup circuitry has reached a valid level, the regular boost DC-DC is enabled and the startup circuit is disabled. The boost DC-DC is an efficient pulse frequency modulation architecture, delivering up to 25 mA output current (see the device data sheet for specific limits). In addition, the boost DC-DC can be completely shut down using a dedicated input pin, saving system power during storage and shipping.

The boost DC-DC configuration has an input range of 0.8 to 1.65 V and up to 25 mA output current, enabling operation directly from single-cell Silver Oxide, Alkaline, and other low-voltage battery chemistries.

Refer to the device data sheet for more details on the input supply voltage range.

3.1 Basic Boost DC-DC

A boost DC-DC is a type of switching regulator that efficiently converts a low input voltage to a higher output voltage while lowering the current consumption. A basic block diagram of a generic boost DC-DC is shown below:

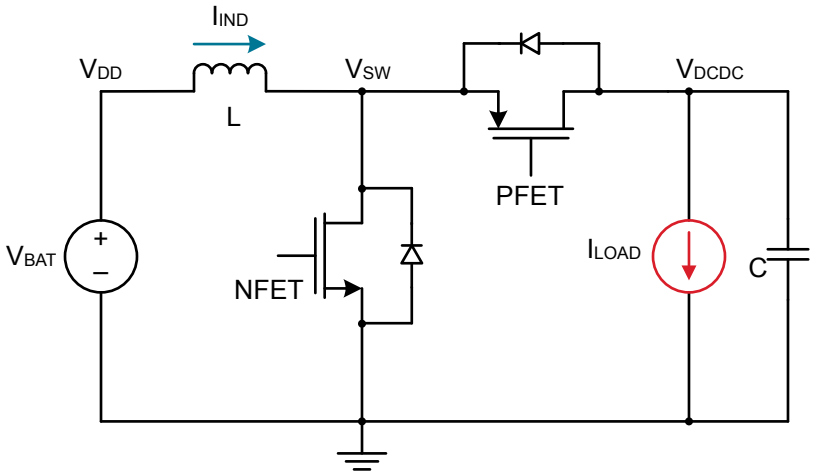


Figure 3.1. Basic Boost DC-DC Block Diagram

3.2 PFM Boost DC-DC

The pulse frequency modulation (PFM) boost DC-DC design in EFM32 and EFR32 Series 2 utilizes a fixed peak-current, comparator-based feedback regulation method. The PFM switching cycle consists of three phases with two periods in which the boost DC-DC's PFET and NFET switches are turned on in a complimentary fashion and a third period in which both the PFET and NFET switches are turned off to ensure that the current to the load remains positive or zero.

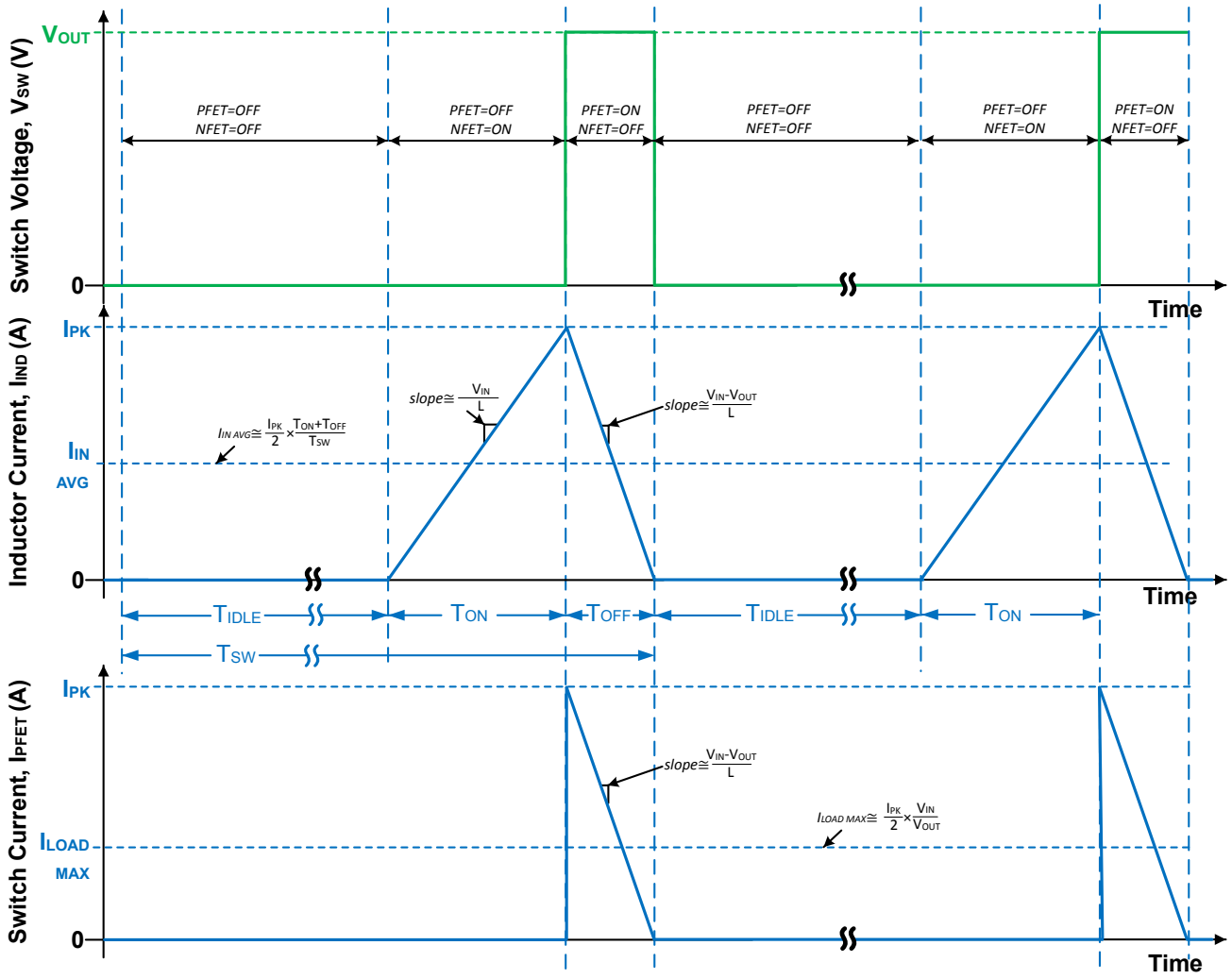


Figure 3.2. Boost DC-DC Switch Voltage and Inductor Current during Switching Cycle

A switching cycle is initiated when the boost DC-DC voltage comparator detects that the output voltage(V_{DVDD}) is less than the reference voltage. The NFET switch is closed and begins to conduct, charging the inductor until it reaches the fixed I_{PK} current limit. When the peak current detector triggers, the PFET is switched on, and the NFET is switched off, which discharges the inductor current to zero. When the zero-crossing detector triggers, it turns off the PFET, and the cycle repeats again, waiting for the voltage comparator trigger.

3.3 BOOST_EN and Shutdown

A dedicated BOOST_EN pin on the device allows the boost DC-DC to be activated and deactivated from an external signal. By default, the boost DC-DC will start up whenever the BOOST_EN pin is logic high, and then the logic level at BOOST_EN will be ignored after the converter output reaches its target voltage and the device powers on.

If the application should disable the boost DC-DC when a low level is seen at the BOOST_EN input, firmware on the device must clear the EMU_BOOSTCTRL.BOOSTENCTRL bit to 0. If EMU_BOOSTCTRL.BOOSTENCTRL is 0 and the BOOST_EN input is low, the boost DC-DC will go into a very low power shutdown state. A subsequent logic high level on BOOST_EN can re-enable the boost DC-DC.

After startup, if the BOOST_EN input is not needed to disable the boost DC-DC, it can be used as a general purpose digital input by reading the logic level of the EMU_STATUS.BOOSTENPIN bit. The BOOST_EN pin may also be used as a falling-edge or rising-edge interrupt source to the EMU interrupt vector. Separate interrupt flags for rising and falling edges are available in the EMU_IF register as BOOSTNEGEDGE and BOOSTPOSEDGE. The EMU_IEN register allows code to enable these interrupt sources.

Table 3.1. Boost DC-DC Behavior with respect to BOOST_EN Pin and EMU_BOOSTCTRL.BOOSTENCTRL Bit

BOOSTENCTRL Bit	Description
0	A logic high on BOOST_EN pin will power up the device.
	A logic low on BOOST_EN pin will power down the boost DC-DC.
1	A logic high on BOOST_EN pin will power up the device.
	A logic low on BOOST_EN pin will be ignored (i.e., the boost DC-DC will continue to run).

3.4 Boost DC-DC Startup

Out of power-on-reset (POR), the boost DC-DC is disabled. To start up the boost DC-DC converter, the BOOST_EN pin must be held high for ~50 msec to allow the boost DC-DC to go through the necessary startup stages.

Note:

- The maximum output load during the boost DC-DC startup (i.e., before the output is in regulation) is limited to ~3 mA, so some consideration needs to be paid to the loads on the boost DC-DC output.
- The boost DC-DC output may momentarily be high around 1.8V - 2.2 V during startup. External circuitry connected to the boost DC-DC output needs to be able to momentarily tolerate 2.2 V.

The boost DC-DC has some dedicated registers as listed below that can be used for configuring it.

- EMU_BOOSTCTRL
- DCDC_BSTCTRL
- DCDC_BSTEM01CTRL
- DCDC_BSTEM23CTRL
- DCDC_EM01CTRL
- DCDC_EM23CTRL

See 5.2 Configure the Boost DC-DC section for more details.

Boost DC-DC Behavior on Reset

- If a Debug/Soft reset occurs, the boost DC-DC will continue operating as configured.
- If a Hard/POR/BOD reset occurs, then the device will reset the boost DC-DC configuration registers and if the BOOST_EN input is high, the boost DC-DC may immediately attempt to restart.

3.5 Typical Use Cases

3.5.1 Use Case 1: BOOST_EN Hard Tied to VBAT

In this scenario, BOOST_EN is always held high. On a hard RESET event, the device will immediately attempt to start up again.

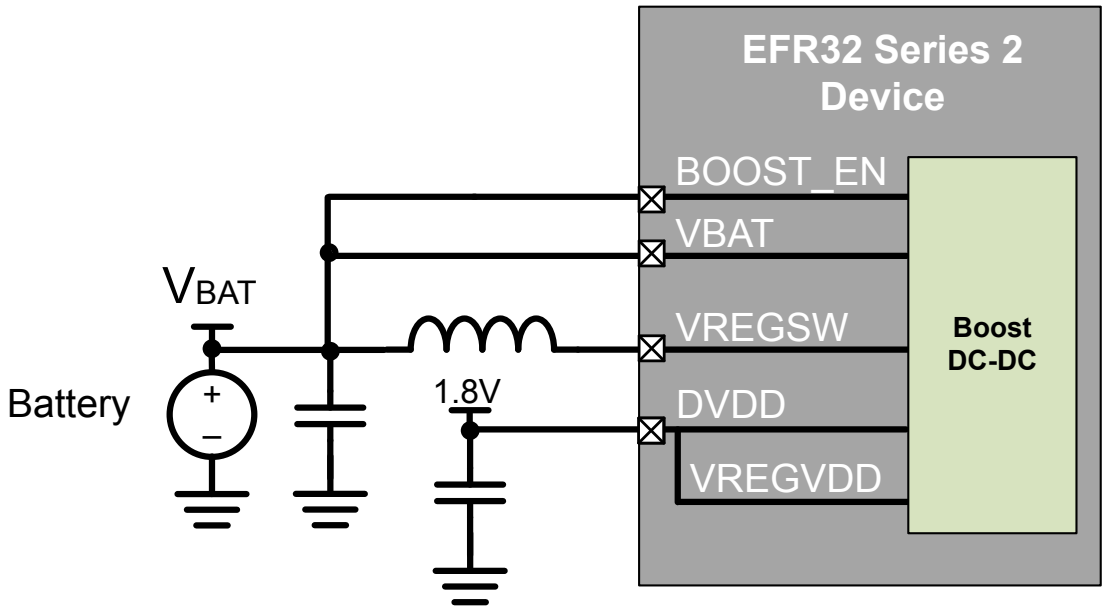


Figure 3.3. Typical Connections for Use Case 1: BOOST_EN Hard Tied to VBAT

3.5.2 Use Case 2: BOOST_EN Connected to VBAT through Momentary Pushbutton

In this scenario, BOOST_EN is pulled high momentarily on a button press. An external pull down (> 1 MΩ) is required on BOOST_EN input for this use case. A 0.1 µF external capacitor may be needed on BOOST_EN input to handle button chatter/debounce.

By default the EMU resets the EMU_BOOSTCTRL.BOOSTENCTRL bit to 1. However, after startup, firmware can clear EMU_BOOSTCTRL.BOOSTENCTRL to 0 to allow the boost converter to shut down if BOOST_EN goes to logic low level. If the boost DC-DC is disabled by firmware or a hard RESET event occurs, the button would need to be pressed again to restart the device .

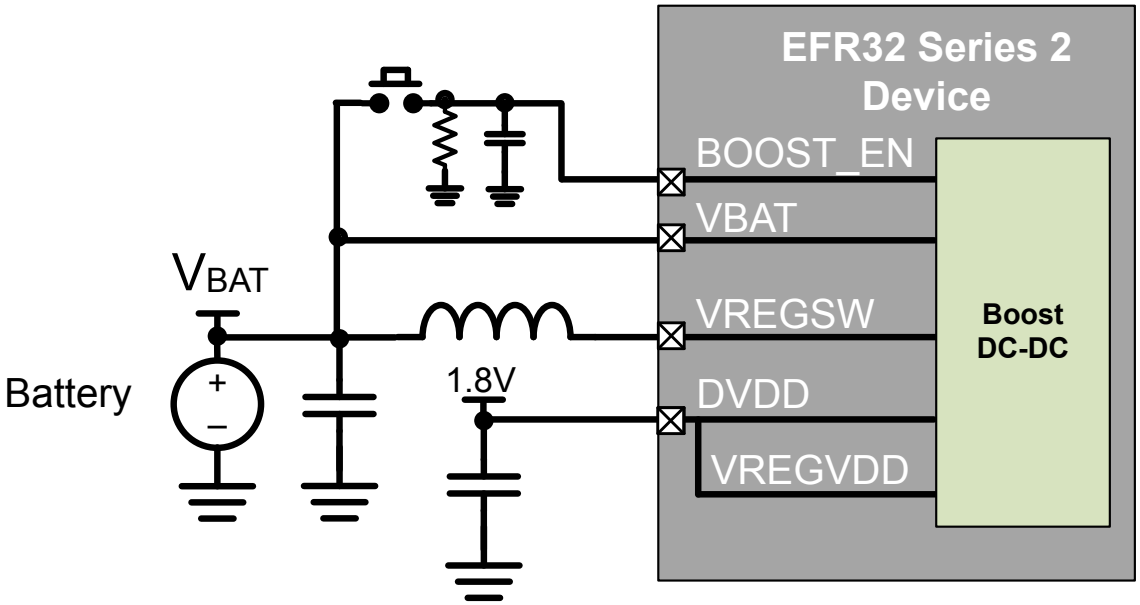


Figure 3.4. Typical Connections for Use Case 2: BOOST_EN Connected to VBAT through Momentary Pushbutton

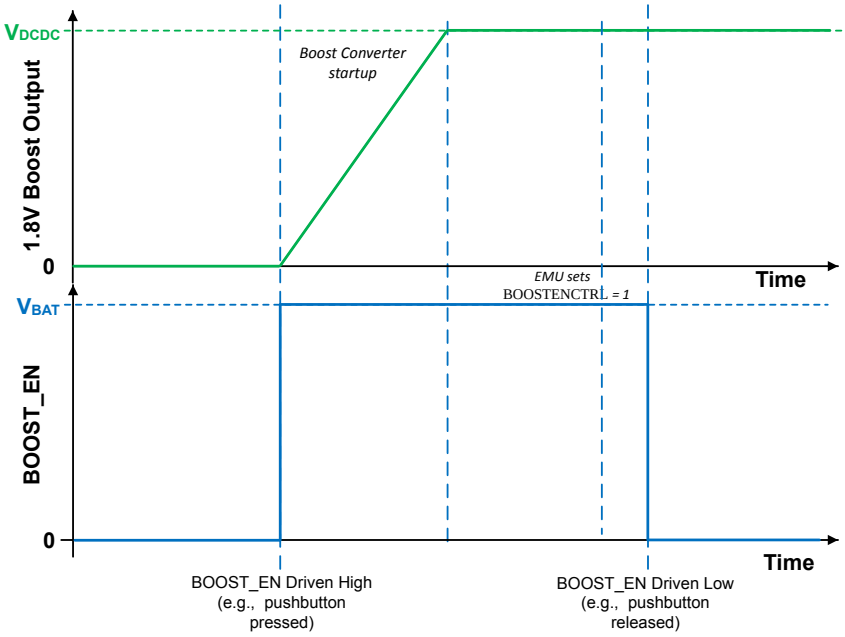


Figure 3.5. Switching cycle for Use Case 2: BOOST_EN Connected to VBAT through Momentary Pushbutton

Note: Instead of a push button, the BOOST_EN input may also be controlled by an external IC if desired.

3.6 Recommended Configuration Settings

Certain DC-DC parameters are adjustable for fine-tuning of performance, but the majority of applications will not need to use any other than the default/recommended settings in boost mode. All data sheet parameters are specified using the recommended settings detailed in this section.

The DCDC_BSTEM01CTRL and DCDC_BSTEM23CTRL registers each have an IPKVAL field to adjust the maximum peak/load current, and a DRVSPEED field to adjust the driver speed. DCDC_BSTEM01CTRL sets the configuration for EM0 and EM1 operation while DCDC_BSTEM23CTRL sets the configuration for EM2 and EM3 operation. The DCDC_BSTCTRL IPKTMAXCTRL and BSTTOFFMAX fields adjust the maximum times for peak current detection and off time which impact the voltage ripple at the boost DC-DC output. The recommended settings are shown in Table 3.2 DRVSPEED, IPKVAL, IPKMAXCTRL, and BSTTOFFMAX Recommended Settings for Boost DC-DC on page 12.

Table 3.2. DRVSPEED, IPKVAL, IPKMAXCTRL, and BSTTOFFMAX Recommended Settings for Boost DC-DC

Bit Field	Recommended Setting
DCDC_BSTEM01CTRL.IPKVAL	13 (LOAD25MA)
DCDC_BSTEM01CTRL.DRVSPEED	1 (DEFAULT_SETTING)
DCDC_BSTEM23CTRL.IPKVAL	10 (LOAD10MA)
DCDC_BSTEM23CTRL.DRVSPEED	1 (DEFAULT_SETTING)
DCDC_BSTCTRL.IPKTMAXCTRL	4 (TMAX_1P19US)
DCDC_BSTCTRL.BSTTOFFMAX	7 (TMAX_2P03US)

4. Power Configurations

In order to deliver the best energy efficiency, most EFM32 and EFR32 Series 2 devices incorporate the DC-DC module to power internal circuits. Operation with or without the DC-DC is supported and, when used, the DC-DC requires an external inductor and capacitor (refer to the data sheet for recommended values).

EFM32 and EFR32 Series 2 devices with the DC-DC have multiple power supply rails: buck DC-DC input (VREGVDD), boost DC-DC input (VBAT, EFR32xG27 only), digital LDO and flash supply (DVDD), analog blocks supply (AVDD), I/O pins supply (IOVDD), RF analog supply (RFVDD, EFR32 Series 2 only), RF power amplifier supply (PAVDD, EFR32 Series 2 only), and the low-voltage digital logic supply (DECOUPLE). Additional detail for each configuration and option is provided in the following sections.

Due to on-chip circuitry (e.g., diodes), some EFM32 and EFR32 Series 2 device's power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFM32 and EFR32 Series 2 device's supply pins are defined below. Exceeding these constraints can result in damage to the device and/or increased current draw.

No DC-DC or Buck DC-DC

- VREGVDD ≥ DVDD: In systems not using the DC-DC, VREGVDD must be externally shorted to DVDD. In systems using the buck DC-DC, DVDD (buck DC-DC output) should be connected to the recommended L_{DCDC} and C_{DCDC} configuration and should not be driven by an off-chip regulator.
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pins.
- VBAT, BOOST_EN: Tie to VSS (EFR32xG27 WLCSP package only).

Boost DC-DC

- VBAT: Boost DC-DC input. Connect to recommended supply and L_{DCDC}.
- DVDD: Boost DC-DC output. Should be bypassed with the recommended C_{DCDC}. Should not be driven by an off-chip regulator.
- VREGVDD: Tie directly to DVDD (EFR32xG27 WLCSP package only).
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pins.

Additionally, there are other system-level considerations related to power supply selection:

- The usable range for analog signals connected to GPIO pins (such as IADC inputs) is limited to the lower of AVDD and IOVDD.
- The RESETn pin is internally pulled to the DVDD supply. If RESETn is driven by external circuitry or pulled up to a voltage above DVDD, additional current will flow into the pin due to the on-chip pull-up.

4.1 Startup Configuration: No DC-DC and Buck DC-DC

At power-on reset (POR), the system operates in a safe startup configuration that supports the no DC-DC and buck DC-DC power configurations. The startup configuration is shown in the simplified diagram below.

In the startup configuration the DC-DC bypass switch is ON (i.e., the VREGVDD pin is shorted internally to the DVDD pin).

After power-on, software can turn on the buck DC-DC if the external hardware configuration supports it.

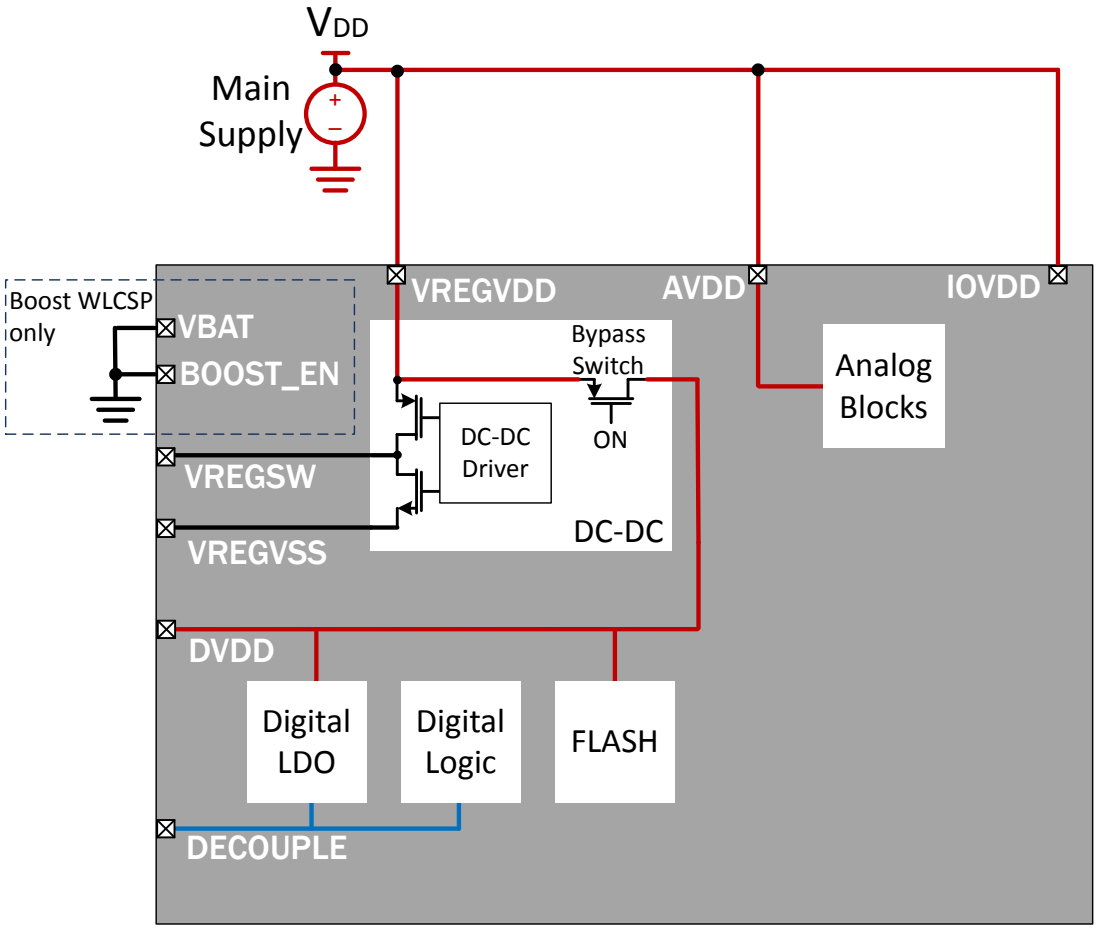


Figure 4.1. Startup Power Configuration

Note: Devices supporting both buck DC-DC and boost DC-DC should have the VBAT and BOOST_EN pins tied to ground when operating in no DC-DC or buck DC-DC power configuration.

4.2 Power Configuration 1: No DC-DC

Power Configuration 1 is supported on devices with a buck DC-DC. In Power Configuration 1, the buck DC-DC is unused, and all power is supplied by external sources. The DVDD pin must be shorted to VREGVDD.

Other supplies may be supplied by the same supply as VREGVDD and DVDD (as shown in Figure 4.2 DC-DC Off Power Configuration on page 15), or they may be powered from one or more sources.

VREGSW must be left disconnected in this configuration.

Devices supporting both buck DC-DC and boost DC-DC should have the VBAT and BOOST_EN pins tied to ground when operating without DC-DC.

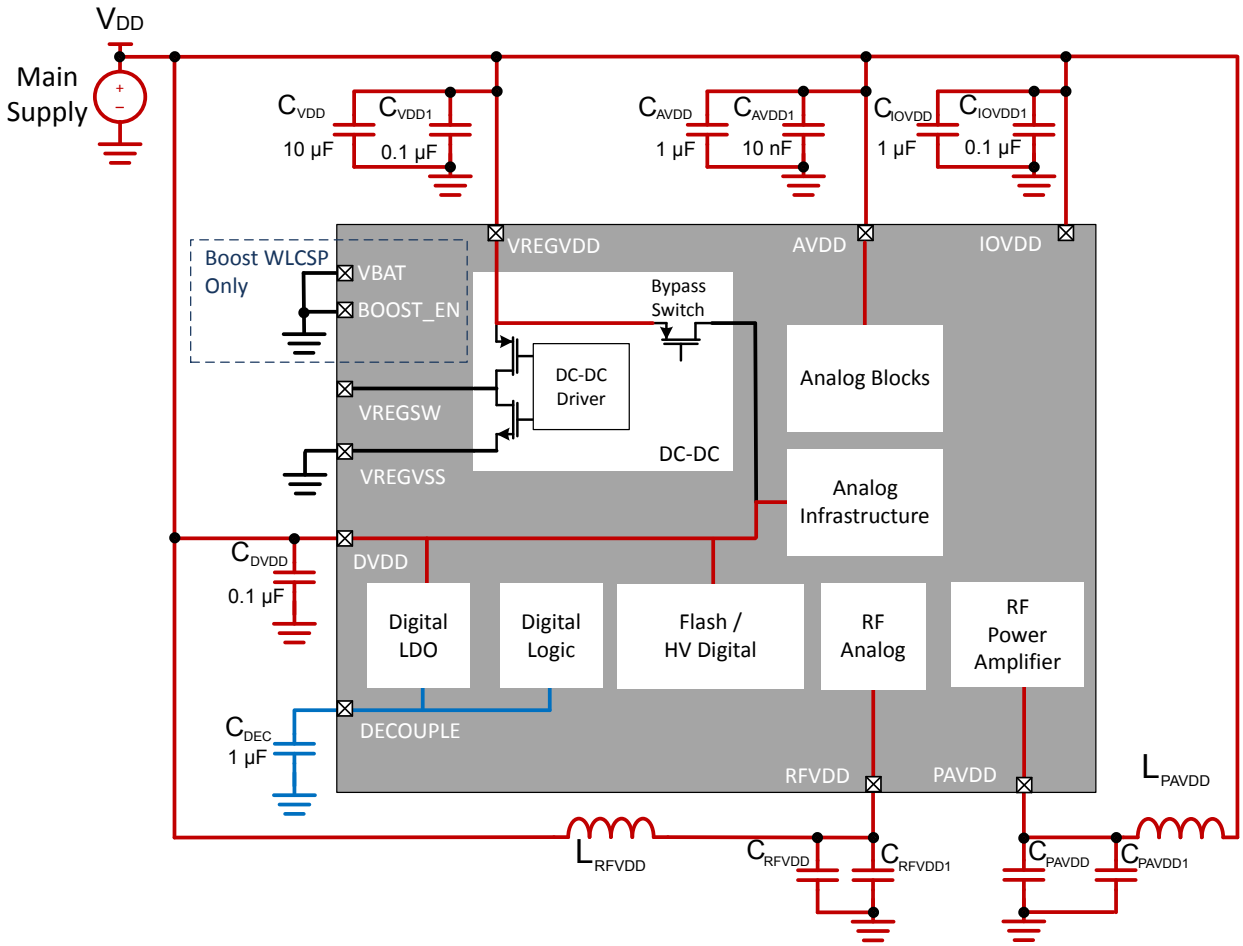


Figure 4.2. DC-DC Off Power Configuration

Note: Please consult AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations for specific values of the C_{RFVDD}, C_{RFVDD1}, C_{PAVDD}, C_{PAVDD1}, L_{RFVDD}, and L_{RFVDD1} components for each device family.

4.3 Power Configuration 2: Buck DC-DC

Power Configuration 2 is supported on devices with a buck DC-DC. The buck DC-DC can be used to power the rest of the supplies on the device at 1.8 V from a higher voltage (1.8 to 3.8 V) supply connected to VREGVDD.

For the best energy efficiency, the DC-DC should generally be used to power DVDD, RFVDD, and, if permissible for the desired transmit power level, PAVDD. When the buck DC-DC regulates the DVDD supply, the maximum voltage may be limited by the operating temperature and/or the average lifetime load conditions. Refer to the device data sheet for additional details.

When the buck DC-DC is used, its output (V_{DCDC}) is connected to DVDD and, on EFR32 Series 2 devices, to RFVDD and PAVDD for supported transmit power levels. The buck DC-DC can optionally power AVDD and IOVDD if V_{DCDC} is compatible with the system's analog and digital I/O voltage levels. In the configuration shown in Figure 4.3 Buck DC-DC Power Configuration on page 16, the AVDD and IOVDD supplies are connected to the main supply to support higher voltage external interfaces.

Devices supporting both buck DC-DC and boost DC-DC should have the VBAT and BOOST_EN pins tied to ground when operating with buck DC-DC.

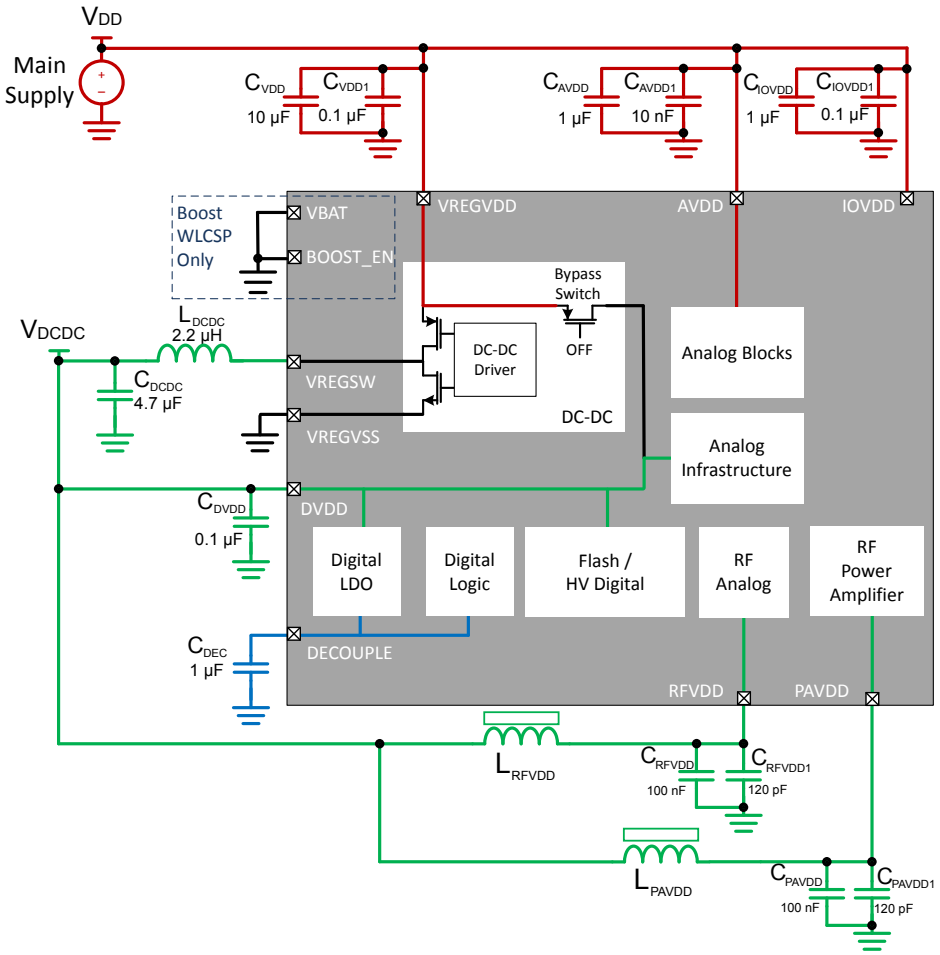


Figure 4.3. Buck DC-DC Power Configuration

Note: The component values shown in this figure are for 2.4 GHz operation on EFR32xG22. The filter component values for RFVDD and PAVDD differ on other devices and for other radio configurations. See AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations for details.

As the VREGVDD voltage approaches the buck DC-DC output voltage, it eventually reaches a point where it becomes inefficient (or impossible) for the buck DC-DC to regulate V_{DCDC}. At this point, software should enable bypass mode, which disables the DC-DC and shorts the VREGVDD supply voltage directly to the buck DC-DC output. If and when sufficient voltage margin on VREGVDD returns, the buck DC-DC can be re-enabled.

4.4 Power Configuration 3: Boost DC-DC

Power Configuration 3 is supported on devices with a boost DC-DC converter. The boost DC-DC converter can be used to power the rest of the supplies on the device at 1.8 V from a lower voltage (0.8 to 1.7 V) supply connected to VBAT. The boost DC-DC output (V_{DCDC}) is used to supply all the other supplies on the chip. Optionally, IOVDD may be connected to VBAT or a different external supply to match the logic levels of connected devices.

Devices supporting both buck DC-DC and boost DC-DC should have the VREGVDD and DVDD pins shorted together when operating with boost DC-DC.

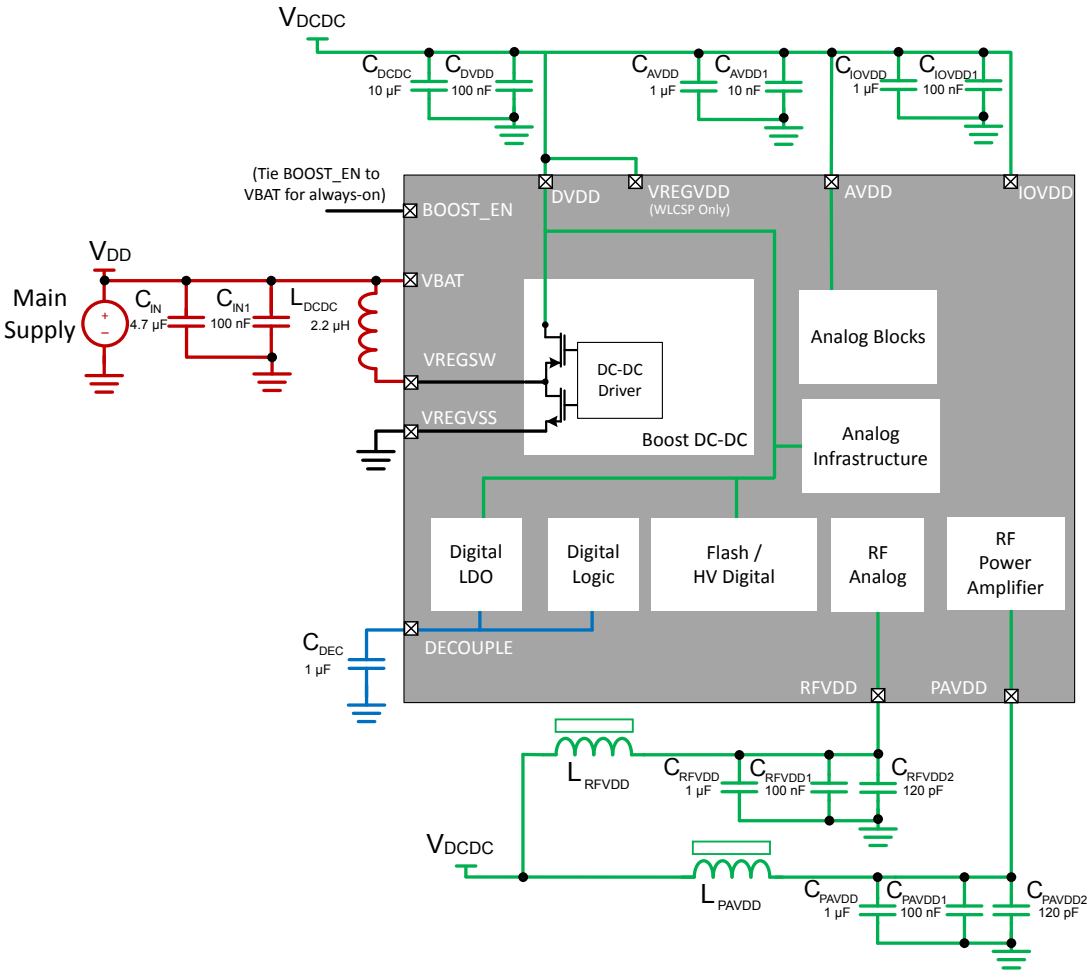


Figure 4.4. Boost DC-DC Power Configuration

The boost DC-DC has a dedicated enable pin, BOOST_EN, which can be used to start (and optionally shut down) the converter. The BOOST_EN pin may be tied to VBAT to enable the boost DC-DC whenever VBAT is powered.

5. DC-DC Programming Using EMLIB

To simplify use of the DC-DC, emlib contains functions that properly configure the DC-DC for efficient operation. Use of these emlib functions is strongly encouraged because they workaround any errata issues that may affect the DC-DC. More information on the EMU emlib library can be found in the EMLIB API.

5.1 Configure the Buck DC-DC

1. Declare a structure of type `EMU_DCDCInit_TypeDef`.

```
typedef struct
{
        EMU_DcdcMode_TypeDef            mode;
        EMU_VreginCmpThreshold_TypeDef  cmpThreshold;
        EMU_DcdcTonMaxTimeout_TypeDef   tonMax;
        bool                            dcmOnlyEn;
        EMU_DcdcDriveSpeed_TypeDef      driveSpeedEM01;
        EMU_DcdcDriveSpeed_TypeDef      driveSpeedEM23;
        EMU_DcdcPeakCurrent_TypeDef     peakCurrentEM01;
        EMU_DcdcPeakCurrent_TypeDef     peakCurrentEM23;
} EMU_DCDCInit_TypeDef;
```

Table 5.1. Parameter Descriptions and Configuration Settings

Parameters	Description and Configuration Settings
`mode`	The buck DC-DC operating mode may be set to: • `emuDcdcMode_Bypass` — Enables bypass mode (i.e., the DC-to-DC converter is not switching, and the VREGVDD pin is shorted internally to the DVDD pin) • `emuDcdcMode_Regulation` — Requests DC-to-DC regulation and disables the bypass switch
`cmpThreshold`	VREGIN comparator threshold voltage. A status bit and optional interrupts indicate if the VREGIN voltage is above or below: • `emuVreginCmpThreshold_2v0` — regulator input threshold voltage set to 2.0 V • `emuVreginCmpThreshold_2v1` — regulator input threshold voltage set to 2.1 V • `emuVreginCmpThreshold_2v2` — regulator input threshold voltage set to 2.2 V • `emuVreginCmpThreshold_2v3` — regulator input threshold voltage set to 2.3 V

Parameters	Description and Configuration Settings
`tonMax`	`tonMax` corresponds to the IPKTMAXCTRL field, which specifies the timeout duration during which the buck DC-DC is expected to reach the programmed peak current (IPK). The TMAX interrupt flag in the DCDC_IF register is set if peak current is not reached before the specified timeout: For EFx32xG22 and EFR32xG27: • `emuDcdcTonMaxTimeout_Off` — timeout disabled • `emuDcdcTonMaxTimeout_0P35us` — 0.35 µs • `emuDcdcTonMaxTimeout_0P63us` — 0.63 µs • `emuDcdcTonMaxTimeout_0P91us` — 0.91 µs • `emuDcdcTonMaxTimeout_1P19us` — 1.19 µs • `emuDcdcTonMaxTimeout_1P47us` — 1.47 µs • `emuDcdcTonMaxTimeout_1P75us` — 1.75 µs • `emuDcdcTonMaxTimeout_2P03us` — 2.03 µs For all other devices, the IPKTMAXCTRL value can be set from 0 to 31 inclusive. When `tonMax` is set to 0, the timeout is disabled. Otherwise, the Ton max time is equal to: Ton_max = (ipk_tmax_ctrl + 1) * 0.07us For example, if IPKTMAXCTRL is set to 16, then: Ton_max = (16 + 1) * 0.07us = 1.19us Please consult the EMLIB API for specific enum defines for individual settings of this field.
`dcmOnlyEn`	`dcmOnlyEn` enable DCM only (on supported devices) defined as follows: • false — DUALMODE — CCM regulation to support higher load currents at lower input voltages • true — DCMONLYEN — DCM regulation only (default configuration)
`driveSpeedEM01` and `driveSpeedEM23`	Drive speed settings in EM0/1 and EM2/3, respectively. Drive speed determines the trade-off between EMI and regulator efficiency: • `emuDcdcDriveSpeed_BestEmi` — Not recommended for use (no benefit to this setting) • `emuDcdcDriveSpeed_Default` — Default efficiency, acceptable EMI • `emuDcdcDriveSpeed_Intermediate` — Not recommended for use (no benefit to this setting) • `emuDcdcDriveSpeed_BestEfficiency` — Not recommended for use (no benefit to this setting)

Parameters	Description and Configuration Settings
`peakCurrentEM01`	Peak current settings in EM0/1. Buck DC-DC peak current correlates with load current as follows: • `emuDcdcPeakCurrent_Load36mA` — Load current = 36 mA; peak current = 90 mA • `emuDcdcPeakCurrent_Load40mA` — Load current = 40 mA; peak current = 100 mA • `emuDcdcPeakCurrent_Load44mA` — Load current = 44 mA; peak current = 110 mA • `emuDcdcPeakCurrent_Load48mA` — Load current = 48 mA; peak current = 120 mA • `emuDcdcPeakCurrent_Load52mA` — Load current = 52 mA; peak current = 130 mA • `emuDcdcPeakCurrent_Load56mA` — Load current = 56 mA; peak current = 140 mA • `emuDcdcPeakCurrent_Load60mA` — Load current = 60 mA; peak current = 150 mA
`peakCurrentEM23`	Peak current settings in EM2/3. Buck DC-DC peak current correlates with load current as follows: • `emuDcdcPeakCurrent_Load5mA` — Load current = 5 mA; peak current = 90 mA • `emuDcdcPeakCurrent_Load10mA` — Load current = 10 mA; peak current = 150 mA

2. Call `EMU_DCDCInit()`, passing the `EMU_DCDCInit_TypeDef` structure created in step 1, as an argument. Alternately, the `EMU_DCDCINIT_DEFAULT` default initializer can be used, as shown below. Upon completion of this function, the buck DC-DC will be configured and in regulation unless bypass is specified. This function does the following:
   - Enables the DC-DC clock tree in order to modify the DC-DC module registers.
   - If the register is available, enable the DC-DC module.
   - Unlocks access to all DC-DC registers.
   - Configures the VREGIN comparator threshold based on the `cmpThreshold` value.
   - Configures the CTRL register using values from `tonMax` and `dcmOnlyEn`.
   - Loads the EM01CTRL0 and EM23CTRL0 registers with the respective drive speed and peak current settings.
   - Configures the DC-DC for the specified operating mode (regulation or bypass).
   - Relocks DC-DC registers if previously locked.

Programming Example for Configuring Buck DC-DC

Using the buck DC-DC default configuration:

```
EMU_DCDCInit_TypeDef dcdcInit = EMU_DCDCINIT_DEFAULT;
EMU_DCDCInit(&dcdcInit);
```

5.2 Configure the Boost DC-DC

1. Declare a structure of type `EMU_DCDCBoostInit_TypeDef`.

```
typedef struct {
  EMU_DcdcBoostTonMaxTimeout_TypeDef    tonMax;
  bool                                  externalShutdownEn;
  EMU_DcdcBoostDriveSpeed_TypeDef       driveSpeedEM01;
  EMU_DcdcBoostDriveSpeed_TypeDef       driveSpeedEM23;
  EMU_DcdcBoostEM01PeakCurrent_TypeDef  peakCurrentEM01;
  EMU_DcdcBoostEM23PeakCurrent_TypeDef  peakCurrentEM23;
} EMU_DCDCBoostInit_TypeDef;
```

Table 5.2. Parameter Descriptions and Configuration Settings

Parameters	Description and Configuration Settings
`tonMax`	`tonMax` corresponds to the DCDC_BSTCTRL.IPKT-MAXCTRL field, which specifies the timeout duration during which the boost DC-DC is expected to reach the programmed peak current (IPK). The TMAX interrupt flag in the DCDC_IF register is set if peak current is not reached before the specified timeout: • `emuDcdcBoostTonMaxTimeout_Off` — timeout disabled • `emuDcdcBoostTonMaxTimeout_0P35us` — 0.35 µs • `emuDcdcBoostTonMaxTimeout_0P63us` — 0.63 µs • `emuDcdcBoostTonMaxTimeout_0P91us` — 0.91 µs • `emuDcdcBoostTonMaxTimeout_1P19us` — 1.19 µs • `emuDcdcBoostTonMaxTimeout_1P47us` — 1.47 µs • `emuDcdcBoostTonMaxTimeout_1P75us` — 1.75 µs • `emuDcdcBoostTonMaxTimeout_2P03us` — 2.03 µs
`externalShutdownEn`	`externalShutdownEn` determines the post-boot behavior of the BOOST_EN input. It is defined as follows: • `false` — BOOST_EN operates as a general input (readable by software) or interrupt line. • `true` — A logic low level on BOOST_EN will disable the boost DCDCconverter and power down the device
`driveSpeedEM01` and `driveSpeedEM23`	Drive speed settings in EM0/1 and EM2/3, respectively. Drive speed determines the trade-off between EMI and regulator efficiency: • `emuDcdcBoostDriveSpeed_Default` — Recommended for use for best efficiency and low EMI

Parameters	Description and Configuration Settings
peakCurrentEM01	Peak current settings in EM0/1. Boost DC-DC peak current correlates with load current as follows: • emuDcdcBoostEM01PeakCurrent_Load10mA — Load current = 10 mA; peak current = 90 mA • emuDcdcBoostEM01PeakCurrent_Load11mA — Load current = 11.7 mA; peak current = 100 mA • emuDcdcBoostEM01PeakCurrent_Load13mA — Load current = 13.3 mA; peak current = 110 mA • emuDcdcBoostEM01PeakCurrent_Load15mA — Load current = 15 mA; peak current = 120 mA • emuDcdcBoostEM01PeakCurrent_Load16mA — Load current = 16.7 mA; peak current = 130 mA • emuDcdcBoostEM01PeakCurrent_Load18mA — Load current = 18.3 mA; peak current = 140 mA • emuDcdcBoostEM01PeakCurrent_Load20mA — Load current = 20 mA; peak current = 150 mA • emuDcdcBoostEM01PeakCurrent_Load21mA — Load current = 21.7 mA; peak current = 160 mA • emuDcdcBoostEM01PeakCurrent_Load23mA — Load current = 23.3 mA; peak current = 170 mA • emuDcdcBoostEM01PeakCurrent_Load25mA — Load current = 25 mA; peak current = 180 mA • emuDcdcBoostEM01PeakCurrent_Load26mA — Load current = 26.7 mA; peak current = 190 mA
peakCurrentEM23	Peak current settings in EM2/3. Boost DC-DC peak current correlates with load current as follows: • emuDcdcBoostEM23PeakCurrent_Load5mA — Load current = 5 mA; peak current = 90 mA • emuDcdcBoostEM23PeakCurrent_Load10mA — Load current = 10 mA; peak current = 150 mA

2. Call EMU_DCDCBoostInit(), passing the EMU_DCDCBoostInit_TypeDef structure created in step 1 as an argument. Alternately, the EMU_DCDCBOOSTINIT_DEFAULT default initializer can be used, as shown below. Upon completion of this function, the boost DC-DC will be configured and in regulation. This function does the following:
   - Enables the DC-DC clock tree in order to modify the DC-DC module registers.
   - Unlocks access to all DC-DC registers.
   - Configures the BSTCTRL register using values from tonMax.
   - Loads the BSTEM01CTRL and BSTEM23CTRL registers with the respective drive speed and peak current settings.
   - Loads BOOSTCTRL register with the value from externalShutdownEn.
   - Configures the DC-DC for the regulation mode.
   - Relocks DC-DC registers if previously locked.

Programming Example for Configuring Boost DC-DC

Using the boost DC-DC default configuration:

```
EMU_DCDCBoostInit_TypeDef dcdcInit = EMU_DCDCBOOSTINIT_DEFAULT;
EMU_DCDCBoostInit(&dcdcInit);
```

5.3 Turning the DC-DC Off

To power off the DC-DC and turn on the internal bypass switch, call the EMU_DCDCPowerOff() function. This function should be used when VREGIN drops below the low threshold, e.g., in response to the VREGINLOW interrupt.

Note: In a boost DC-DC there is no DC-DC bypass mode.

5.4 Operation in Low Energy Modes (EM2, EM3, and EM4)

Whether or not the DC-DC is enabled does not impact use of the `EMU_EnterEM2()` and `EMU_EnterEM3()` functions to enter low-energy modes. When entering EM2 or EM3, the DC-DC remains in the previously programmed regulation or bypass mode. Note, however, that the DC-DC cannot remain enabled in EM4, and the `EMU_EnterEM4()` function explicitly places the DC-DC in bypass mode to comply with this requirement.

Note: In a boost DC-DC there is no DC-DC bypass mode, so EM4 state is not possible. EM4 entry will be blocked and the EM4ERRIF flag will be set, if attempted.

6. DC-DC Configuration Reference

Note: Emlib contains functions to properly configure the DC-DC for efficient operation. Use of these functions is highly recommended because they account for any errata that may affect the block.

6.1 DC-DC Module Register Locks

The EMU and DC-DC modules have locking mechanisms that can be used to prevent accidental changes to the EMU and DC-DC configuration registers. These are unlocked by default. If they are locked when calling a configuration function, emlib will unlock the registers, perform the necessary modifications, and then re-lock the registers upon exit.

1. All EMU registers may be unlocked by writing 0xADE8 to the EMU_LOCK register or locked by writing any other value.
2. All DC-DC registers may be unlocked by writing 0xABCD to the DCDC_LOCK register or locked by writing any other value.

7. Component Selection Guide

7.1 DC-DC Output Capacitor

The components shown in Table 7.1 Recommended Buck DC-DC Output Capacitor on page 26 and Table 7.2 Recommended Boost DC-DC Output Capacitor on page 26 have been used for DC-DC validation and characterization testing on EFM32 and EFR32 Series 2 devices. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. Be certain that the minimum capacitance counting all error sources complies with specific device data sheet guidance (e.g., some devices mandate no less than 3.6 µF).
The output capacitor should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55°C – +85°C (standard temperature range devices) or -55°C – +125°C (extended temperature range devices).

The system designer should pay particular attention to the characteristics of the output capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages) can experience a dramatic reduction in capacitance value as the temperature or bias voltage increases. A change that pushes the DC-DC output capacitance outside of the data sheet specified limits may result in output instability.

Table 7.1. Recommended Buck DC-DC Output Capacitor

Manufacturer	Part Number	Value (µF)	Voltage Rating (V)	Dielectric	Operating Temperature (°C)	Package
Samsung	CL10B475KQ8NQNC	4.7 ± 10%	6.3	X7R	-55 to +125	0603/1608
TDK	CGA5L3X8R1C475K160AB	4.7 ± 10%	16	X8R	-55 to +150	1206/3216

Table 7.2. Recommended Boost DC-DC Output Capacitor

Manufacturer	Part Number	Value (µF)	Voltage Rating (V)	Dielectric	Operating Temperature (°C)	Package
TDK	C2012X8L0J106K125AC	10 ± 10%	6.3	X8L	-55 to +150	0805/2012

7.2 DC-DC Inductor

Please refer to the device specific data sheets for the inductors used for DC-DC validation and characterization testing.

Depending on system requirements, the following inductors may also be suitable, but only EM0 efficiency has been measured.

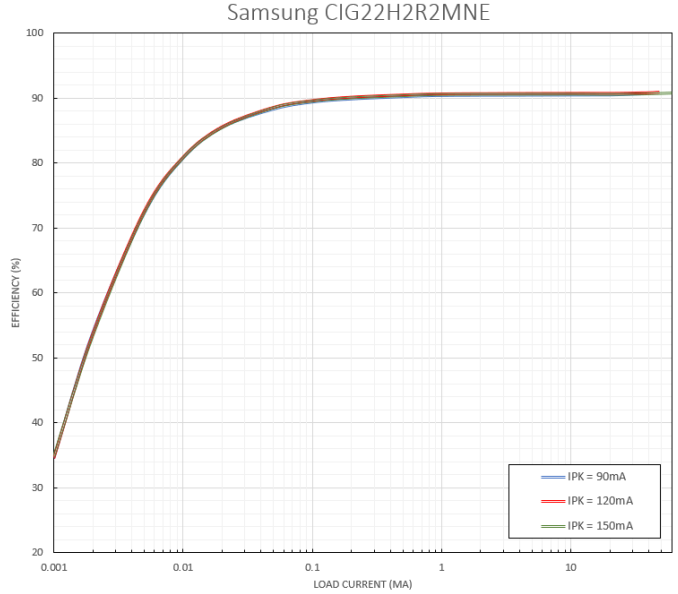
Table 7.3. Example Buck DC-DC Inductors

Manufacturer	Part Number	Value (µH)	$I_{saturation}$ (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Samsung	CIG22H2R2MNE	2.2 ± 20%	1800	0.116 ± 20%	-40 to +125	1008/2520
TDK	MLZ2012N2R2LT000	2.2 ± 20%	170[1]	0.12 ± 20%	-55 to +125	0805/2012
Murata	LQM18PZ2R2MDH	2.2 ± 20%	250	0.47 max	-55 to +125	0603/1608
Murata	LQM18PZ2R2MFH	2.2 ± 20%	300	0.47 max	-55 to +125	0603/1608
Murata	LQM18PZ2R2MCH	2.2 ± 20%	200	0.48 max	-55 to +125	0603/1608
Murata	LQM18PN2R2MGH	2.2 ± 20%	250	0.25 max	-40 to +85	0603/1608
TDK	MLZ1608A2R2WT000	2.2 ± 20%	130[1]	0.25 ± 30%	-55 to +125	0603/1608
Murata	LQM18PH2R2MFRL	2.2 ± 20%	150[1]	0.375 max	-55 to +150	0603/1608
Samsung	CIG22L2R2MNE	2.2 ± 20%	Unspecified	0.08 ± 25%	-40 to +125	1008/2520
Samsung	CIGT201610LH2R2MNE	2.2 ± 20%	2300	0.14 ± 20%	-40 to +125	0806/2016
TDK	KLZ2012MHR2R2HTD25	2.2 ± 20%	400	0.16 ± 30%	-55 to +150	0805/2012
Murata	DFE2HCAH2R2MJ0L	2.2 ± 20%	2500	0.101 max	-40 to 150	1008/2520

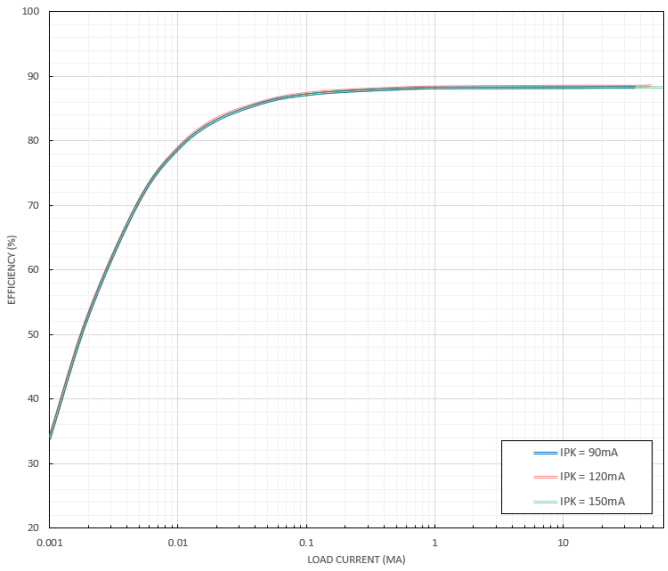
Note:

1. If using EFR32xG23 or EFR32xG24 devices, please choose an inductor that has an saturation current higher than 180mA.

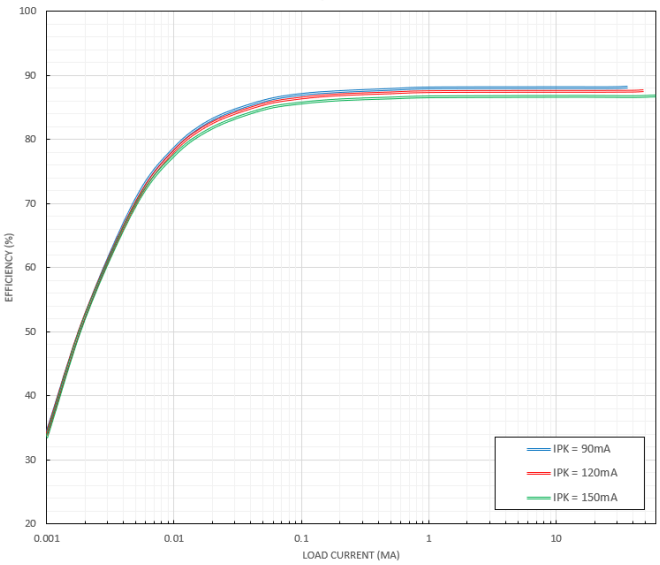
Samsung CIG22H2R2MNE



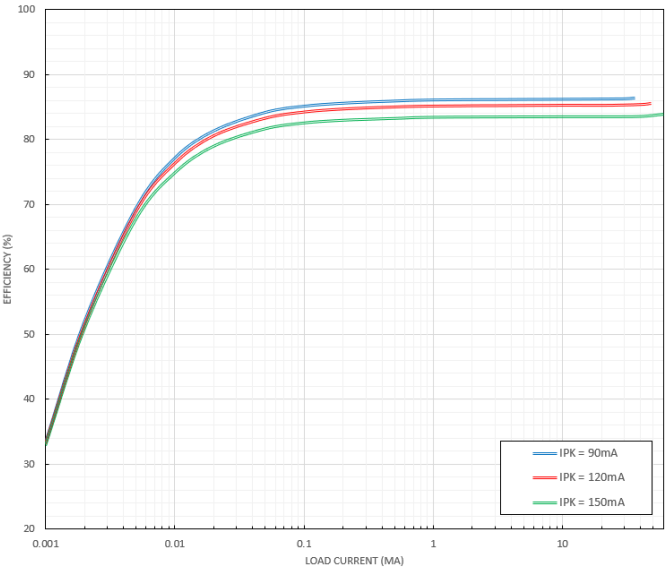
TDK MLZ2012N2R2LT000



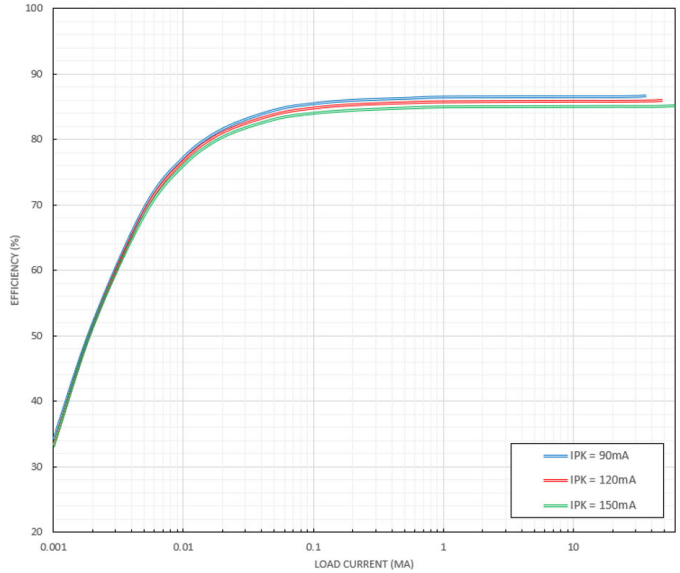
Murata LQM18PZ2R2MDH



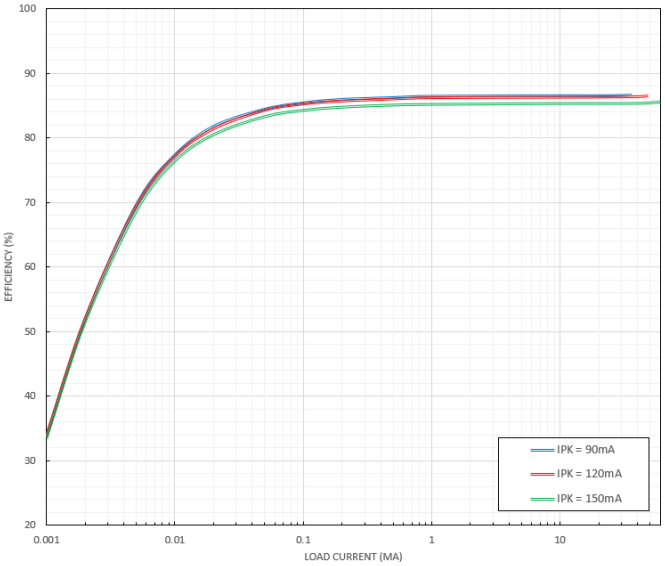
Murata LQM18PZ2R2MFH



Murata LQM18PZ2R2MCH



Murata LQM18PZ2R2MGH



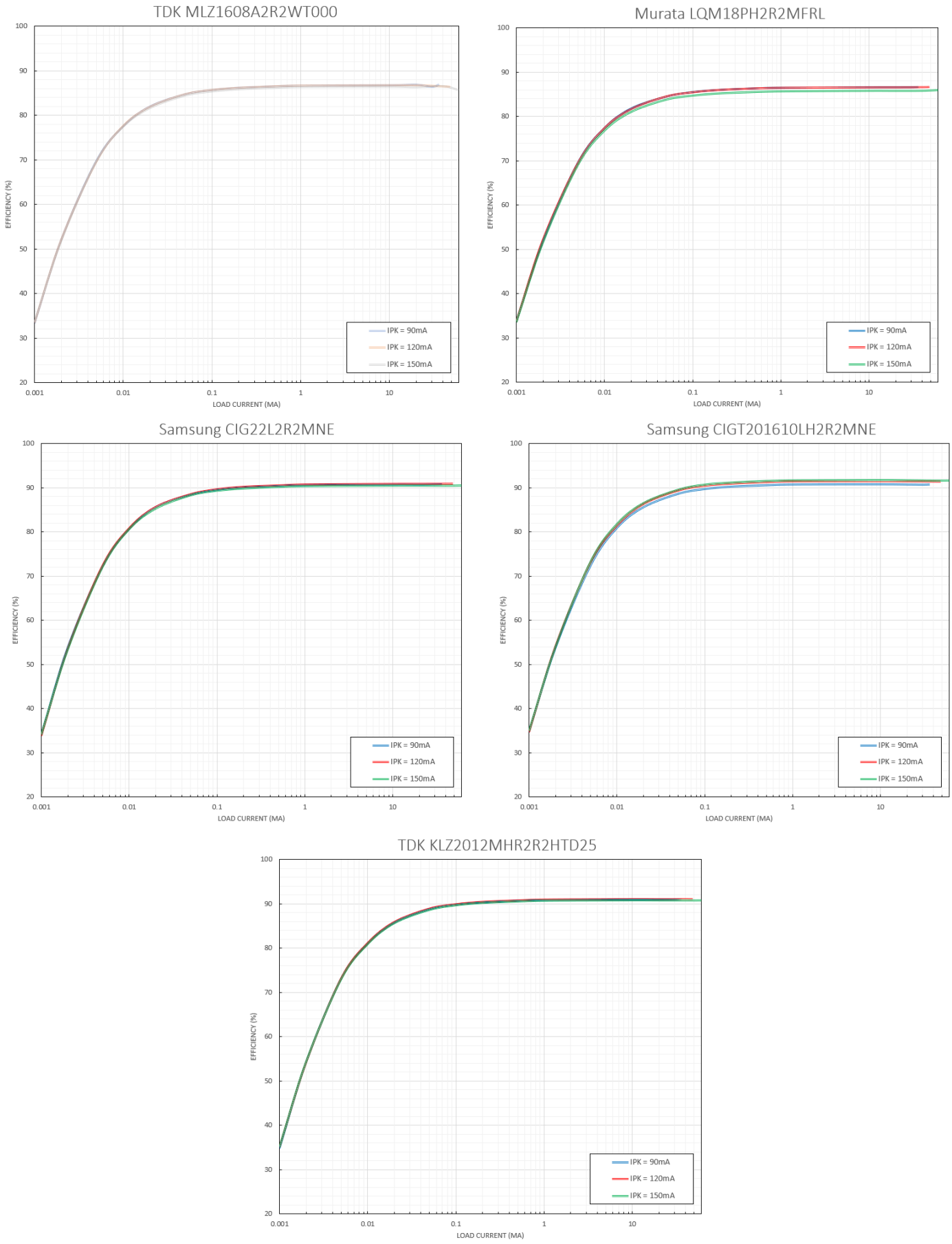


Figure 7.1. Inductor Efficiency Curves, Buck DC-DC Mode, L_{DCDC} = 2.2 µH, VREGVDD = 3.3 V, V_{DCDC} = 1.8 V

8. DC-DC Layout Considerations

Because the DC-DC is a high-frequency, high-current module, some special layout considerations are required for optimal operation.

8.1 Buck DC-DC Layout Considerations

The following connections should be made on the PCB using minimum trace length and resistance:

- Between the VREGSW pin and the L_{DCDC} inductor
- Between the L_{DCDC} inductor and the C_{DCDC} capacitor
- Between the DVDD pin and the C_{DCDC} capacitor
- Between the Main Supply and the VREGVDD pin
- Between the VREGVSS pin and ground
- Between the VBAT, BOOST_EN pins and ground (EFR32xG27 WLCSP package only)

The L_{DCDC} inductor should be placed far away from any noise-sensitive circuitry (e.g., the radio antenna). The inductor should ideally be on the opposite side of the PCB, so that there is a solid ground plane shielding the noisy inductor from the sensitive circuitry.

For more detailed radio-specific layout guidelines, see AN928.2: EFR32 Series 2 Layout Design Guide.

8.2 Boost DC-DC Layout Considerations

The following connections should be made on the PCB using minimum trace length and resistance:

- Between the VBAT pin and the L_{DCDC} inductor
- Between the VREGSW pin and the L_{DCDC} inductor
- Between the L_{DCDC} inductor and the C_{IN} capacitor
- Between the DVDD pin and the C_{DCDC} capacitor
- Between the DVDD pin and the VREGVDD pin (EFR32xG27 WLCSP package only)
- Between the VREGVSS pin and ground

The L_{DCDC} inductor should be placed far away from any noise-sensitive circuitry (e.g., the radio antenna). The inductor should ideally be on the opposite side of the PCB, so that there is a solid ground plane shielding the noisy inductor from the sensitive circuitry.

For more detailed radio-specific layout guidelines, see AN928.2: EFR32 Series 2 Layout Design Guide.

9. Revision History

Revision 0.6

June, 2023

- Added EFR32FG25, EFR32BG27, and EFR32MG27 to the list of applicable devices.
- Separated 2.1 Basic Buck DC-DC from 1. DC-DC Overview into its own section.
- Updated recommended buck configurations settings in Table 2.1 DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for Buck DC-DC on page 6.
- Added 3. Boost DC-DC Module Overview, 4.4 Power Configuration 3: Boost DC-DC, 5.2 Configure the Boost DC-DC, and 8.2 Boost DC-DC Layout Considerations.
- Updated 4. Power Configurations, 4.1 Startup Configuration: No DC-DC and Buck DC-DC, 4.2 Power Configuration 1: No DC-DC, 4.3 Power Configuration 2: Buck DC-DC, and 8.1 Buck DC-DC Layout Considerations to include boost DC-DC pin descriptions.
- Updated driveSpeedEM01, driveSpeedEM23, peakCurrentEM01, and peakCurrentEM23 descriptions in Table 5.1 Parameter Descriptions and Configuration Settings on page 19.
- Added notes to 5.3 Turning the DC-DC Off and 5.4 Operation in Low Energy Modes (EM2, EM3, and EM4) describing operation in boost DC-DC.
- Added Table 7.2 Recommended Boost DC-DC Output Capacitor on page 26.
- Minor updates throughout the document.

Revision 0.5

March, 2022

- Added EFM32PG23 to the list of applicable devices.

Revision 0.4

Feburary, 2022

- Added EFR32BG24 and EFR32MG24 to the list of applicable devices.
- Updated 2.3 Bypass Mode and VREGVDD Comparator to reflect correct indication of the DCDC_STATUS_VREGIN bit.
- Updated 2.4 Buck DC-DC Startup for EFR32xG23 and EFR32xG24 DC-DC startup procedure.
- Updated Table 2.1 DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for Buck DC-DC on page 6 for EFR32xG23 and EFR32xG24
- Corrected Figure 4.2 DC-DC Off Power Configuration on page 15
- Corrected Figure 4.3 Buck DC-DC Power Configuration on page 16
- Added Table 5.1 Parameter Descriptions and Configuration Settings on page 19
- Added Murata DFE2HCAH2R2MJ0 as a recommended inductor in Table 7.3 Example Buck DC-DC Inductors on page 27
- Updated Figure 7.1 Inductor Efficiency Curves, Buck DC-DC Mode, L_{DCDC} = 2.2 µH, VREGVDD = 3.3 V, V_{DCDC} = 1.8 V on page 28
- Updated component specifications in Table 7.3 Example Buck DC-DC Inductors on page 27
- Removed DCM and CCM section as these are no longer relevant on series 2 devices.

Revision 0.3

December, 2021

- Added EFR32ZG23 to the list of applicable devices.

Revision 0.2

August, 2021

- Added EFM32PG22 and EFR32FG23 to the list of applicable devices.
- Corrections to register names and bits throughout.
- Figures in updated to reflect Series 2 architecture.
- Added TDK CGA5L3X8R1C475K160AB to Table 7.1 Recommended Buck DC-DC Output Capacitor on page 26.
- Updated language regarding minimum capacitance in 7.1 DC-DC Output Capacitor.

Revision 0.1

April, 2020

- Initial Revision

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