Hitless switching is a requirement found in many communications systems using phase and frequency synchronization. Hitless switching allows the input clocks of a PLL to be switched during system operation with minimal impact on the communication links. The Si534x and Si538x family of clock devices support hitless switching for many common communications standards. Hitless switching behavior in these devices is easily configured by using Silicon Labs’ ClockBuilder Pro™ software.

**KEY FEATURES**

- Hitless Switching / Phase Build-Out
- Si5345 / Si5344 / Si5342
- Si5344H / Si5342H
- Si5347 / Si5346
- Si5348
- Si5380
1. Introduction to Hitless and Input Clock Switching

The Si534x/8x family of jitter attenuator devices provide hitless switching performance meeting many common communications standards, including ITU-T G.8262 Synchronous Ethernet (SyncE) Options 1 and 2, ITU-T G.812 Type III and IV, ITU-T G.813 Option 1, and Telcordia GR-1244 and GR-253 (Stratum-3/3E).

These communications systems use two or more input clocks as a way to improve system flexibility and reliability. The performance of modern data communications systems is often determined by the quality of the clocks used to transmit and receive data as measured by time jitter in the location of clock edges.

Synchronous communication systems additionally rely on having minimal phase and frequency deviations when the input clock is switched during operation. In this document, the term ‘hitless switching’ indicates that the device output clock continues to meet the communications standard performance requirements, both during and after an input clock switch. One technique for providing hitless switching is to use phase build-out as defined in a number of communications standards. This technique maintains a stable output phase, even when switching between input clocks with phase difference between them. For synchronized systems, phase transient levels are the primary metric in addition to jitter requirements.

The most common metric used for measuring phase transient performance during an input clock switch is Maximum Time-Interval Error (MTIE), as shown in device measurement results at the end of this document. MTIE finds the maximum time-domain deviations from stable reference clock edge times and so is a good measure of the limits of clock switch behavior. MTIE maximum limits are specified in many communications standards where frequency and/or phase synchronization is required.

1.1 System Level Applications of Hitless Switching

The block diagram below shows a clock system for synchronized communications using multiple levels of timing devices. At the top, the first level is the redundant timing cards which handle most of the clock selection, holdover, and jitter tolerance duties. The line cards are below these, on the second level. While a typical clock system may only use two timing cards, it may have many more line cards. These are used to provide additional connections, as well as redundancy from multiple input clock source. The input clocks are switched during operation between master and slave clock sources while minimizing the effects of the clock switch on data reception and transmission.

This document focuses primarily on Hitless Switching performance using Si534x/8x devices in line card applications. Since there are often more line cards than timing cards in a system, it often makes sense to use less expensive crystals or non-temperature-compensated crystal oscillators (XO’s) as reference clocks. The figure below shows the Si5345 as the line card device, though other devices in the family such as the multi-PLL Si5347 can be used here as well.
Figure 1.1. Example of a Common Synchronization System Arrangement

Line card applications, as with the Si5345 in the previous figure, can use a higher PLL loop bandwidth in the range of 100 Hz. This allows the use of less expensive crystals and XO’s as the reference timing source, without significantly degrading the output phase transient performance.

Since the timing cards provide the primary wander filtering for the system, they use a lower PLL loop bandwidth of 0.001 Hz, 0.1 Hz, and up to 1 – 10 Hz. Higher performance TCXO’s (Temperature-Controlled Crystal Oscillator) or OCXO’s (Oven-Controlled Crystal Oscillator) are used in these cases to provide low phase transients in locked and holdover modes. Though not discussed further here, additional compliance reports for Si534x/8x devices in line card configurations are available from the Silicon Labs website through the following links:

- ITU-T G.8262 Compliance Test Results for Si5345/44/42
- ITU-T G.8262 Compliance Test Results for Si5347/46
- ITU-T G.8262 Compliance Test Results for Si5348
- ITU-T G.812 Compliance Test Results for Si5348
- ITU-T G.813 Compliance Test Results for Si5348
- Telcordia GR-253-CORE Compliance Test Results for Si5348
- Telcordia GR-1244-CORE Compliance Test Results for Si5348
1.2 Clock Frequency Tolerance Effects on Phase

Unless they are derived from the same source, two different clock sources will have some frequency difference between them. This is true even for crystals or oscillators specified with the same nominal frequency. The differences in the period of the clocks accumulates and causes the relative phases of the clock edges to vary over time. Synchronized communications systems require control the phase of the clocks, maintaining a long term average frequency difference of 0 ppm. In the short term, switching events and noise can cause small, short-term variations in the frequencies.

![Diagram](attachment:Figure_1.2.png)

These frequency offsets are often quite small and are usually measured in units of parts-per-million (ppm). Offset in ppm = \(1 \times 10^6 \times \left( \frac{F_{\text{MEAS}} - F_{\text{REF}}}{F_{\text{REF}}} \right)\), where \(F_{\text{MEAS}}\) is the measured frequency and \(F_{\text{REF}}\) is either the ideal frequency value or the frequency of a second clock being used for comparison. Some standards allow up to ±100 ppm difference between clocks. In others this difference is ±20 ppm, ±4.6 ppm, or even lower.
1.3 Hitless Switching

When measuring hitless switching performance the frequency and phase variation are measured using two input clocks traceable to the same frequency so that they have the same long term average frequency. In other words, the frequency offset between the input clocks should be 0 ppm for meaningful hitless switching results.

Since the phase should be consistent between two synchronized clocks, we can then describe the static phase difference between these clocks. Ideally, when switching between two clocks where the edges are exactly aligned in time there should be no frequency or phase deviation in the output clock. However, real devices always introduce some amount of non-ideality into the results. Without hitless switching, it is possible that the two clocks are up to 180° out of phase with each other. In this case, one of the clock pulses will be significantly shortened or extended, causing significant frequency and phase variations. Also, temperature variations in the system application can lead to delay changes that slowly change the phase relationship over time.

Hitless switching is used to minimize frequency and phase variations on the output clock when the PLL input clock is switched. Using phase build-out, the device absorbs the phase difference between input clocks at the time of the switch. The output clock will track the new input after the switch has been made but maintaining the phase of the original clock. This significantly reduces the frequency and phase variation from the switch.

The simplified timing diagrams shown below illustrates two cases of PLL input clock switching. The orange segments correspond to CLK 1, while the green segments correspond to CLK 2. These two clocks have the same frequency with 0 ppm frequency offset and with 180° of constant phase difference between them.

The first case illustrates the desired hitless switch. In this case the phase difference of 180° is absorbed by the hitless switching circuitry, preserving the input frequency and phase. This allows the PLL to continue operation with minimal disturbances. This is an example of a hitless switch with phase build-out.

The second case show what would happen with a regular, non-hitless, switch. Without hitless switching, the clock signal at the input of the PLL immediately reacts to the change cause frequency and phase steps, which then must be tracked out by the PLL. This poorly controlled reaction to the input switch leads to short-lived frequency and phase disturbances at the output of the PLL. These types of switches should be avoided for optimal performance in synchronized communication systems.

![Figure 1.3. Comparison of Hitless and Asynchronous Switches](image-url)
2. Configuring Hitless Switching in ClockBuilder Pro

Silicon Labs’ ClockBuilder Pro software (CBPro™ for short) can be used to configure Hitless Switching and other input clock switching parameters, which can then be stored in the device’s non-volatile memory (NVM). When the device is powered up or reset, the values of these and other registers will be loaded as the default operating condition of the device. In-system control can be done using the serial interface (either I2C or SPI) to update register values. The screen captures shown here are for the Si5345 device, but also apply to the other Si534x/8x devices. The ClockBuilder Pro software can be downloaded from the Silicon Labs website:

http://www.silabs.com/CBPro

2.1 Common CBPro Hitless Switching Controls

Input clock frequencies are entered on the "Define Input Clocks" page of CBPro. When using revision D and revision B devices, input backplane frequencies and $F_{PFD}$ update rate must be ≥1 MHz. Use of input frequencies or $F_{PFD}$ frequencies lower than this may cause switching artefacts with revision B and D devices. The $F_{PFD}$ rate can be found in the frequency plan report from CBPro. Also, for best hitless switching performance, the use of gapped input clocks should be avoided.

![Figure 2.1. Input Clock Frequency Selection in CBPro](image-url)
Input switching selections are configured on the "Input Clock Selection" page of CBPro. Both automatic and manual switches are available, as shown in the figures below. Either automatic or manual switching is selected using the radio buttons at the top of the page. See the appropriate device reference manual for more information on manual switching options, as these vary by part number. The latest versions of the Si534x/8x product documents can be found here: http://www.silabs.com/products/clocksoscillators/Pages/si538x-4x-evb.aspx.

When automatic switching is selected, the device will switch to the highest priority valid input clock when the current input clock indicates a fault with Loss-of-Signal (LOS) or Out-of-Frequency (OOF). The priority of input clock selection can be changed by clicking each input and clicking the up or down arrows to adjust its position in the list. "Auto-revert" mode will switch back to the original clock if and when it becomes valid again, i.e. input faults are no longer asserted. "Non-revert" mode will continue to use the new clock, even if the original becomes valid again. For hitless switching applications, it is recommended to leave both OOF and LOS selected for all input clocks in the "Valid Input Clock Mask" section.

![Automatic Input Clock Switching Configuration in CBPro](image)

**Figure 2.2. Automatic Input Clock Switching Configuration in CBPro**
User-controlled manual input switching is also available. The Si5345 provides both register- and pin-controlled switching, though only one method may be used at a time. Other Si534x/8x devices have different options and may provide either one method or the other. When the device being used has clock select pins IN_SEL0 and IN_SEL1, pin-controlled manual switching may be used by the system at any time, though switching faster than the PLL can respond may cause unpredictable results. Register-controlled switches can be performed using the SPI/I2C-compatible serial interface of the device.

![Figure 2.3. Manual Input Clock Switching Configuration in CBPro](image)

Figure 2.3. Manual Input Clock Switching Configuration in CBPro
2.2 CBPro Hitless Switching Controls Differences between Device Revisions

Revision D of the Si534x/8x devices added features to enhance input clock switching, therefore some of the CBPro setup screens will be slightly different from revision B. The frequency plan revision can be checked on the "Device Revision" page of CBPro, as shown in the figure below. Frequency plans should always be written to devices of the same revision for proper operation.

Note: Multi-PLL devices, such as the Si5347, have independent CBPro DSPLL. Configure pages for each PLL.

Figure 2.4. Checking Frequency Plan Revision in CBPro
2.2.1 Hitless Switching Configuration for Rev. D Si534x/8x

Revision D of the Si534x/8x devices added the "Ramped Input Switching" feature which provides adjustable rate frequency ramping when switching between two inputs with non-0 ppm frequency difference. While this feature will not be directly discussed here, CBPro displays the hitless switching options differently for Rev. D than for Rev. B. The "DSPLL Configure" page of CBPro is used to configure hitless switching behavior under the "Input Switching & Holdover" sub-section. When hitless switching phase build-out behavior is desired, the "Enable hitless switching" checkbox should be selected.

With 0 ppm offset input frequencies, ramped input switching is not needed and should be disabled as shown below. The "Ramped Exit from Holdover" option should always remain selected regardless of whether "Ramped Input Switching" is selected or not.

![Hitless Switching Configuration in CBPro – Rev. D Devices](image-url)
Figure 2.6. Disabling Ramped Input Switching in CBPro – Rev. D Devices
2.2.2 Hitless Switching Configuration for Rev. B Si534x/8x

The "DSPLL Configure" page of CBPro is used to enable hitless switching phase build-out behavior in the "Input Switching & Holdover" sub-section of the window. When hitless switching behavior is desired, the "Enable hitless switching" checkbox should be selected, as shown below.

![Figure 2.7. Hitless Switching Configuration in CBPro – Rev. B Devices](image-url)
3. Measuring Clock Switch Performance

Measuring the dynamic phase response of a PLL to an input switch requires precision measurements and specialized equipment beyond what is commonly found in many laboratories. There are a number of ways to measure the effects of hitless switching events. Each method has both strengths and weaknesses depending on which parameters are being measured. The control methods are different for these tests, depending on whether the input clock switch control method is manual or automatic.
3.1 Measurement Equipment Needed

The following table compares several methods for measuring the output phase response of a PLL to an input switch. The methods have different strengths for measuring certain aspects of the PLL response. While these are discussed briefly below, the measurements for this application note were taken using the frequency counter method. There are several methods for measuring the response of a PLL to a clock switch. See the descriptions and table below for a comparison of some of the strengths and limitations between these different methods.

**Table 3.1. Hitless Switching Measurement Method Comparison**

<table>
<thead>
<tr>
<th>Measurement Type</th>
<th>Strengths</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ixia / Anue 3500</td>
<td>• Displays MTIE results quickly</td>
<td>• Input analysis frequencies are limited</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>• Shows the limits of phase movement</td>
<td>• Requires additional software and capture memory to display phase/frequency vs. time and MTIE</td>
</tr>
<tr>
<td></td>
<td>• High sample rates possible</td>
<td>• Longer measurements can be affected by wander</td>
</tr>
<tr>
<td>Frequency Counter with Processing Software</td>
<td>• Long time captures even with short gate times</td>
<td>• Short gate times increase measurement noise</td>
</tr>
<tr>
<td></td>
<td>• Multiple analyses from a single data capture (MTIE, Frequency, Phase, etc.)</td>
<td>• Longer gate times may miss peak values</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Longer time between measurement and analysis</td>
</tr>
<tr>
<td>Keysight E5052B SSA Transient Mode</td>
<td>• Displays both Frequency and Phase vs. time</td>
<td>• Does not display MTIE</td>
</tr>
<tr>
<td>Phase Detector or Mixer with Oscilloscope</td>
<td>• Displays phase vs. time</td>
<td>• Difficult to set up for accurate measurements</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Requires an extra signal source</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Does not provide frequency information</td>
</tr>
</tbody>
</table>

The equipment used to generate the hitless switching results given below is the Ixia / Anue 3500 Synchronization Test Solution. This measures MTIE and includes the templates for a number of common communications standards. There is a somewhat limited set of input frequencies available for analysis covering a number of standards.

A common method of observing the maximum phase response to a clock switch is to use an oscilloscope in persistence mode to measure the PLL output clock. In this case, the PLL is often triggered by the PLL input clock. However, this requires the input and output frequencies to be identical, or to be integer ratios of each other, which limits flexibility. Alternately, a source separate from the PLL input source can be used to provide flexibility as long as both sources are synchronized to the same 10 MHz reference. The oscilloscope shows maximum phase variation around the nominal timing. However, there are several limitations to this approach. First, this approach does not give much detail about the shape of the response versus time. Second, it does not give any information about frequency deviation or MTIE. Third, the longer the measurement time the more the results may be increased by wander effects.

Another approach is to use a frequency counter along with post-processing software to calculate the MTIE. This can provide several different analyses from a single capture. However, there are inherent trade-offs between noise and time granularity. When using short gate times fast events may be observed, but the measurement noise will be increased and sometimes can be larger than the event being measured. Use of longer gate times may average out fast events altogether, giving overly optimistic results.

Use of a signal source analyzer, such as the Keysight E5052, in transient mode can give a more detailed view of frequency and phase versus time. This is often useful in verifying small perturbations and in troubleshooting systems. However, this instrument does not display common compliance metrics such as MTIE.

Another method used for observing the behavior of phase versus time is to use a phase detector or mixer along with an oscilloscope. This method requires an additional low noise signal source if the output frequency is not the same as the input frequency. This source must be synchronized to the same 10 MHz reference as the PLL input source in order to generate meaningful results. Also, the output of the phase detector/mixer must be low-pass filtered before connecting to the oscilloscope input to filter out higher frequency products. Given the higher complexity of this approach, it will not be covered further here.
3.2 Controlling Clock Switches in a Test Environment

As explained in the section above on configuring hitless switching in CBPro, there are two types of clock switches: manual and automatic. The methods for initiating and testing these switches are different, and can lead to differences in the phase response due to a switch. In both cases though, a periodic digital control signal can be used to control the switches. This will be discussed more below in the sections on the test setups.

Manual switches are initiated by the user with the IN_SEL0 and IN_SEL1 pins or register settings of the device. Manual switches are intended to occur between two valid input clocks. In other words, manual switches are performed while both the old and new input clocks are valid, without alarms. Since both clocks are present and valid and have the same frequency, a hitless switch between them only needs to perform phase build-out to keep the output phase consistent with the original clock. If an invalid input is selected using manual control, the device will enter holdover until either the selected clock becomes valid or another valid input is selected.

Automatic switches are initiated when the currently selected input clock indicates and alarm. In testing scenarios, the easiest way to do this is to disable the highest priority input clock. When this input clock signal is turned off the input will indicate an alarm and the internal clock switching control will switch to the highest priority valid input clock available. If there are no available valid clocks at this time, the device will enter holdover mode until a valid input clock is once again presented to the device. Since the alarm detection functions require a finite amount of time before indicating an alarm, an automatic clock switch will be delayed by a short amount of time compared to a manual switch.

3.3 Setups for Measuring Clock Switch Performance

In all cases below, measurement best practices should be followed given the accuracy required. These include, but are not limited to:

- Use soldered or torque wrench tightened connections, as hand tightened connections may be inconsistent.
- Use of reasonably matched-length cables for differential measurements.
- Use of a balun when measuring differential signals with single-ended measurement equipment.
- Avoidance of ground loops between equipment by connecting all equipment to a single AC power circuit.
3.3.1 Setup for Measuring Automatic Hitless Switch Performance

An automatic hitless switch is triggered when the current input clock indicates an alarm. Measuring this in a laboratory test is possible by periodically enabling and disabling the highest priority input clock source. As shown in Figure 2.5 Hitless Switching Configuration in CBPro – Rev. D Devices on page 9, the automatic switch priority is set with IN1 highest, followed by IN0. Also, since the automatic mode is set to [Auto-revert], IN1 will be the selected input clock whenever it shows no alarms. When IN1 indicates an alarm, then the PLL will switch to using IN0. When a valid clock is presented to IN1 again and the alarms are cleared, then the PLL will switch back to using IN1.

In the figure below, the input clock is constantly provided to IN0, but the clock signal to IN1 is periodically removed and restored. In this case, the use of the output enable controls of a Si53301 clock buffer evaluation board is shown. However, this interruption of the clock can be performed by other methods as well. This control causes the PLL source to alternate between IN1 and IN0. Since both clocks are derived from the same source, they will have 0 ppm frequency offset. In order to check the worst case switch conditions, one of IN0/IN1 differential signals may swap connectors, effectively inverting the polarity of the input clock to the device under test. This provides a 180° phase difference between the Si534x/8x inputs.

![Figure 3.1. Automatic Hitless Switching Example Test Setup](image)

A low frequency source is used to control the switching rate operating with a period of $T$ seconds. Note that while both destinations for this signal are high-impedance, a 50 Ω termination may be required to properly terminate the output of the source. If the source allows selectable output impedance, then it may be set to high impedance and a 50 Ω termination may not be necessary. It is very important to verify that there are no reflections or ringing on this control signal, as these may cause unpredictable results from the measurement equipment.

When using an oscilloscope to measure the maximum phase deviation, a third source may be used to provide a stable trigger. In this case, it is important that the primary clock source and the stable oscilloscope trigger signal are synchronized to the same 10 MHz reference source. If this is not done, the small frequency offset between the two sources will be reflected in the results, obscuring the performance of the device under test. Use of the Ixia / Anue 3500 also requires connections to the common 10 MHz reference to generate the input clock sources.

Other arrangements are also possible and clocks may be generated by other means, as long as the principles in this section are followed.
### 3.3.2 Setup for Measuring Manual Hitless Switch Performance

A manual hitless switch is controlled by the user or system level application and may be performed at any time. To measure this in a laboratory test, the INSEL0/1 pins are controlled periodically to switch between valid input clocks. Both input clocks should remain valid without indicating alarms during manual switching. If the PLL is switched to an invalid input clock, the PLL will enter holdover instead. The PLL will exit holdover when either the selected clock becomes valid again, or the PLL is manually switched to a valid input clock.

In the figure below, the input clock is constantly provided to both the IN0 and IN1 inputs without interruption. The IN_SEL0 signal is alternated between 0 V and 3.3 V to control the input selection. Since both clocks are derived from the same source, they will have 0 ppm offset. Since both clocks are derived from the same source, they will have 0 ppm frequency offset. In order to check the worst case switch conditions, one of IN0/IN1 differential signals may swap connectors, effectively inverting the polarity of the input clock to the device under test. This provides a 180° phase difference between the Si534x/8x inputs.

![Diagram](image.png)

**Figure 3.2. Manual Hitless Switching Example Test Setup**

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Other arrangements are also possible and clocks may be generated by other means, as long as the principles in this section are followed.

### 3.4 Hitless Switching Results and Conditions

When showing the MTIE data for the Si534x/8x devices in the following sections, the maximum limit template for several common standards is shown as a green line in the plots. The red line showing the measured data shows a significant margin to these requirements for automatic and manual switching when the input and \( F_{PFD} \) frequencies are both >1 MHz.

The measurements below were taken using the Anue 3500 Synchronization Test Solution equipment. These results were generated using a standard Si5345-EB evaluation board with a Si5344-EB generating the source input clocks. The frequency plan for these measurements uses 25 MHz input clocks with 0 ppm frequency difference. These input clocks are connected so that they have 180° phase difference at the inputs to the Si5344-EB. Both frequency plans use \( F_{PFD} = 1.923 \text{ MHz} \), with the only differences being in the input clock switching method of either manual or automatic switching as shown in the section on CBPro setup and use given previously.
4. Manual Hitless Switching Performance

Figure 4.1. Manual Hitless Switching – G.8262 Option 1 MTIE
5. Automatic Hitless Switching Performance

Figure 5.1. Automatic Hitless Switching – G.8262 Option 1 MTIE
ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

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