



# AN1081: Integrated Passive Devices for EFR32 Series 1 Sub-GHz RF Matching

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The external RF matching network for EFR32 Series 1 devices supporting sub-GHz band operation may be further simplified by integrating all components in a single, Integrated Passive Device (IPD). This application note covers the various aspects of utilizing an IPD in an EFR32 Series 1 design.

EFR32 Series 1 devices supporting sub-GHz frequency bands utilize an external matching network. This network serves several purposes, including impedance transformation from a 50  $\Omega$  antenna to the optimum transmit and receive path impedances for EFR32, single-ended to differential conversion, and lowpass filtering to minimize transmit harmonics and receive out-of-band interference. This network is often implemented by discrete components. Some applications, however, benefit in terms of minimized space, bill of materials, and complexity by integrating all in a single ceramic device, the IPD.

Readers interested in a detailed description of the discrete sub-GHz matching network should refer to [AN923: EFR32 sub-GHz Matching Guide](#).

Performance data for the individual EFR32 Series 1 IPDs are provided in the following application notes:

- [AN1146: Johanson 434 MHz IPDs for EFR32 Series 1 Wireless SOCs](#)
- [AN1147: Murata 434 MHz IPDs for EFR32 Series 1 Wireless SOCs](#)
- [AN1148: Johanson 868 MHz IPDs for EFR32 Series 1 Wireless SOCs](#)
- [AN1149: Murata 868 MHz IPDs for EFR32 Series 1 Wireless SOCs](#)

## KEY POINTS

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- Integrated Passive Devices (IPDs) simplify the EFR32 Series 1 sub-GHz RF matching network design, reducing complexity and PCB board space by 70%
- IPDs are available from leading RF ceramics providers supporting common sub-GHz bands
- Including IPDs in EFR32 Series 1 designs is made straightforward with a few hardware and software design considerations

## 1. Supported Devices and Bands

IPDs are available from leading RF ceramics providers for common bands. As with the discrete EFR32 Series 1 matching networks, IPDs are optimized for a specific frequency, target output power, and supply voltage. Available designs are listed in the following table.

**Table 1.1. IPD Devices for EFR32 Series 1**

Band	TX Power	VDDPA	Manufacturer	Part Number	SGPACTUNE Register, TX	SGPACTUNE Register, RX
434 MHz	+14 dBm	1.8 V	Murata	LFD21433MMF5E258	22	0
434 MHz	+14 dBm	1.8 V	Johanson	0434BM15B0027	22	0
868 MHz	+14 dBm	1.8 V	Murata	LFD21868MMF5E233	0	0
	> +14 dBm	3.3 V			5	0
868 MHz	+14 dBm	1.8 V	Johanson	0868BM15G0027	0	0
	> +14 dBm	3.3 V			5	0

**Note:** Measurements on sample boards showed that the 868 MHz Murata and Johanson IPDs can be used at 3.3 V VDDPA supply voltage: ~ 18-19 dBm output power can be achieved with acceptable TX current and harmonic performance. However, note that extensive characterization of the 868 MHz Murata and Johanson IPDs were performed only for max. +14 dBm transmit power when the PA is powered from 1.8 V.

## 2. Implementation

Incorporation of an IPD in an EFR32 Series 1 design is straightforward with a few additional considerations in PCB and firmware designs.

### 2.1 PCB Design

PCB design is straightforward with focus on minimizing trace lengths and parasitic reactances.

Key considerations include:

- Grounding of IPD ground pins: All should have a clear / straightforward return path to the main RF ground, typically on the PCB plane below the IPD and RFIC.
- Antenna Connection: Provides a 50 Ω controlled impedance connection from IPD ANT port to antenna. This net should include a 56 pF ac coupling capacitor  $C_{COUPLE}$  as some IPD designs' antenna ports are dc-coupled.
- DC Bypass Capacitor,  $C_{BYPASS}$ : 56 pF

The reference RF section schematic and layout and recommended PCB land pattern are shown in the figures below.

Refer to [AN928.1: EFR32 Series 1 Layout Design Guide](#) for additional EFR32 Series 1 PCB design guidance.

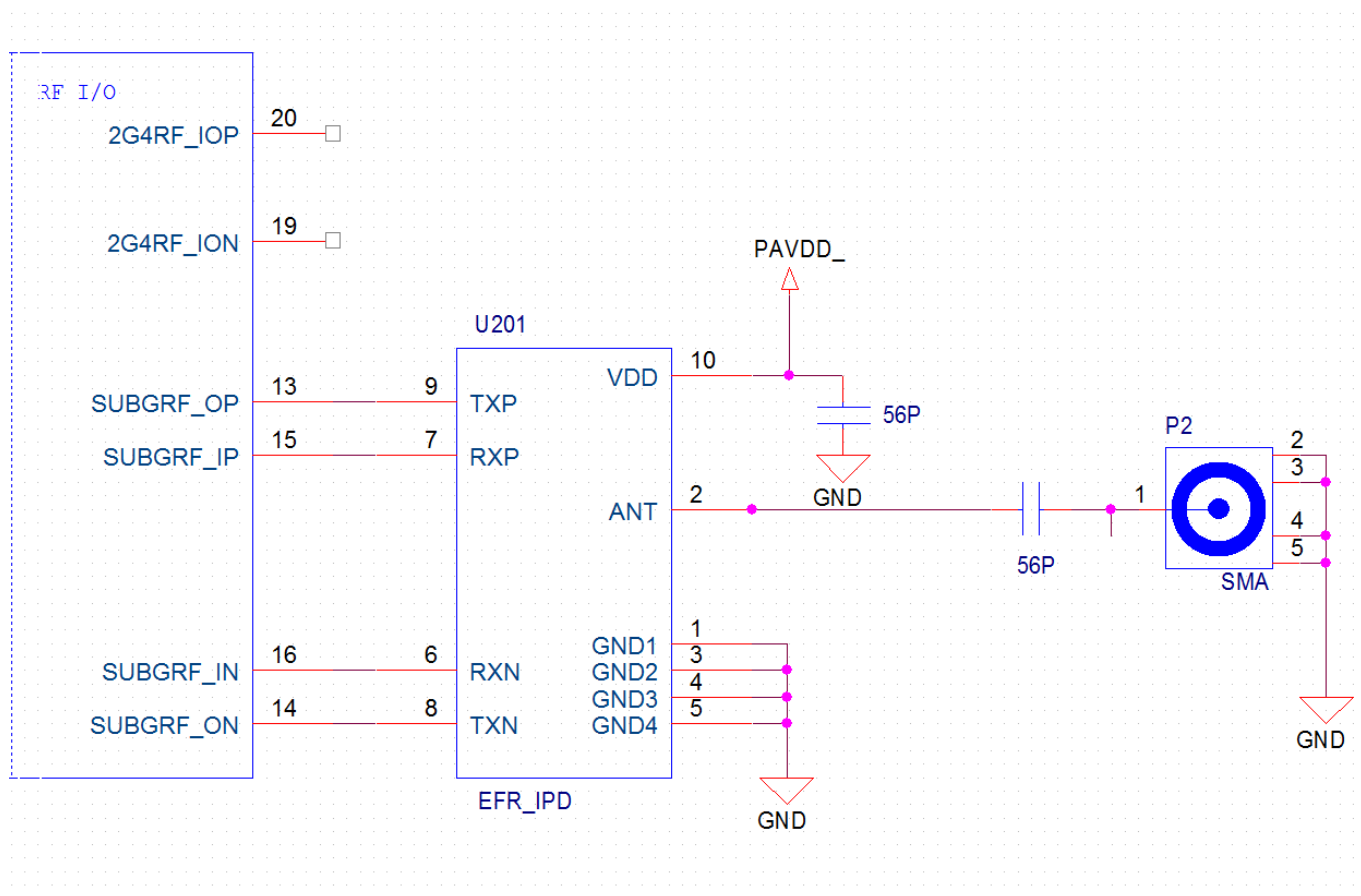


Figure 2.1. RF Section Reference Schematic

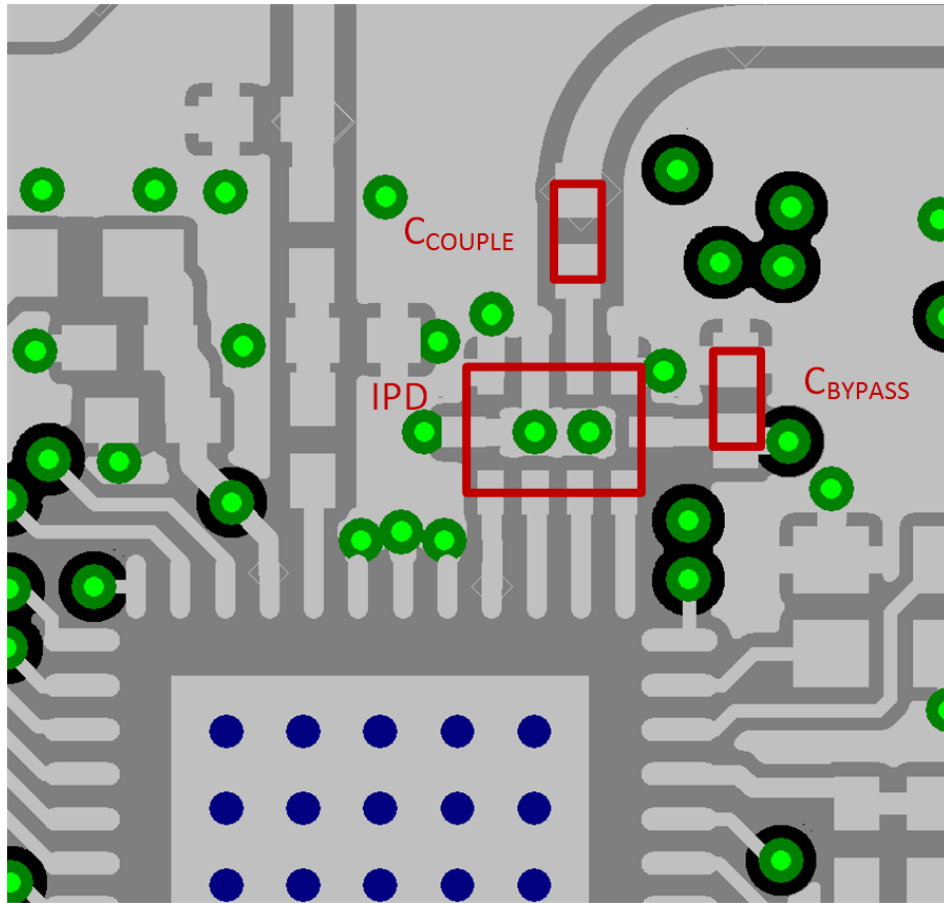


Figure 2.2. RF Section Reference Layout

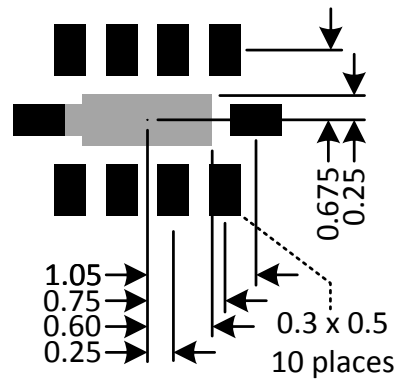


Figure 2.3. IPD Land Pattern

**Note:** Darker colors denote pads. Lighter colors denote recommended ground fill beneath the device. Pads 0.3 mm x 0.5 mm, 10 places.

## 2.2 Firmware/Software

As with the discrete design, there are a few firmware configuration items to consider when using the IPD, including:

- PA initialization: Includes VDDPA source, etc.
- PA dBm curve optimization: The dBm-based API input refers back to a curvefit to determine the correct PA device settings. This curve is slightly different for each match and should be optimized. As well, the offset value may be different for different RF front ends.
- PA tuning (sgpactune value): This is an internal tuning value, optimized for each matching network, supply voltage, and frequency. Optimal values have been determined by Silicon Labs and the IPD manufacturer and are listed in [Table 1.1 IPD Devices for EFR32 Series 1 on page 2](#).

Refer to the RAIL API programming literature for details on the API calls required to implement these items.

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