AN1104: Making Accurate PCIe Gen 4.0 Clock Jitter Measurements

The Si522xx family of clock generators and Si532xx buffers were designed to meet and exceed the requirements detailed in PCIe Gen 4.0 standards.

It is typical for standards to become more demanding as data rates increase. PCI-Express standards are no different, going from PCIe Gen3.1 where the jitter requirement is 1.0ps RMS to PCIe Gen4.0 where the jitter requirement is 0.5ps RMS. This application note will discuss the issues when measuring PCIe Gen 4.0 in time domain and the best practices to resolve them. By following the recommended methodology, results will provide accurate time domain results. The principles in this application can be applied to time domain jitter measurements for most clock based timing solutions including PCIe Gen1/2/3 measurements.

KEY POINTS

- Silicon Labs PCIe Clock Jitter Tool is an easy-to-use software for PCIe jitter measurements
- Even the best oscilloscopes contribute noise when making time based jitter measurements.
- Corrections to time domain jitter measurements can made using phase noise based measurements.

1. Introduction

PCIe Gen 4.0 clock jitter requirement is a more challenging 0.5 ps rms compared to the previous 1.0 ps rms Gen 3.1 requirement. This demanding jitter requirement requires an improvement in both PCIe clock source performance and a reduction in the test equipment jitter contribution. Improving test equipment may not be possible, and in this case the oscilloscope's jitter has to be determined then mathematically accounted for, resulting in a corrected and accurate Device Under Test (DUT) measurement value. As of the time of this writing, even the best oscilloscope will add excessive jitter to the measured results. Therefore, the second method of determining the scope jitter and subtracting it out is used for the most accurate value possible and is described in this application note.

The oscilloscope will introduce noise errors due to the input amplifier noise as well as the A/D clock quantization noise, which must be subtracted out. We must keep in mind that quantization noise is affected by the input slew rate which requires the oscilloscope noise to be characterized under each input slew rate, such as when analyzing DUTs having different performance. Additionally, oscilloscope settings must be fully optimized. Finally, hardware must be fully optimized as well, including Printed Circuit Board, layout, termination methodology, cable length matching, and power supply noise filtering.

The recommended best method is to first measure the DUT with a Phase Noise Analyzer, PNA. We'll use a Keysight E5052 in our example. Because the PNA will not lock to a signal with large modulation, the DUT spread spectrum feature must be turned off. The DUT time domain jitter is then measured with a high speed/low noise Digital Storage Oscilloscope (DSO). We'll use an Agilent DSA90804 in our example, again with the spread spectrum turned off. From these results. the oscilloscope jitter will then be calculated using the route of the subtraction of squares. Finally, the DUT's time domain jitter is measured with the spread spectrum turned on, and the final DUT jitter is calculated again using an RSS subtraction method.

2. PCIe Clock Timing Schemes, Jitter Measurement and Correction Methodology

PCIe has two different clock architectures which is fundamentally either a shared clock or independent clock scheme. The first is referred to as Common Clock Architecture where the transmit and receive sides share the same clock. See Figure 2.1 Common Clock Architecture on page 3. The second clock architecture involves two independent clocks which are referred to as Separate RefClk with no Spread Spectrum (SRNS) or Separate RefClk with Independent Spread Spectrum Clock (SRIS), in which there are separate reference clocks on the transmit side and on the receive side. See Figure 2.2 SRNS/SRIS Clock Architecture on page 3.

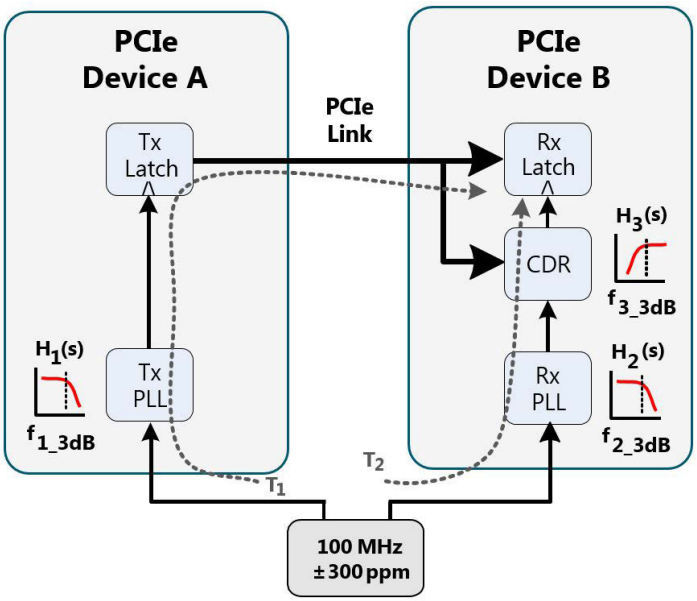

Figure 2.1. Common Clock Architecture

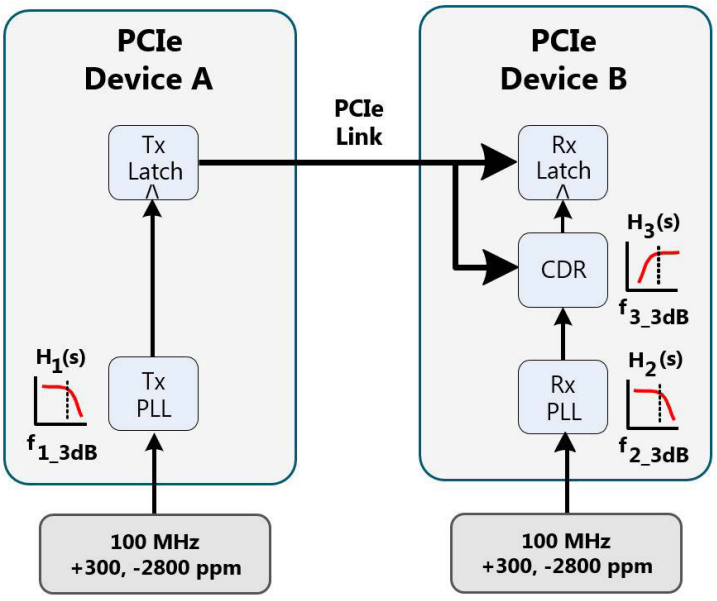

Figure 2.2. SRNS/SRIS Clock Architecture

The clock and data retiming section, CDR, includes a low pass filter function in both timing architectures. The CDR filter will track low frequencies and provide correct clock and data alignment, however, high frequencies will pass if prevalent cause eye closure. The key difference between the two is the noise in the Common Clock Architecture is a function of the transmit and receive PLL BW *differences*. Whereas in the SRNS/SRIS scheme the reference clocks are independent of each other and given their dominant jitter is random, then their combined impact on the system is the *root sum square of the individual terms*, resulting in higher overall jitter - potentially requiring lower clock noise solutions. SRNS/SRIS will also need to correct for the differences in clock accuracy between the transmit and receive sides, which can potentially degrade latency performance. The advantage of SRNS/SRIS methodology is it does not rely on clock sharing and thus clock transmission, simplifying design such as when the receive and transmit sections are in physically different locations.

It can be noted that there are 64 different filter combination schemes due to the various PCIe H1(s), H2(s) and H3(s) requirements and definitions. Calculating these, or even a single scheme, can be laborious. To alleviate this, Silicon Labs provides a PCIe Clock Jitter Tool which immensely simplifies this task, and can analyze either a phase noise measurement or a time domain measurement. This application note along with the PCIe Clock Jitter Tool should be used to correctly measure and determine PCIe reference clock and buffer jitter.

The two methods used when measuring PCIe jitter are time and phase domain, each having their own advantages and disadvantages but can provide highly accurate results when combined. A phase noise measurement is recognized as the most accurate tool to use when measuring low noise clocking sources such as crystal based oscillators, TCXO's and OCXO's. The disadvantage is PCIe reference clock phase noise can only be measured with the spread spectrum feature turned off.

Time domain oscilloscopes have the advantage of measuring jitter with the spread spectrum turned off or on. The issue with a time domain measurement is the relatively high noise floor of the instrument, on the order of -140 to -145 dBc vs. -170 to -180 dBc of a PNA. This oscilloscope performance limits the jitter accuracy when measuring low noise clocks.

However, highly accurate PCIe clock jitter can be provided by first collecting phase noise data with the SSC turned off, then time domain measurements with SSC turned off and then time domain measurements repeated with SSC turned on. Data collected can then be easily run through the PCIE Clock Jitter Tool and finally RSS subtraction is used to correct the DSO noise, resulting in accurate jitter measurements.

2.1 Phase Noise Measurement

Application specific phase noise test equipment has extremely low noise floors making them the choice for measuring low phase noise devices such as crystal based oscillators. A Keysight E5052B is used in the examples presented. Phase noise is measured over a range of offsets, as an example 100 Hz to 40 MHz offset for a 100.000 MHz PCIe reference clock shown below. In this example, the phase jitter integrated over 12 kHz to 20MHz with a 242.895 fs result. Data can be saved as a CSV file and then unfiltered phase jitter over any integration band can be calculated using Silicon Labs Phase Noise to Jitter calculator (https://www.silabs.com/tools/pages/phase-noise-jitter-calculator.aspx) or PCIe filtered phase jitter calculated using the Silicon Labs PCIe Jitter Tool (https://www.silabs.com/products/timing/pci-express-learning-center). It should be noted that the PCIe Clock Jitter Tool expects the PNA .csv file to extend from 10 kHz to 50 MHz as this is the PCI-SIG mandated integration range. The user must ensure this range is included in the .csv file, extrapolating where necessary.

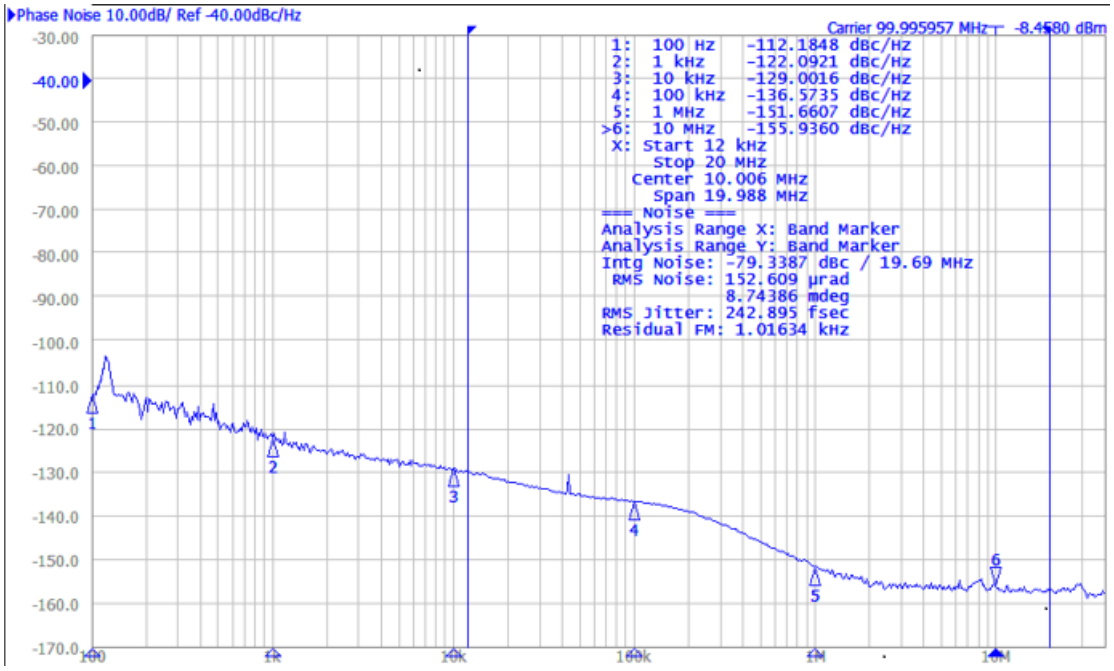

Figure 2.3. PCIe Clock Phase Noise Plot

Phase noise is measured at about 0.2 % increments of the offset range. The phase noise power is calculated for each of these discrete frequency bins, resulting in a bin value. The bin value is a magnitude value only with no phase information, whereas a Fast Fourier Transform, FFT, translation of a time domain measurement contains magnitude and phase. See the figure below. It should be noted that integrating a phase noise based magnitude only, I A' - F' I, is always larger than an equivalent time domain based magnitude plus phase measurement, I A – F I. Therefore, the phase noise based jitter measurement; a magnitude only measurement, is a conservative and legitimate method to use when measuring clock jitter.

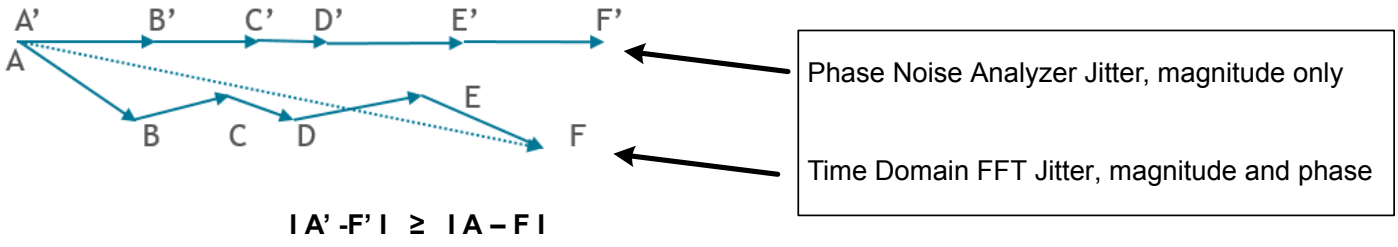

Figure 2.4. Jitter Analysis

The PCIe Clock Jitter Tool will apply the appropriate PCIe filters to a phase noise based measurement providing the required jitter values. Below is an example of various Gen 4.0 filters applied to a reference clock from Si52204-A01AGM using a phase noise measurement and Silicon Labs PCIe Clock Jitter Tool. The PCIe Clock Jitter Tool can calculate time domain jitter with GEN 4.0 filters applied as well.

Table 2.1. Jitter Based on a Phase Noise Measurement using SiLabs PCIe Clock Jitter Tool

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak	Specification			Analysis Result			Compli-ance Result
											HF RMS	LF RMS	Pk-Pk	HF RMS	LF RMS	Pk-Pk	
1	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	500 fs			72.23 fs	20.11 fs	N/A	PASS
2	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	2 dB	2 MHz	0.01 dB	10 MHz	0 dB	500 fs			153.86 fs	111.73 fs	N/A	PASS
3	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB	500 fs			182.93 fs	45.75 fs	N/A	PASS
4	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	2 dB	2 MHz	0.01 dB	10 MHz	0 dB	500 fs			206.63 fs	112.45 fs	N/A	PASS
5	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	0.01 dB	2 MHz	1 dB	10 MHz	0 dB	500 fs			103.76 fs	37.96 fs	N/A	PASS
6	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	2 dB	2 MHz	1 dB	10 MHz	0 dB	500 fs			102.85 fs	66.53 fs	N/A	PASS
7	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	0.01 dB	2 MHz	1 dB	10 MHz	0 dB	500 fs			217.70 fs	74.55 fs	N/A	PASS
8	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	2 dB	2 MHz	1 dB	10 MHz	0 dB	500 fs			234.87 fs	120.87 fs	N/A	PASS
9	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	500 fs			222.54 fs	98.24 fs	N/A	PASS
10	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	2 dB	5 MHz	0.01 dB	10 MHz	0 dB	500 fs			298.06 fs	170.06 fs	N/A	PASS
11	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	500 fs			162.26 fs	36.40 fs	N/A	PASS
12	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	2 dB	5 MHz	0.01 dB	10 MHz	0 dB	500 fs			219.27 fs	68.43 fs	N/A	PASS
13	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	0.01 dB	5 MHz	1 dB	10 MHz	0 dB	500 fs			228.26 fs	127.77 fs	N/A	PASS
14	GEN4	16 Gb/s	Common Clock	4.0	2 MHz	2 dB	5 MHz	1 dB	10 MHz	0 dB	500 fs			300.21 fs	182.22 fs	N/A	PASS
15	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	0.01 dB	5 MHz	1 dB	10 MHz	0 dB	500 fs			151.39 fs	63.80	N/A	PASS
16	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	2 dB	5 MHz	1 dB	10 MHz	0 dB	500 fs			177.60 fs	40.41 fs	N/A	PASS

2.2 Oscilloscope Noise Measurement and Correction

A digital oscilloscope (DSO) is required to measure jitter on a PCIe reference clock with the spread spectrum turned on, however oscilloscope noise can be on the order of -142 dBc, well above the performance of a today's clock generators and buffers. Phase jitter measurements as described in the previous section can be used to correct the DSO's noise by measuring the PCIe reference clock with the spread spectrum feature disabled. The equation below is used to calculate the DSO's jitter noise.

$$J_{DSO} = \text{Square Root} (J_{DSO\_SpreadOff}^2 - J_{PhaseNoise}^2)$$

Equation 1. DSO Noise Formula

The PCIe Clock Jitter with the spread turned on, is then corrected using the formula below, after measurements are made:

$$J_{PCIeClock} = \text{Square Root} (J_{DSO\_SpreadOn}^2 - J_{DSO}^2)$$

Equation 2. PCIe Clock Correction Formula

It should be noted that a DSO additive noise is dominated by two factors: the input amplifier noise and the A/D's sample clock jitter. The DSO's A/D sample clock jitter is approximately constant; however, the input amplified noise is slew rate dependent, and thus also set-up and DUT dependent. The application use - load, termination length, etc. - must be replicated as close to the actual use conditions as possible and the DUT of interest must be measured. If devices with various output slew rates need to be compared, then JDSO_Spreadoff needs to measured and JDSO calculated for each slew rate/test condition. It is not advised to use a single JDSO value for various devices and test conditions. The equation below is not used in measuring or determining a DSO jitter, rather demonstrates the DSO's dominating noise contributing factors.

$$\text{DSO Jitter} = \text{Square Root} (\text{AmplifierNoise}^2_{\text{(input slew rate dependent)}} + \text{A/D Sample Clock Jitter}^2)$$

Equation 3. Dominating DSO Noise Contributors

2.3 Jitter Correction Example

The following is an example of a Corrected PCIe Clock Jitter Measurement

The first step is to measure the phase noise of the DUT, with the spread spectrum turned off, and in this example the results are shown in Figure 2.3 PCIe Clock Phase Noise Plot on page 4. The phase noise results are also saved as a csv and imported when using PCIe Clock Jitter Tool. Figure 2.5 Filtered and Unfiltered Jitter Based on a Phase Noise Measurement, Spread Off on page 7 shows the Unfiltered and PCIe Filtered jitter results for one of the H1(s) and H2(s) filter combinations versus offset frequency for the phase noise based measurement. This filter combination was known to give the worst case SSon jitter value based on the DSO results.

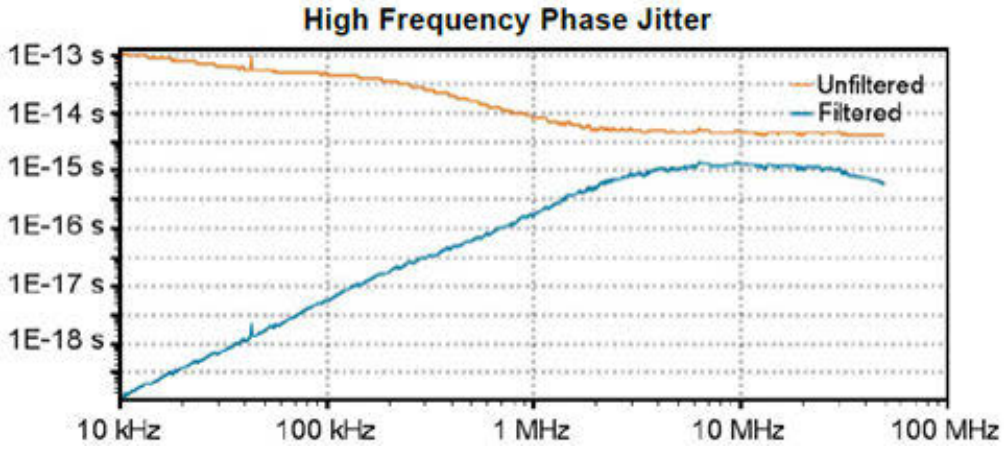

Figure 2.5. Filtered and Unfiltered Jitter Based on a Phase Noise Measurement, Spread Off

The DUT is then measured with the spread off using a DSO, in this case with a Keysight DSA90804A. The PCIe Clock Jitter Tool is used to calculate the PCIe Filtered jitter with results shown in the figure below.

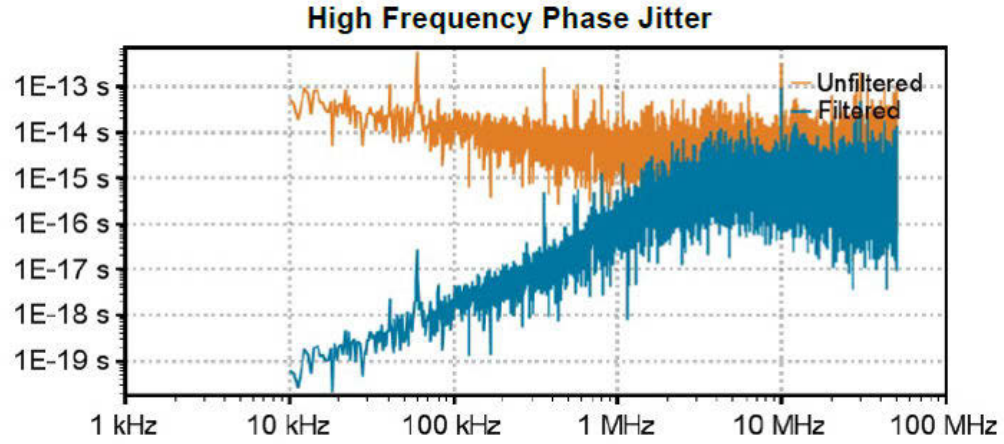

Figure 2.6. Filtered and Unfiltered Phase Noise Based on a DSO Measurement, Spread Off

The phase noise based measurement results in 0.05 ps rms when selecting a 4 MHz /2 dB, 5 MHz/0.1 dB filter.

The DSO based measurement results in 0.28 ps rms when selecting a 4 MHz /2 dB, 5 MHz/0.1 dB filter.

The DSO scope noise is determined to be 0.27 ps rms, using the equation below.

$$DSO\ Jitter = Sqrt\ (0.28^2 - 0.05^2) = 0.27\ ps$$

The DUT Spread Spectrum feature is enabled and a DSO measurement is made. The figure below shows the filtered and unfiltered phase noise verses frequency using the PCIe Clock Jitter Tool.

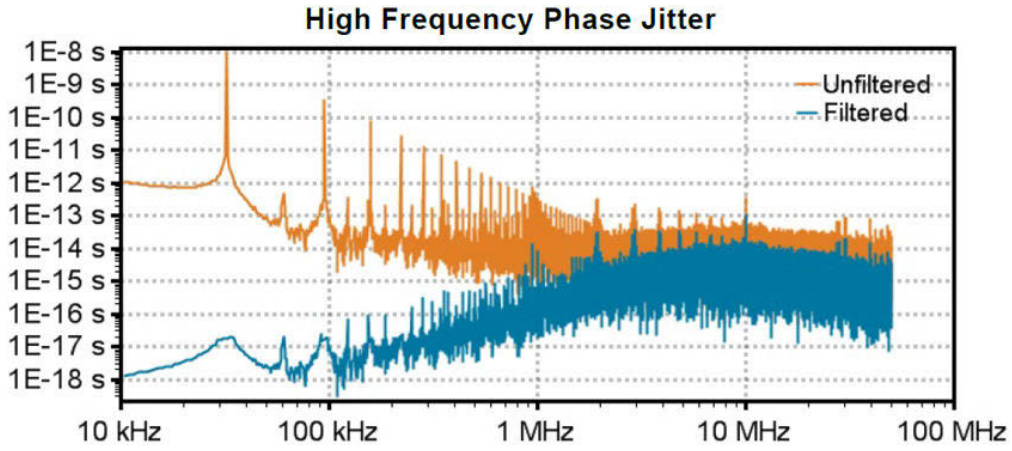

Figure 2.7. Filtered and Unfiltered Jitter Based on a DSO Measurement, Spread On

The DUT PCIe reference clock with spread spectrum enabled based on the DSO measurement results in 0.39 ps rms worst case for the 4 MHz/2 dB, 5 MHz/0.1 dB filter. Using the 0.27 ps correction factor *for the same filter combination* and the equation below results in 0.28 ps actual DUT performance.

$$\textit{Correct DUT Jitter} = \sqrt{(0.39^2 - 0.27^2)} = 0.28 \text{ ps}$$

The figure below shows that an example -143 dBc noise floor results in 0.27 ps rms of integrated jitter using the same 4 MHz/2 dB, 5 MH/0.1 dB filter which is in line with the Keysight DSA90804A DSO specifications.

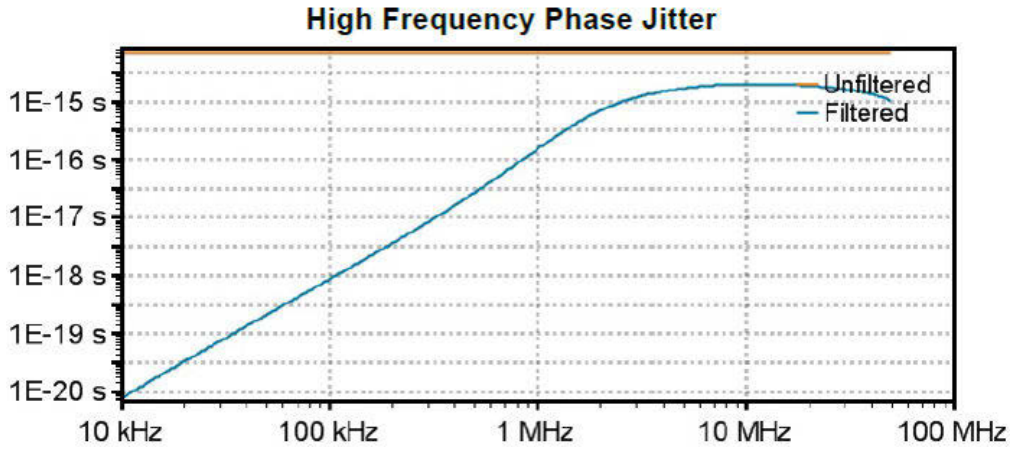

Figure 2.8. Filtered and Unfiltered DSO Jitter

This example shows uncorrected DUT performance of 390 fs versus a 280 fs corrected value. This difference can cause a false failure, and it's advised to use DSO noise correction when making GEN 4.0 measurements. This same correction methodology can be applied to any high-performance clock measurement.

3. Conclusions

The most accurate time domain jitter measurements will result when:

1. Optimizing hardware set up.
2. Optimizing test equipment settings.
3. Measure phase noise with the spread spectrum turned off, add estimated readings out to 50 MHz offset as needed.
4. Measure time domain jitter with the spread spectrum turned off with applicable DUT slew rate plus load.
5. Measure time domain jitter with the spread spectrum turned on with applicable DUT slew rate plus load.
6. Calculate test equipment contributed noise by RSS subtracting the results from steps 3 and 4.
7. Calculate DUT performance by RSS subtracting the results from steps 5 and 6.

If you have questions about the information described in this document, please contact support at https://www.silabs.com/support.

To download Silicon Labs PCIe Clock Jitter Tool, visit this site: https://www.silabs.com/products/timing/pci-express-learning-center

4. References

"Refclk Fanout Best Practices for 8GT/s and 16GT/s Systems," G. Richmond, Silicon Labs, presented at PCI-SIG Developers Conference (June 7, 2017) in Santa Clara, CA.

“Removing Oscilloscope Noise from RMS Jitter Measurements” G Giust and F Benford, Jitter Labs (July 26, 2017)

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