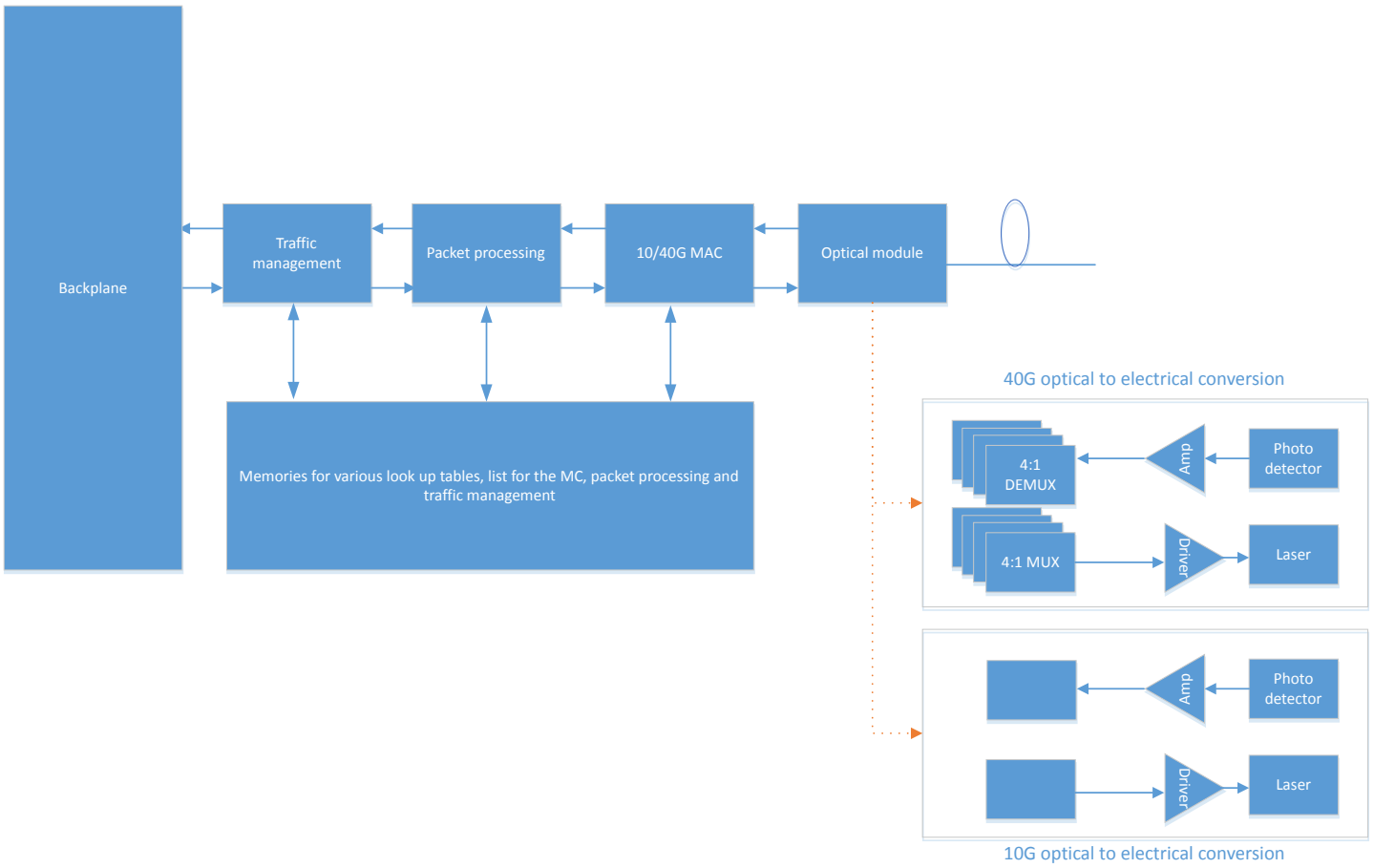
AN1106: Optimizing Jitter in 10G/40G Data Center Applications

This application note outlines the common reference clock frequencies that would be required in many systems along with an analysis for the jitter requirements for each of these frequencies. It also shows how the Si5332 could fit as the ideal clock-tree-in-a-chip solution for 10G/40G line card designs.

KEY POINTS

- Si5332 clocking solutions for 10/40G data centers
- Si5332 clock-tree scaling benefits
- Si5332 excellent jitter performance



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1. Introduction

Data center designs inherently comprise servers and storage arrays. However, the communication within the datacenter system and with the external world is driven by two inter-dependent needs:

1. Increase communication speeds
2. Support all (or at least mostly all) different communication links

The implementation of optical links, along with (or in many advanced designs, “as”) Ethernet and Storage area network fabrics, drives both the need to increase communication speeds and to embrace optical communication links. The adoption of such optical links poses challenges to datacenter design both for server and storage arrays, namely, the need to support an optical-electrical-optical transceiver design and the associated electrical design to support ever faster data rates.

The need to design these new sub-systems and ensure compatibility with other sub-systems in a server or a storage array design boils down to specific challenges in clock-tree designs. This application note aims to introduce a powerful, single-chip solution to these challenges: the Si5332.

The following take-aways set up the clock-tree design definition for such line cards:

1. The 40G system is a 4X parallel implementation of a 10G system.
2. Apart from the jitter attenuation needed at the optical module and MAC levels, there is a need for an accurate and low-noise reference clocks for traffic management and for packet processing.
3. There is also the need for reference clocks to run the interfaces between the different sub-systems and the memories that house look-up tables, lists, and so on for the sub-systems.
4. The backplane to the line card interface could potentially have Ethernet communication links and PCIe links.

The remaining parts of this document outline the common reference clock frequencies required in many systems as well as provide an analysis for the jitter requirements for each of these frequencies. It also shows how the Si5332 could fit as the ideal clock-tree-in-a-chip solution for 10G/40G line card designs.

2. Common Frequencies and Requirements for 10G/40G Line Cards

The table below shows the different clock frequencies that can be used in 10G/40G line cards and the specifications for each frequency.

Table 2.1. Reference Clock Frequencies and Jitter Specifications

Protocol/ System	Clock frequency (MHz)	Jitter specification (fs)
10GbE/40GbE	161.1328125	350
	322.265625	350
	257.8125	350
SerDes reference clocks	125	350
	150	350
	156.25	350
	312.5	350
PCIe	100	500
System reference clocks	100	5000
	125	5000
	133.33	5000
	266.67	5000

The basis for 10G/40G jitter specification:

All 10G/40G systems typically have data rates of 10.3125 GBPS. This translates to a unit interval of 96.97 ps. Assuming a 10% budget for jitter for an acceptable “eye-opening” and 50% budget for reference clock jitter and a BER of 1e-12, the RMS jitter budget is 346.32 fs or ~350 fs.

The basis for PCIe clock jitter:

The PCIe clock jitter specification varies greatly over PCIe generations. The latest PCIe gen4 (usually needed for systems to match the data speeds of 10G/40G links) high-frequency jitter specification is 500 fs. To add to this specification's needs, PCIe systems usually need to support spread spectrum clocking as an option and still be able to meet the high-frequency jitter specification.

The basis for System reference clocks jitter:

Memories and digital systems in the sub-blocks (shown on the cover page) need precision clocks but can usually tolerate jitter of ~5 ps RMS. The typical specifications for such systems are about 100 ps max period (and/or cycle-cycle jitter). Clock jitter of up to 5 ps RMS is usually acceptable assuming that these systems also need a BER of 1e-12.

3. Jitter Performance

The 12-output Si5332 (shown in the figure below) is ideal for 10G/40G line cards. It will satisfy the jitter requirements and also provide four independent clocks needed for each domain as listed in the requirements. See Chapter 2. Common Frequencies and Requirements for 10G/40G Line Cards.

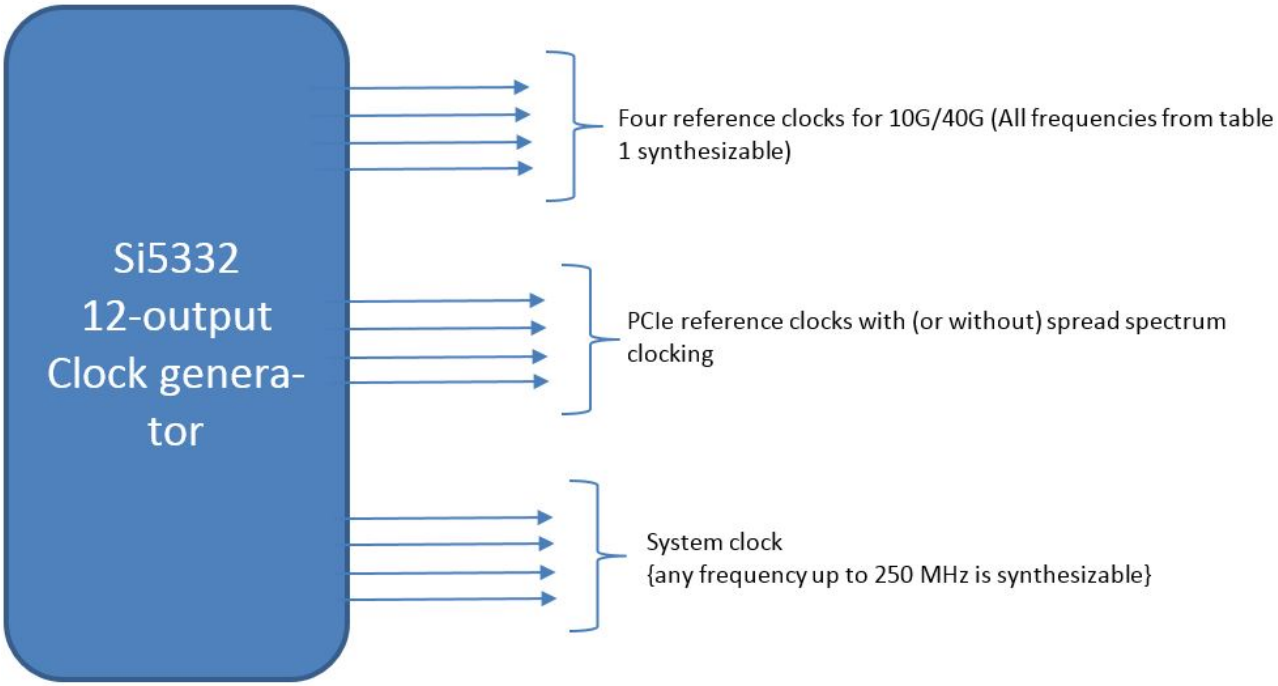


Figure 3.1. Clock-Tree-In-A-Chip Solution

Si5332 jitter performance for 10G/40G systems:

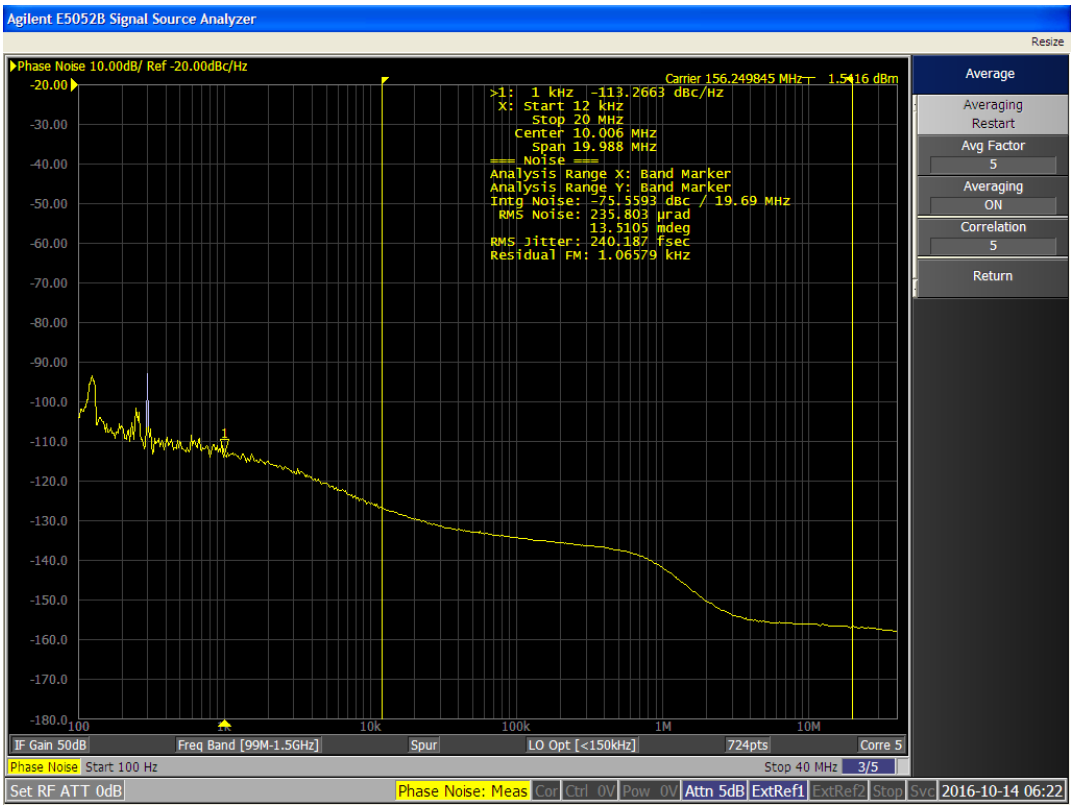


Figure 3.2. 156.25 MHz Phase Noise Plot

The Si5332 RMS jitter in the 12K-20MHz band is ~250 fs with 25 MHz crystal references. It can be as low as 175 fs when 50 MHz crystal references are used. Hence, the jitter margin provided by Si5332 for 10G/40G systems are about 30-50%. Note that 322.265625 MHz outputs need to be generated using Si5340 or Si5341 as the Si5332 cannot support output frequencies greater than 312.5 MHz.

Jitter performance PCIe gen 4:

The Si5332 100 MHz clock was tested for PCIe jitter and can meet the PCIe specifications with at least 40% margin to up to 90% margin depeding on the PCIe gen jitter that is being measured. For PCIe gen 4, a clock with spread spectrum clocking off can provide about 90% margin with respect to the 0.5 ps high frequency jitter specs, thereby offering almost all the jitter budget to the system (i.e., deterministic jitter in the high-speed links in the PCIe ser-des system).

#	Class	Data Rate	Architecture	Specs	PLL1 BW	PLL1 Pk	PLL2 BW	PLL2 PK	CDR BW	CDR PK	Delay	SSC Separation
37	GEN4	16 Gb/s	Common Clock	4.0	4 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB	12 ns	On (1)

Test	Specification	Analysis Result	Compliance Result
Refclk HF RMS Jitter	1 ps	54.691 fs	PASS
Refclk LF RMS Jitter		0.932 fs	N/A

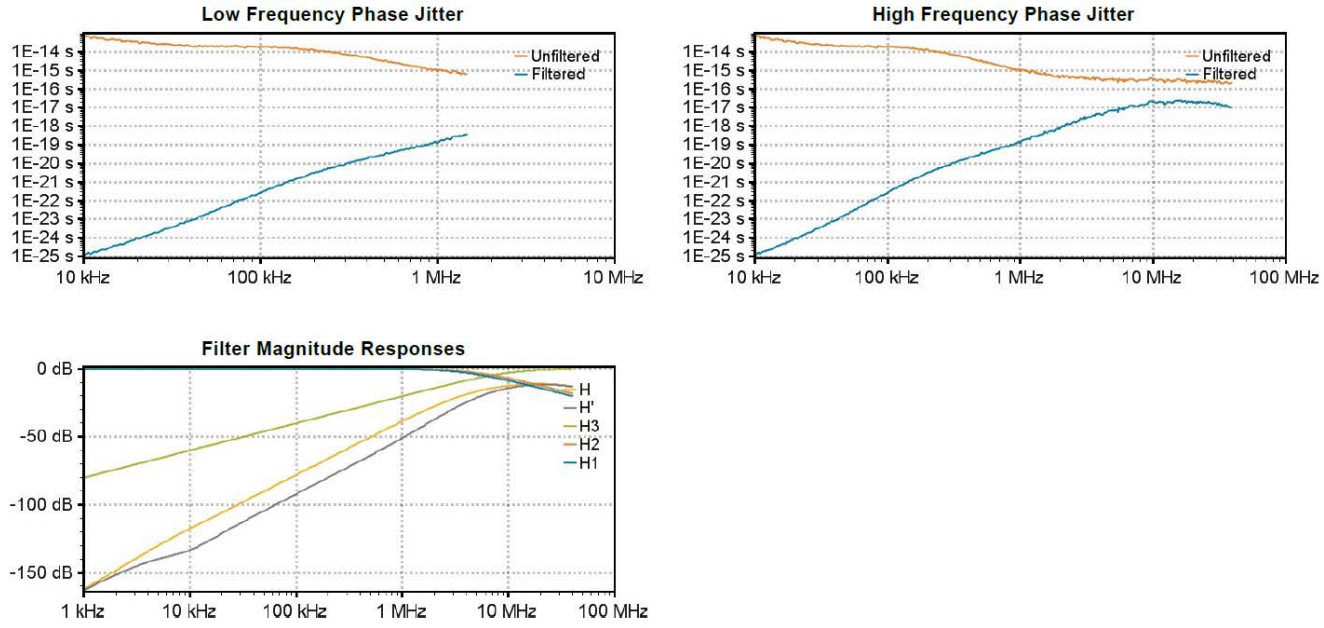


Figure 3.3. A Snippet of the PCIe Gen4 Testing for Si5332 Clocks (no SSC)

Jitter performance System clocks:

The jitter for CMOS clocks is less than 1ps (usually in the 250 fs range) and, therefore, the Si5332 are about 5X better than the specifications for system clocks and can be considered “near ideal” for digital system reference clocking. The following figure shows the phase noise plot for a 3.3V CMOS clock with a frequency of 208.33MHz as an example.

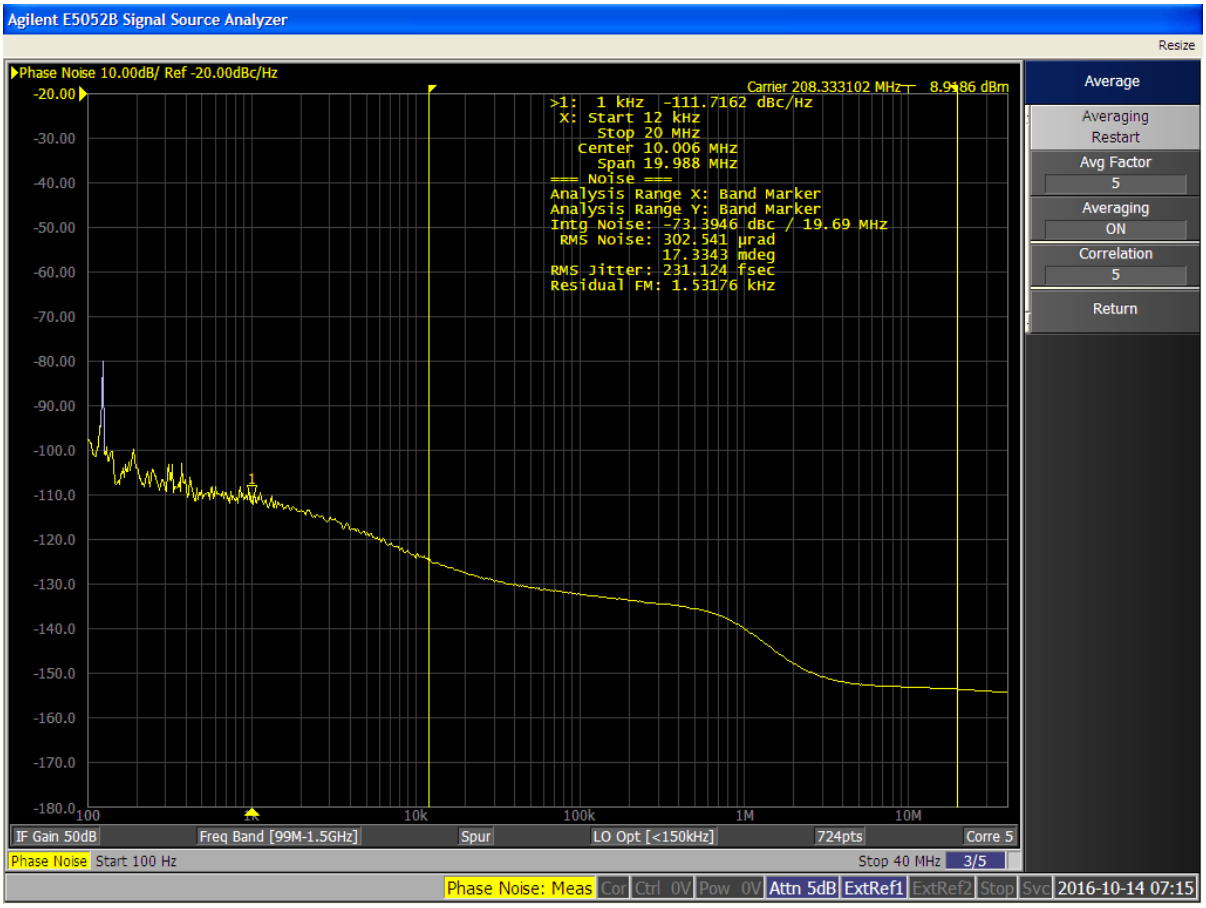
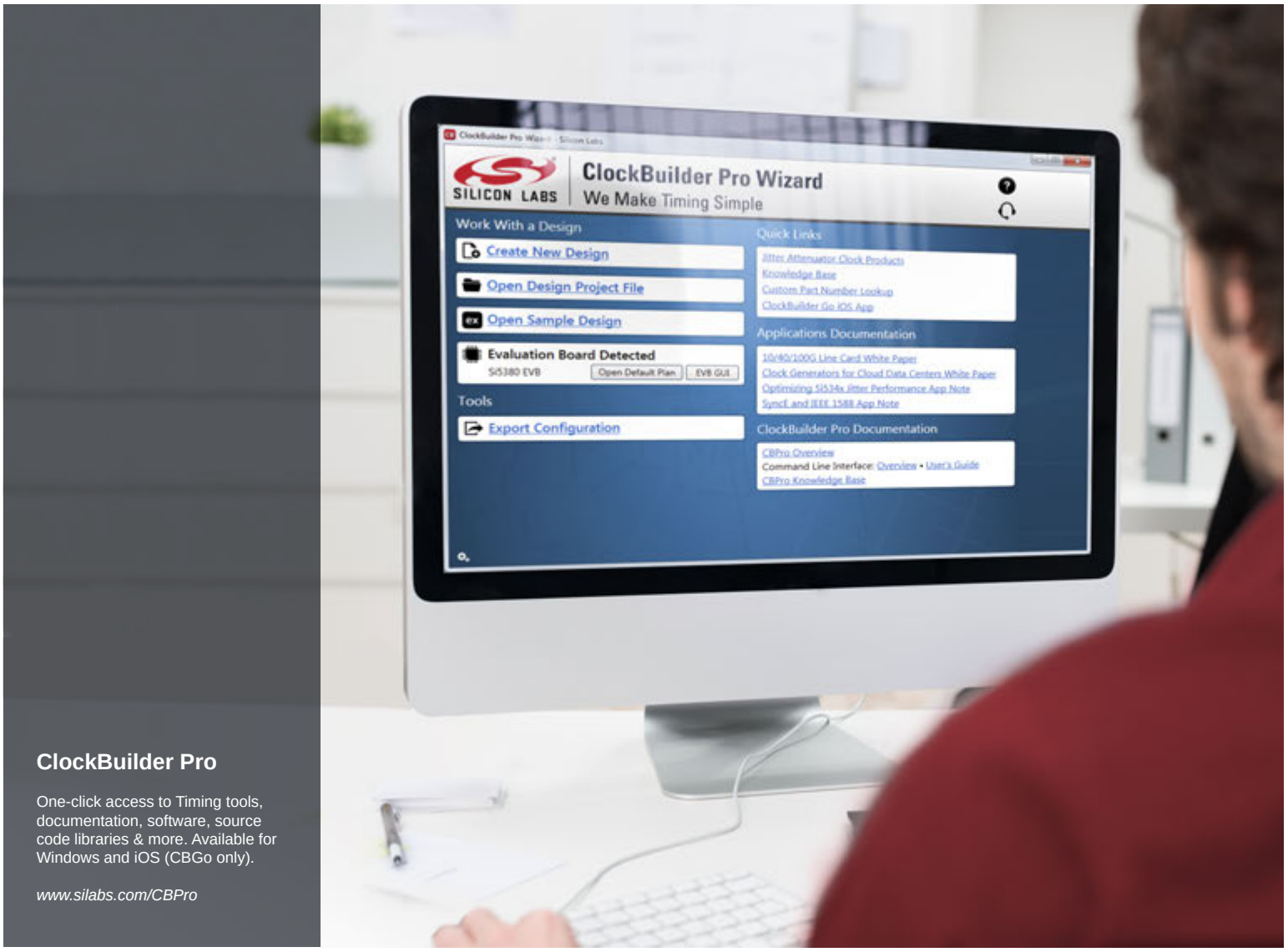


Figure 3.4. 208.33 MHz CMOS Clock Phase Noise Plot

4. Conclusion

The 10/40G line cards for data center clocks need varied clocking solutions for different systems. There is also a benefit in using the same clock tree with scaling for a 10G system vs a 40G system. The Si5332 fits this need best by virtue of its excellent jitter performance (provides about 30-90% margin with respect to all the different jitter specifications) and by virtue of being a 12-output any-frequency clock generator. The Si5332 is a great fit not just for current datacenter designs but is also a future proof clock solutions for rapidly evolving datacenter clocking needs.



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