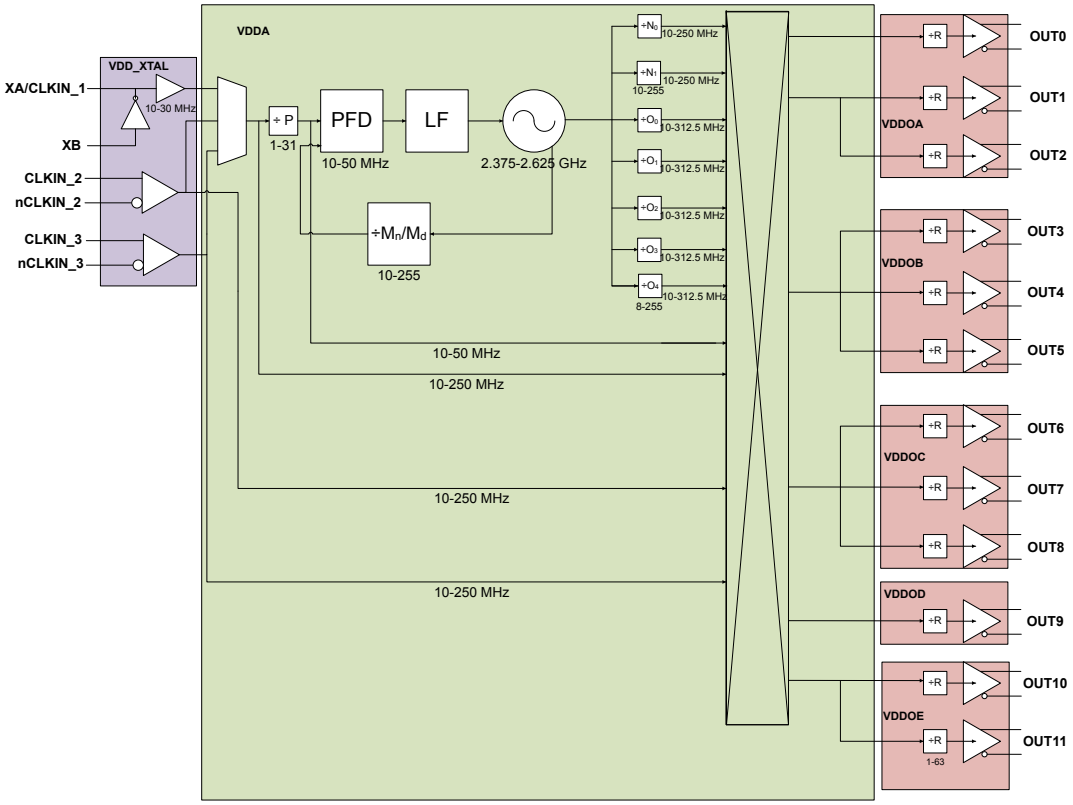
AN1108: Advanced Features Guide for Si5332

The family reference manual covers the fundamental problem of deriving output frequencies from a given input reference to the Si5332 PLL. The family reference manual also lists all the register fields to control all aspects of the Si5332, but not all of the fields are described in the family reference manual. This application note covers other programming options for the Si5332 that can allow the user to exploit the flexibility offered by the Si5332 architecture.

KEY POINTS

- Si5332 Programming Delay
- Single-Chip Clock Tree
- Low-Frequency Outputs



1. Programming Delay in the Si5332

Delay programming is useful for the following reasons:

1. It can be used to de-skew the delay between two outputs as shown in Fig 1.1.
2. It can be used to create a set of “multi-phase” output clocks that are useful in applications, such as switching regular reference clock high-speed digital systems that use multiphase clocks to increase data rates as shown in Fig 1.2.
3. It can be used to program delays on a clock line to compensate for PCB trace delays as shown in Fig 1.3.

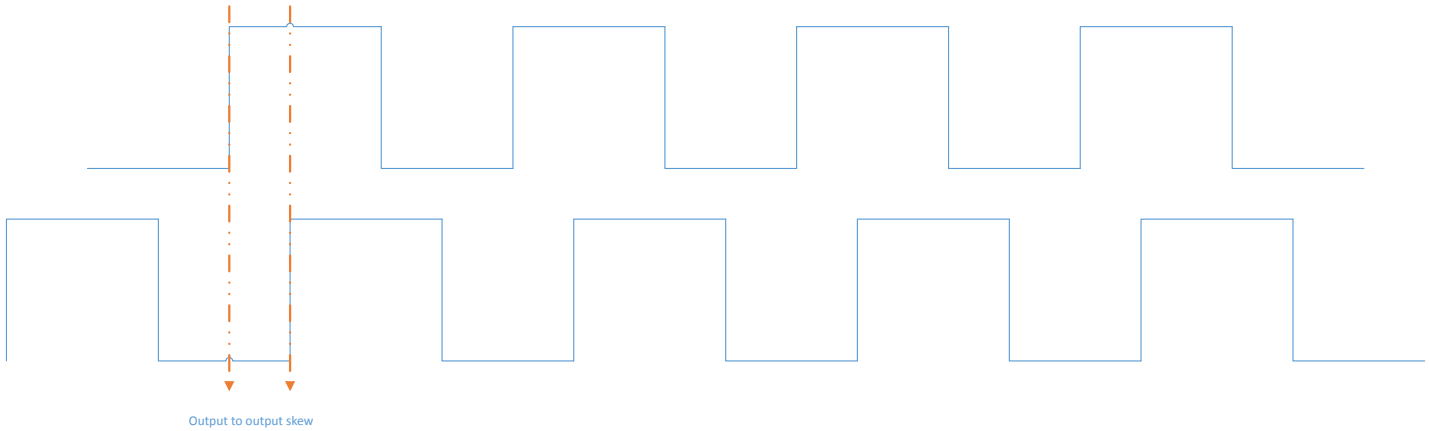


Figure 1.1. Skew Between Output Clocks

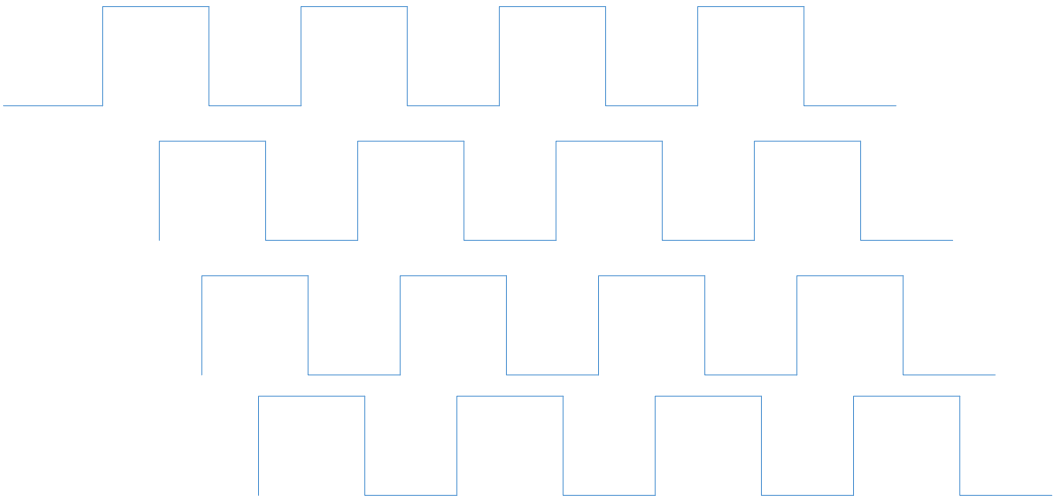


Figure 1.2. Four Multi-phase Output Clock with a Phase Offset of Multiples of π/2

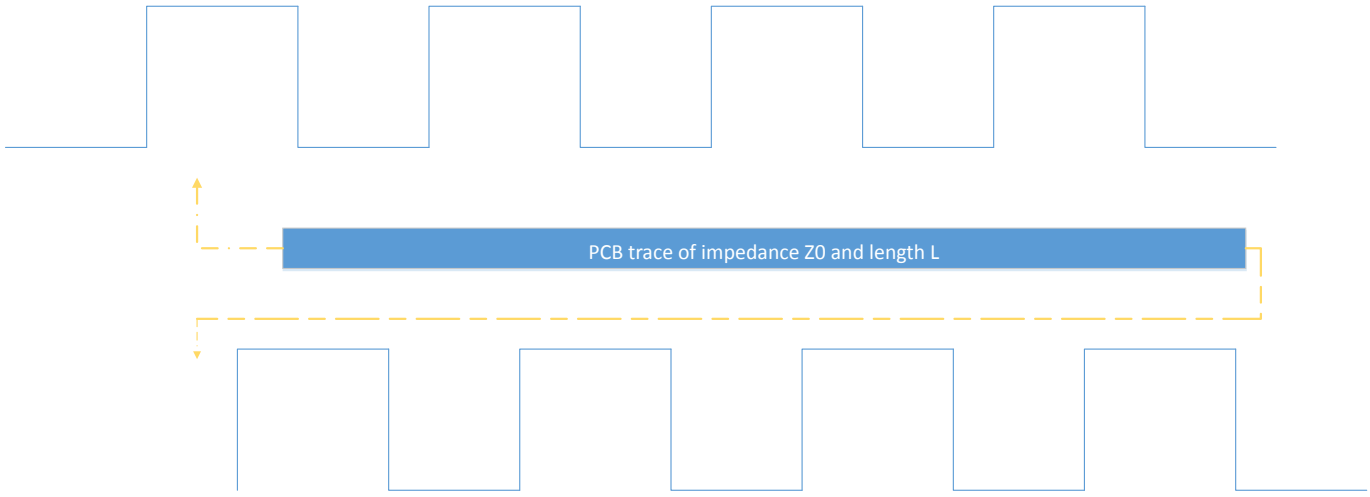


Figure 1.3. Delays Due to PCB Traces

Each programming delay need uses the same single programming tool available to the user. Programming a static phase delay on the output clock is accomplished by setting the OUTx_SKEW register (please refer to the family reference manual for actual register address details). The skew is programable in steps of 35 ps and is an 8-bit register field, i.e., the overall delay can be as high as 8.925 ns. Please note that the Si5332 only supports positive delay programming. However, in many cases, a negative delay can be realized as a 2π+ delay.

2. Clock Tree on a Chip

The Si5332 crossbar multiplexer can be used to set up an entire clock tree on a single Si5332. Consider the clock tree requirement shown in the following figure.

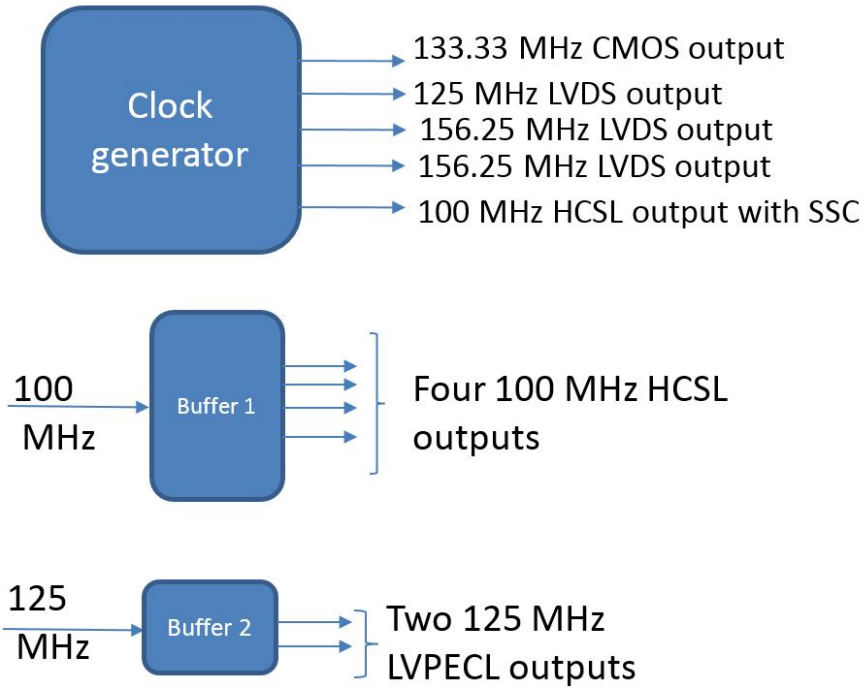


Figure 2.1. Typical Clock Tree Requirement

In such a clock tree requirement, clock generators usually have limitations on generating spread-spectrum clock and/or fractional synthesis. Even if that is satisfied the buffers usually need separate ICs. The Si5332 provides an elegant way of generating all the above needs in a single chip. This flexibility is made possible by the output crossbar multiplexer architecture, as shown below in Figure 2.2 Si5332 Solution for Clock Chip on Tree Requirement on page 5 (please refer to the block diagram to view the full flexibility of the cross-bar multiplexer). This programming flexibility is achieved by setting the following register bit fields:

1. Synthesize all the “clock generator” outputs from the crystal input. Refer to the algorithm listed in the Si5332 family reference manual for solving frequency plan needs like these (set output mux registers OMUX0–OMUX4 to reference the clock generator output frequencies).
2. Set the OMUX4 to reference the 100 MHz input clock by setting OMUX4_SEL0 to 2 and OMUX4_SEL1 to 7.
3. Set the OMUX5 to reference the 125 MHz input clock by setting OMUX5_SEL0 to 3 and OMUX4_SEL1 to 7.

This sets the output mux, and now, each output clock, OUTx, needs to be programmed to reference the correct OMUXy in order to realize the entire clock tree on a single chip. As can be seen, using a single IC has benefits in reduced BOM cost, power, and area for the system board.

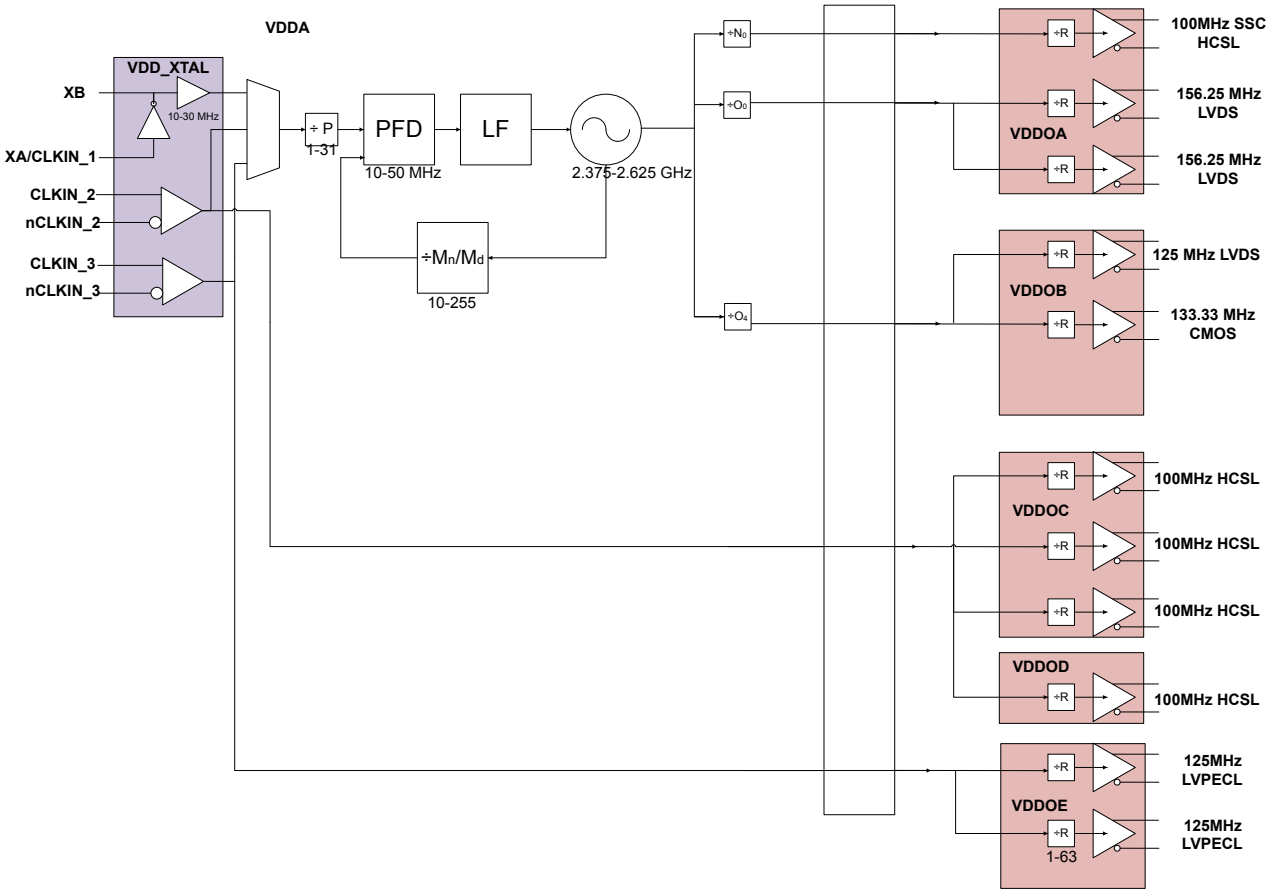


Figure 2.2. Si5332 Solution for Clock Chip on Tree Requirement

3. Generating Low Frequencies

The Si5332 divider values limit the output frequencies to as low as 5 MHz but not lower. However, the output cross point mux provides a unique architecture in which the dividers can be cascaded. This cascading allows the user to generate ultra-low frequencies in certain unique applications. For example, if a user needs to generate a 32.768 kHz clock for RTC applications, the Si5332 can be used as shown in the figure below. The register programming is the same as that described in 1. Programming Delay in the Si5332. Take OUT9 and connect it to CLKIN2, and choose the OMUX to drive OUT10 as a divider output from CLKIN2. In this case, set OUT9 to 2.064384 MHz, and then cascade it to the R-divider of OUT10 to divide it down to 32.768 kHz. At the cost of an extra output, a single chip can be used to generate the RTC clock along with other frequencies.

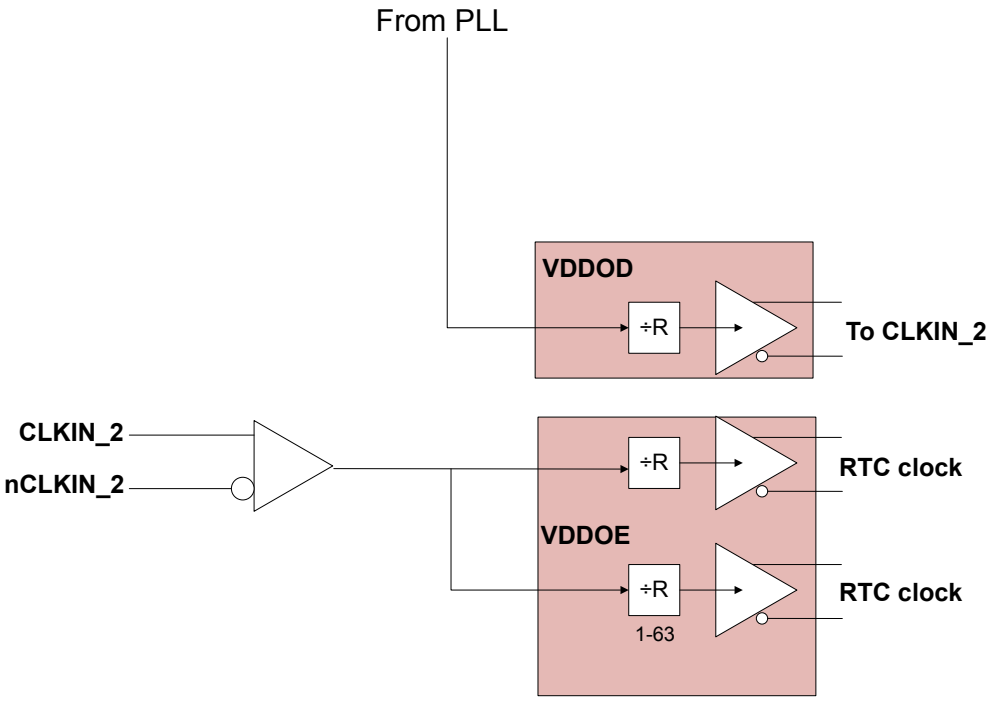


Figure 3.1. Cascading Dividers to Generate Low Frequency Clock Outputs

4. Conclusion

The Si5332 is a versatile clock generator that can support features generally not available on other clock generators,including clock tree on a chip, generation of low frequencies by cascading dividers, and programming delay to offset for PCB skew. This application note provides a guide to programming these features.

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