AN1110: Spread Spectrum Configuration Capability in Si5332

All electronic products need to go through EMI compliance testing. Most of the EMI in electronic systems is caused by clocks. Hence, it is important that system designers ensure that clocks do not cause EMI compliance problems. The Si5332 provides three options for EMI reduction and hence compliance:

1. Differential signaling (over CMOS signaling)
2. Slew rate control (for CMOS signaling)
3. Spread spectrum clocking (for EMI reduction)

Traditional electronic systems are mostly needed to design for just EMI compliance. Modern electronic systems can house may wireless circuits (especially systems designed for consumer applications like a mobile phone, a digital still camera, etc.) and hence also need to design for reducing interference inside the system, such as reducing near-field interference, typically at frequencies greater than 800 MHz. Methods 1 and 2 in the list above are especially useful for reducing “radio frequency interference” or RFI.

KEY FEATURES OR KEY POINTS

- Spread spectrum clocking
- Slew rate control for CMOS drivers
- Differential signaling

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1. Differential Signaling

Differential signaling is a powerful method for reducing EMI and RFI. However, the “cost” of differential signaling is the use of an extra signal and a higher static power consumption. The figure below compares the EMI of the fundamental harmonic of a 100 MHz clock for a single-ended clock and a differential clock.

Figure 1.1. EMI Single-ended (SE) Clock vs Differential (Diff) Clock

Figure 1.2 RMI Single-ended (SE) Clock vs Differential (Diff) Clock on page 3 compares the radio frequency interference (RFI) in the 800MHz – 1 GHz band. The RFI is caused by the harmonics of a clock frequency. There is a direct tradeoff between signal integrity (rise/fall times of clock) and the RFI from a clock. We would ideally need the rise/fall times to be as small as possible, but this requirement increases the “high” frequency harmonic content in the clock and therefore interferes with RF transceiver functions in the system.

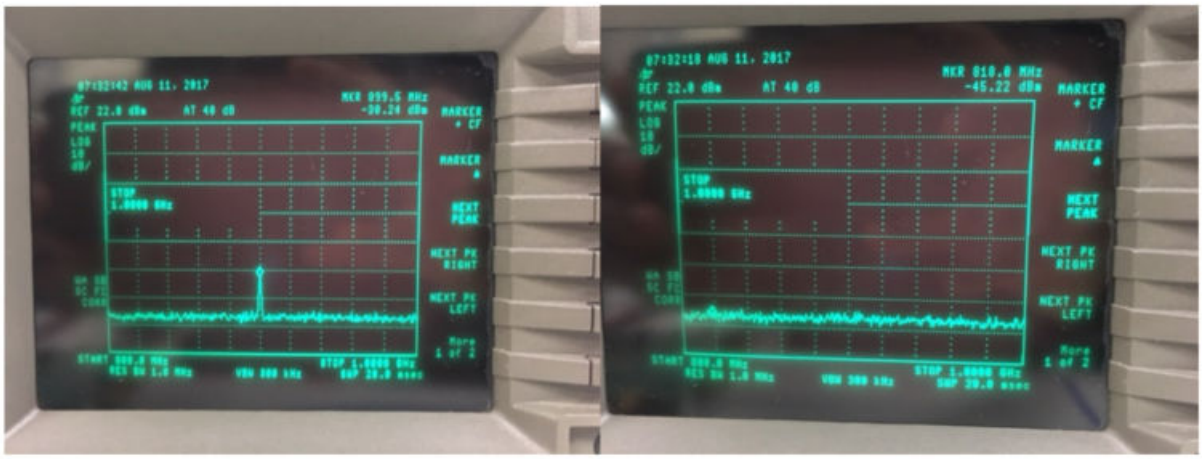


Figure 1.2. RMI Single-ended (SE) Clock vs Differential (Diff) Clock

Figure 1.1 EMI Single-ended (SE) Clock vs Differential (Diff) Clock on page 3 and Figure 1.2 RMI Single-ended (SE) Clock vs Differential (Diff) Clock on page 3 demonstrate an important advantage in using differential clocks, which is that the interference from a differential clock is low even when the signal integrity of the differential clock is good. Thus, a faster rise/fall time does not necessarily mean larger interference as in single-ended clocks.

2. Slew Rate Control for CMOS Clocks

While the previous section demonstrates the power of using differential clocks, using CMOS clocks becomes unavoidable in certain applications, especially in consumer electronic products. The Si5332 provides slew rate control as shown in the figure below (refer to the Si5332 Family Reference Manual for the register field that controls slew rate for CMOS outputs). As seen in the figure, there are four different slew rate settings in Si5332.

Figure 2.1. Slew Rate Control in Si5332

The following table shows the fundamental mode power (EMI) and the power in 800MHz – 1GHz range (RFI) for each slew rate setting.

Slew Rate Setting	EMI (dBm)	RFI (dBm)
Fast	10.75	-25
Slow	10.73	-31.5
Slower	10.5	-36.6
Slowest	10.4	-39

As shown in the table, as the fundamental node power (a place holder for EMI) does not decrease, we can see that the slower slew rates (or larger rise/fall times or poorer signal integrity) helps reduce RFI significantly. Hence, the option of using slower slew rates is especially useful when there is a need to reduce RFI but the poorer signal integrity will often limit the maximum clock frequency that is possible.

3. Spread Spectrum Clocking (for EMI Reduction)

Spread spectrum clocking (SSC) is “frequency modulation” of a clock that is a very powerful tool for reducing EMI. As shown in Fig 4, spread spectrum clocking can significantly reduce EMI.

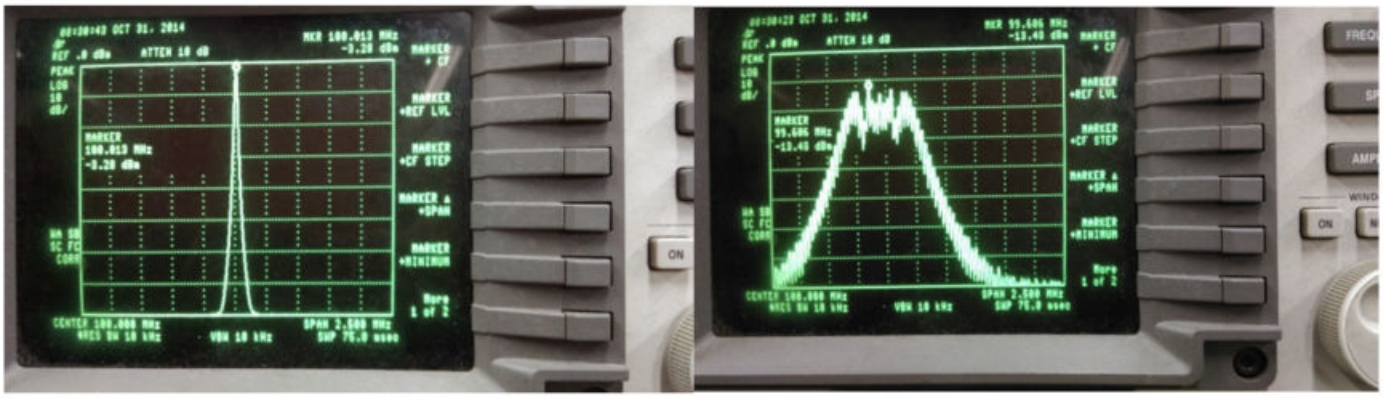


Figure 3.1. EMI Reduction due to -0.5% Down Spread on a 100 MHz Clock Used for PCIE Applications

Spread spectrum clocking is available only on the multisynth divider (id) divider-driven outputs. Each id can implement spread spectrum in either the main divider or the backup divider (the FS option). The user programs both these dividers for both ids and therefore, programs a maximum of four different spread spectrum “profiles” from the same part. The SSC generation equations are shown below. As illustrated in Figure 3.3 Illustration of Center and Down Spread SSC Clocks as Frequency vs Time Plots on page 6, the amplitude of the SSC clock frequency is denoted by ssc% and the modulation rate is denoted by Fmod in the equations below.

$$\text{Amod} = \begin{cases} \{\text{ssc\%} * 2\}/100 & \text{for center spread} \\ \text{ssc\%}/100 & \text{for down spread} \end{cases}$$

$$\text{idxy\_ss\_step\_num} = \frac{\left\{\frac{\text{vcoFreq}}{\text{idxy}}\right\}}{\text{Fmod} * 4}$$

$$\text{idxy\_ss\_step\_res} = \frac{\{\text{Amod} * \text{idxy\_den} * idxy * 128\}}{2 * \text{idxy\_ss\_step\_num}}$$

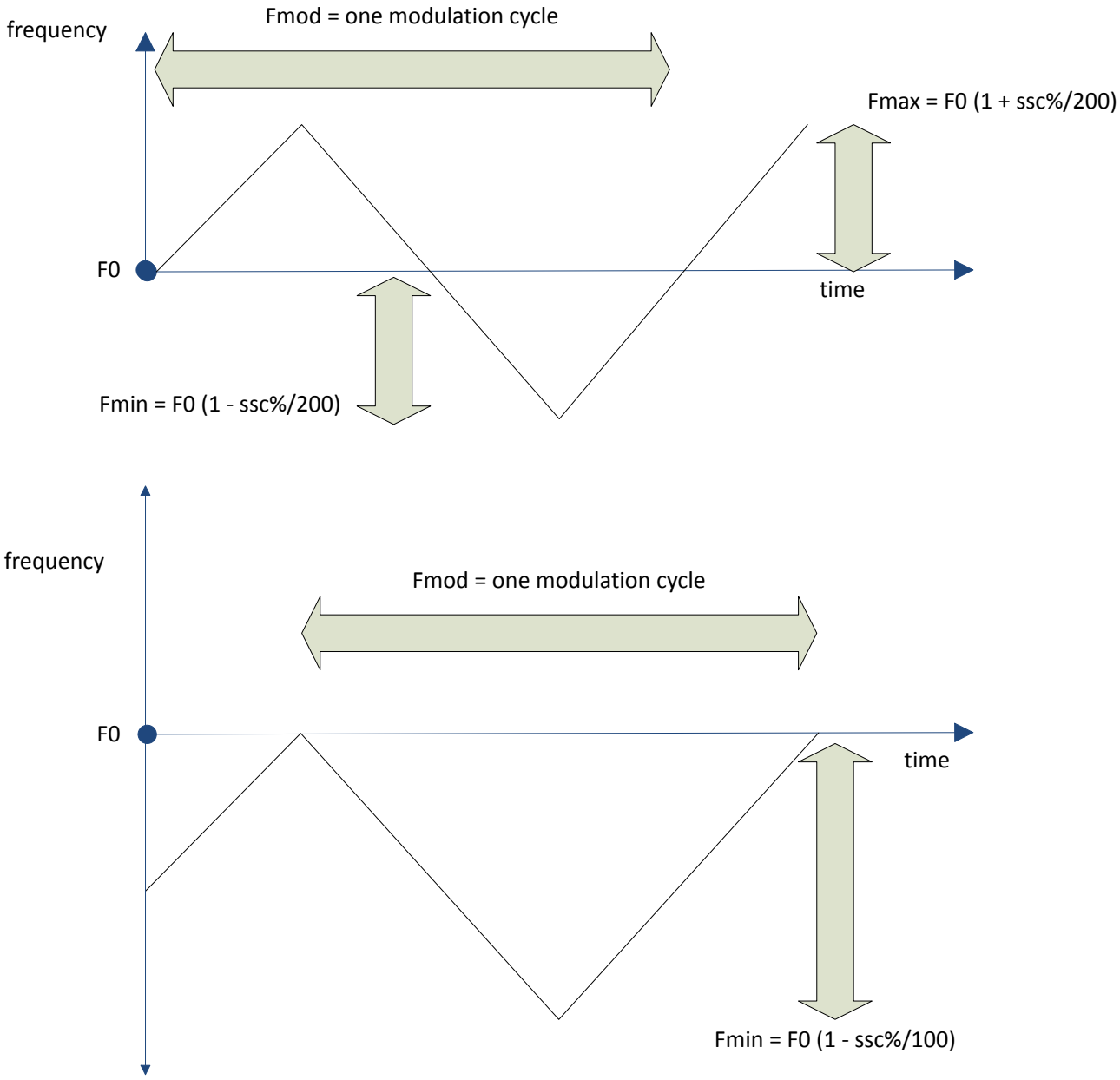


Figure 3.3. Illustration of Center and Down Spread SSC Clocks as Frequency vs Time Plots

The table below describes the physical meanings for the register fields (and terms) idxy_ss_step_num and idxy_ss_step_res. The register field idxy_ss_step_num can also be viewed as the number of frequency steps between the mean and the minimum frequencies in SSC clocking and idxy_ss_step_res as the frequency resolution that is required in each step. The goal should be to maximize the number of steps and minimize the resolution. However, the number of steps is set by the modulation rate (typically 30-33 kHz). The step resolution can be minimized by setting the largest value possible for idxy_den. Idxy_den is the denominator of the id divider and setting it as close as possible to $2^{15} - 1$ is desired.

Table 3.1. SSC Register Fields

Register	Description
idxy_ss_ena	Spread spectrum enable. This is the only bank configuration field which may be changed dynamically while the bank is selected as the active bank. Users may freely enable/disable spread spectrum. 0 = spread spectrum disabled 1 = spread spectrum enabled
idxy_ss_mode	Spread spectrum mode. 0 = disabled 1 = center 2 = invalid 3 = Down
idxy_ss_clk_num	Number of output clocks for each frequency step.
idxy_ss_step_num	Number of frequency steps in one quarter SSC modulation cycle, allows for frequency step in every output clock.
idxy_ss_step_intg	Divide ratio spread step size.
idxy_ss_step_res	Numerator of spread step size error term.
idxy_ss_step_den	Denominator of spread step size error term.

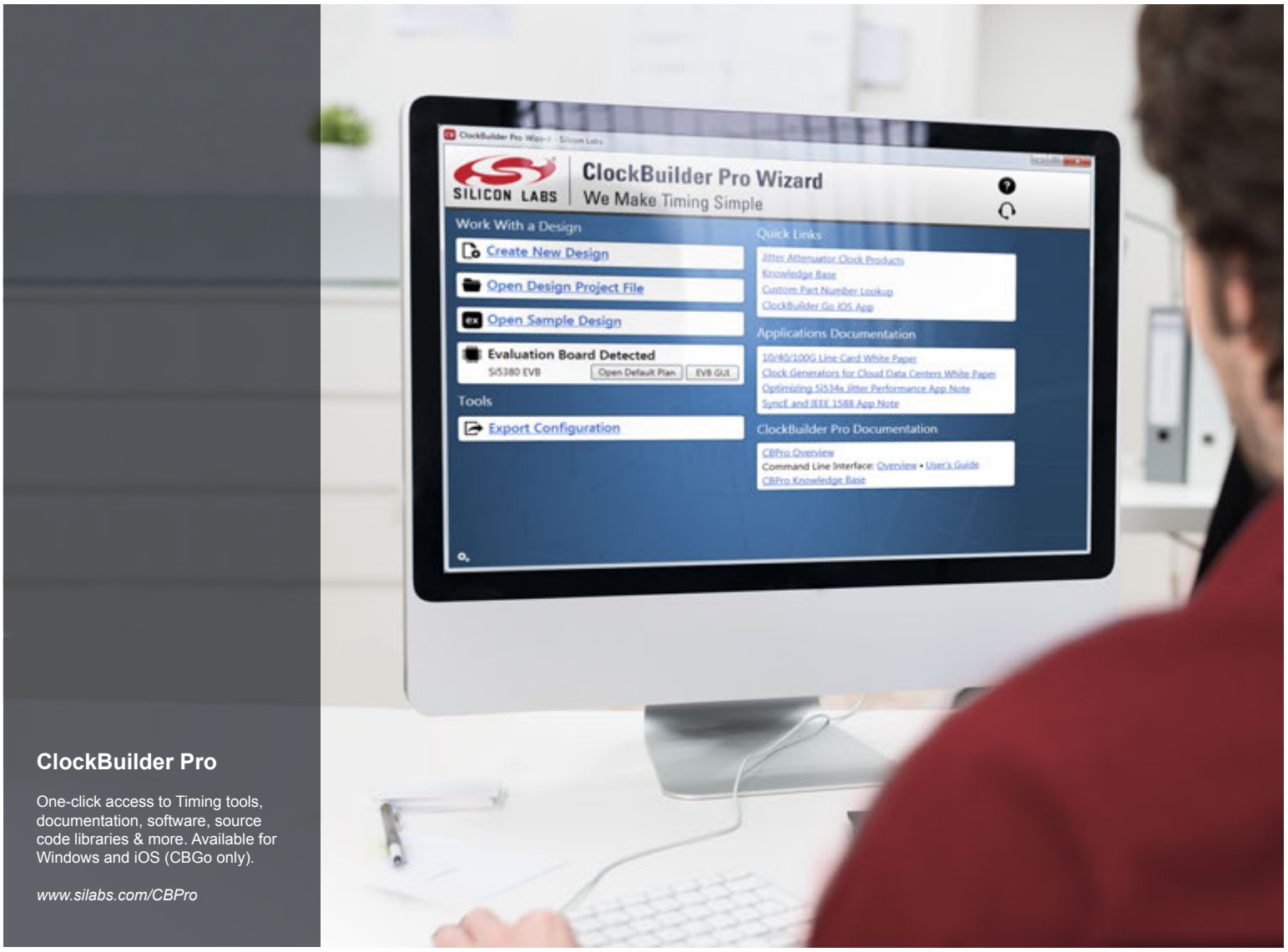
To enable SSC, idxy_ss_ena needs to be set and the right mode selected in idxy_ss_mode. The number of output clocks in each frequency step (idxy_ss_clk_num) needs to be set to 1. The idxy_ss_step_den is the same as idxy_den and idxy_ss_step_intg is always zero.

Details on programming spread spectrum clocking is available in the Si5332 Family Reference Manual. It is highly recommended that the user takes advantage of CBProTM for setting SSC clocks (both for volatile memory programming or for creating custom parts with SSC programming set in NVM).

The Si5332 can support center (up to +/-2.5%) or down (up to -2.5%) spread profiles. However, it is important to note that spread spectrum clocking adds deterministic jitter to the clock and hence, the jitter requirements and tolerance of the system needs to be carefully analyzed before programming/designing spread spectrum clocks.

4. Conclusion

The Si5332 is a versatile clock generator that can support multiple tools to reduce EMI and RFI in electronic systems. In general, using a differential clock is preferred for reducing EMI and RFI. However, when the system can tolerate spread spectrum clocking, using SSC clocks provides a significant EMI reduction advantage. For CMOS clocks, SSC clocking is highly beneficial if the system jitter specifications allow for SSC clocks. Slew rate programming is a useful tool for RFI reduction in CMOS clocks. Using these three tools, any electronic system that uses Si5332 can be designed to provide the best compliance for EMI and RFI requirements.



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