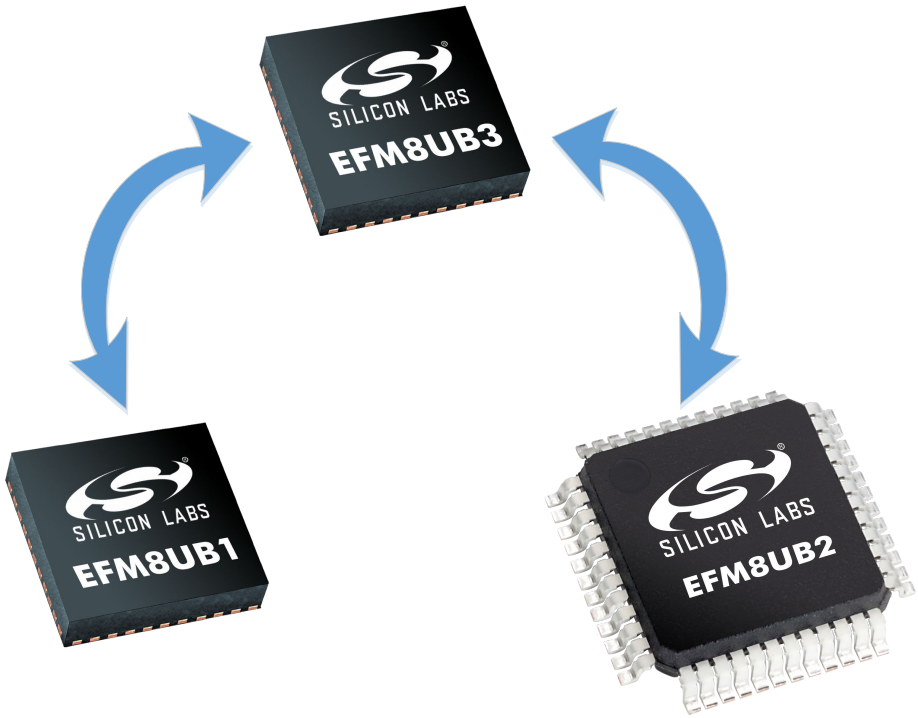
AN1116: EFM8UB1/2 to EFM8UB3 Compatibility and Migration Guide

This porting guide is targeted at migrating an existing design from a EFM8UB1 or EFM8UB2 to a EFM8UB3 microcontroller. Both hardware and software migration needs to be considered.

KEY POINTS

- The EFM8UB3 maintains a high degree of pin and feature compatibility with EFM8UB1.
- Designs will require minimal hardware or software changes when migrating EFM8UB1 to EFM8UB3.
- EFM8UB3 is software compatible with EFM8UB2, only minor changes are required for common peripherals.



1. Introduction

The Universal Bee family of EFM8 microcontrollers is ideal for space constrained USB applications. The family includes devices with a USB 2.0-compliant full speed controller. This application note highlights the differences between EFM8UB1, EFM8UB2, and EFM8UB3 microcontrollers. The EFM8UB3 family is designed to be largely code-compatible and pin-compatible with EFM8UB1 devices, and thus requires only minor changes when porting firmware and hardware between the two families. EFM8UB2 is not pin-compatible with EFM8UB1 and EFM8UB3. This document describes in detail what is required to integrate an EFM8UB3 into a design in place of an existing EFM8UB1 or EFM8UB2 device, respectively.

2. Device Comparison

The table below provides a full feature comparison for EFM8UB1, EFM8UB2, and EFM8UB3. Some peripherals and capabilities are identical between these MCU families, but some are unique to one of the families. When moving a design from one MCU family to another, ensure that the new MCU family includes the necessary features.

Note: The features listed in the table might not be available on every part number of a product family. See the Ordering information section of the applicable data sheet to determine the specific part number that includes features necessary for the design.

Table 2.1. EFM8UB1/2/3 Family Features

Feature	EFM8UB1	EFM8UB2	EFM8UB3
Core & Memory			
Flash	16 or 8 kB	64 or 32 kB	40 kB
XRAM	2304 bytes	4352 or 2304 bytes	3328 bytes
SFR Page	0x00, 0x10, 0x20	0x00, 0x0F	0x00, 0x10, 0x20
Analog			
ADC Resolution & Throughput Rate	200 ksps in 12 Bits 800 ksps in 10 Bits	500 ksps in 10 Bits	200 ksps in 12 Bits 800 ksps in 10 Bits
Voltage Reference	External VREF pin, Internal reference 1.65 V / 2.4 V, Internal 1.8 V LDO, or VDD pin	External VREF pin, Internal reference 1.2 V / 2.4 V, Internal 1.8 V LDO, or VDD pin	External VREF pin, Internal reference 1.65 V / 2.4 V, Internal 1.8 V LDO, or VDD pin
Comparators	2	2	2
Digital			
Port Pins	22/17/13	40/25	17/13
Port Match	✓	—	✓
USB	Low energy USB 2.0 Full/Low speed Controller	USB 2.0 Full/Low speed Controller	Low energy USB 2.0 Full/Low speed Controller
UARTs	UART0, UART1	UART0, UART1	UART1
SPI	1	1	1
SMBus	SMBus0	SMBus0, SMBus1	SMBus0
I2C High-Speed Slave	✓	—	—
Timers	Timer0-4	Timer0-5	Timer0-5
Programmable Counter Array	3-channel	5-channel with watchdog	3-channel
16-bit CRC	✓	—	✓
Configurable Logic Units	—	—	✓
External Memory Interface	—	✓	—
Pinout and Packages			
QFN28	✓	—	—
QSOP24	✓	—	✓
QFN24	—	—	✓
QFN20	✓	—	✓
QFP48/QFP32/QFN32	—	✓	—

3. Device Migration from EFM8UB1 to EFM8UB3

Both Flash and XRAM memory size are increased on EFM8UB3 compared to EFM8UB1. In addition, EFM8UB3 maintains a high degree of pin and feature compatibility with EFM8UB1, requiring only minor changes when porting firmware and hardware between the two device families.

3.1 Pin Compatibility

QSOP24 and QFN20 package options in each product family are pin-compatible, no PCB redesign is necessary when switching between these product families. The table below shows the variants of the EFM8UB1 and EFM8UB3 families.

Table 3.1. Pin-Compatible MCUs

Package	EFM8UB1	EFM8UB3
QFN28	EFM8UB10F16G-QFN28	—
QSOP24	EFM8UB11F16G-QSOP24	EFM8UB31F40G-QSOP24
QFN24	—	EFM8UB31F40G-QFN24
QFN20	EFM8UB10F16G-QFN20 EFM8UB10F8G-QFN20	EFM8UB30F40G-QFN20

3.2 Hardware Incompatibilities

The UART0 and High-Speed I2C Slave peripherals are available in the EFM8UB1 only.

The EFM8UB3 family includes the following new features comparing with EFM8UB1.

- 4 x Configurable Logic Units (CLU0/1/2/3)
- Timer 5
- UART1 RX supports sourcing from CLUx
- SPI SCK, Master MISO, and Slave MOSI supports sourcing from CLUx

3.3 Software Compatibility

The Special Function Registers (SFRs) of the EFM8UB1 and EFM8UB3 are very similar. However, there are a few differences related to functionality or features found on only one of the two device families. The table below shows the combined SFR map of the two device families. The SFRs that differ between the two families are highlighted.

Table 3.2. EFM8UB1 and EFM8UB3 Special Function Register (SFR) Memory Map Comparison

SFR Address									
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	SFR Page
F8	SPI0CN0	—	UART1FCT	P2MAT	P2MASK	P0MAT	P0MASK	—	0x20
	—	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	TMR2CN1	TMR3CN1	TMR4CN1	0x10
	SPI0CN0					P0MAT	P0MASK	VDM0CN	0x00
F0	B	P0MDIN	P1MDIN	P2MDIN	P3MDIN1	I2C0FCT	PRTDRV	SPI0FCT	0x20
		PMR5CN12	IPH	EIP1	EIP2	EIP1H	EIP2H	PCA0PWM	0x10
		P0MDIN	P1MDIN		—	—	PRTDRV		0x00
E8	CLIF0	—	—	—	—	P1MAT	P1MASK	SMB0FCT	0x20
	ADC0CN0	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	—	—	HFOCN	0x10
						P1MAT	P1MASK	RSTSRC	0x00
E0	ACC	XBR0	XBR1	XBR2	—	—	—	EMI0CN	0x20
		—	—	—	PCON1		EIE1		0x10
					1T01TF				
		XBR0	XBR1	XBR2	PCON1				0x00
					1T01TF				
D8	UART1FCN1	CLOUT0	UART1PCF	—	—	CRC0IN	CRC0DAT	SPI0PCF	0x20
	PCA0CN0	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	—	—	ADC0PWR	0x10
						CRC0IN	CRC0DAT		0x00
D0	PSW	—	CRC0ST	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR	0x20
		REF0CN	TMR5RLL	TMR5RLH	TMR5L	TMR5H	HFO1CAL	SFRSTACK	0x10
			CRC0ST	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR	0x00
C8	SCON1	REG0CN	CLU3CF	CLEN0	P2SKIP	CLIE0	CRC0CN0	CRC0FLIP	0x20
	TMR2CN0	—	TMR2RLL	TRM2RLH	TMR2L	TMR2H	EIE2	SFRPGCN	0x10
		REG0CN					CRC0CN0	CRC0FLIP	0x00
C0	SMB0CN0	SMB0CF	SMB0DAT	SMB0FCN0	SMB0FCN1	SMB0RXLN	REG1CN	CLU3FN	0x20
	TMR5CN0	PFE0CN	—	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	HFO0CAL	0x10
	SMB0CN0	SMB0CF	SMB0DAT						0x00
B8	IP	CLU1FN	—	CLU1CF	CLU2FN	CLU2CF	USB0CDCN	USB0CDSTA	0x20
		I2C0STAT	I2C0CN0	I2C0DOUT	I2C0DIN	I2C0SLAD			
		ADC0TK	—	ADC0MX	ADC0CF	ADC0L	ADC0H	CMP1CN0	0x00
									0x10

SFR Address									
B0	P3	CLU0CF	USB0AEC	USB0XCN	—	USB0CF	USB0CDCF	FLKEY	0x20
		LFO0CN	ADC0CN1	ADC0AC		—	—		0x10
						DEVICEID	REVID		0x00
A8	IE	CLKSEL	—	I2C0FCN1	SMB0TC	CLU0FN	USB0ADR	USB0DAT	0x20
						I2C0FCN0			
			CMP1MX	CMP1MD	CMP1CN1	PSTAT0			0x10
					SMB0TC	DERIVID			0x00
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	SFRPAGE	0x20
		—	TMR4RLL	TMR4RLH	TMR4L	TMR4H	CKCON1		0x10
		SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT		0x00
98	SCON1	SBUF1	SPI0FCON0	SPI0FCN1	P3MDOUT	UART1FCN0	UART1LIN	—	0x20
	SCON0	SBUF0							
	TMR4CN0	CMP0CN1	—	CMP0CN0	PCA0CLR	CMP0MD	PCA0CENT	CMP0MX	0x10
	SCON1	SBUF1	PCON1						0x00
	SCON0	SBUF0							
90	P1	CLU2MX	CLU3MX	SMOD1	SBCON1	SBRLL1	SRBLH1	WDTCN	0x20
			SBUF1						
		TMR3CN0	TMR3RLL	TMR3RLH	TMR3L	TMR3H	PCA0POL		0x10
									0x00
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON0	PSCTL	0x20
									0x10
									0x00
80	P0	SP	DPL	DPH	CLU0MX	CLU1MX	CRC0CN1	PCON0	0x20
					—	IT01CF	—		0x10
							CRC0CN1		0x00

Note:

1. **Green** cells denote EFM8UB1 devices only.
2. **Blue** cells denote EFM8UB3 devices only.

4. Device Migration from EFM8UB2 to EFM8UB3

The package options in EFM8UB2 and EFM8UB3 are not completely pin-compatible. Existing EFM8UB2 hardware must be re-designed accordingly when porting.

4.1 Hardware Incompatibilities

The external memory interface (EMIF), UART0 and SMBus1 are available on the EFM8UB2 only.

The I/O Port Match functionality, 16-bit CRC unit and Configurable Logic Units are available on the EFM8UB3 only.

EFM8UB3 includes a number of new features, four priority levels, snooze power mode configuration, flexible wake-up sources selection for suspend or snooze mode.

4.1.1 USB

New features included in the USB0 module on EFM8UB3:

- Low Energy Mode to reduce active supply current based on bus bandwidth
- Charger detection circuitry with automatic detection of SDP, CDP and DCP interfaces.
- D+ and D- can be routed to ADC input to support ACM and proprietary charger architectures.

The figure below shows a typical bus-powered connection diagram for the EFM8UB3. The P3.1/VBUS pin of EFM8UB3 can be used as GPIO or a sense input to the USB module using VBUSEN bit in the USB0CF register. The VBUS pin is not required as a sensing pin for proper operation in Bus-powered mode. It is recommended to use the VBUS pin only as a GPIO by clearing VBUSEN and VBUSIE to 0 in the USB0CF register. To do this using the USB stack, set the device to use bus-powered mode.

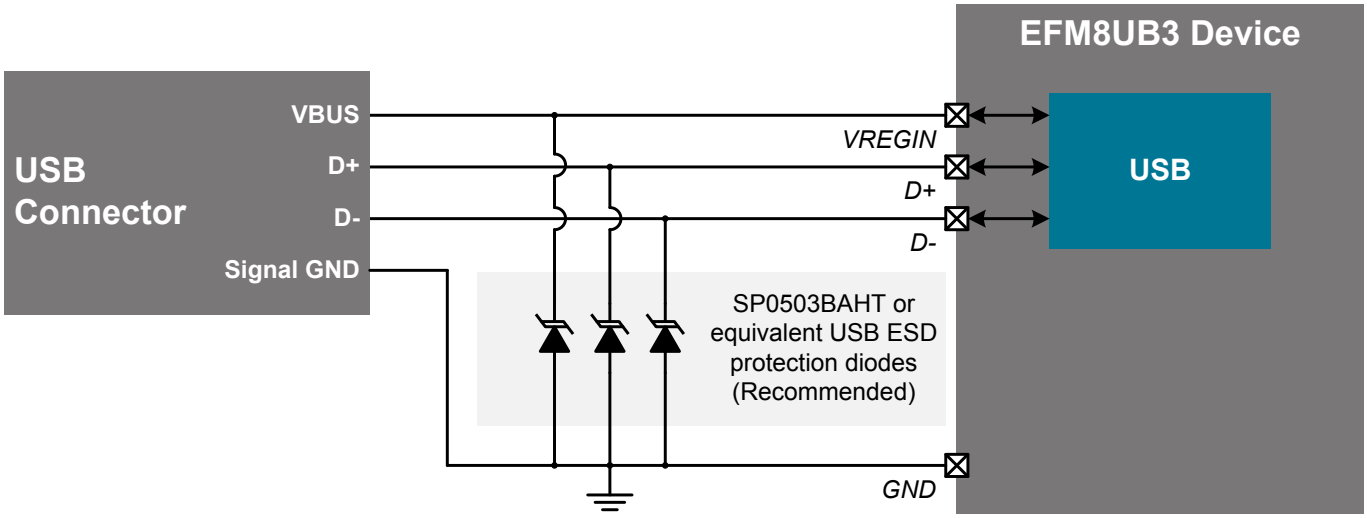


Figure 4.1. Bus-Powered Connection Diagram for USB Pins

The figure below shows a typical self-powered connection diagram for EFM8UB3. As the EFM8UB3 data sheet notes, there are two relevant restrictions on the VBUS pin voltage. The first is the absolute maximum voltage on the VBUS pin, which is defined as VIO + 2.5 V. The second is the input high voltage (VIH) for VBUS to detect when the device is connected to a bus, which is defined as 0.7 x VIO. For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 4.4 V to 5.5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet these specifications and ensure reliable device operation.

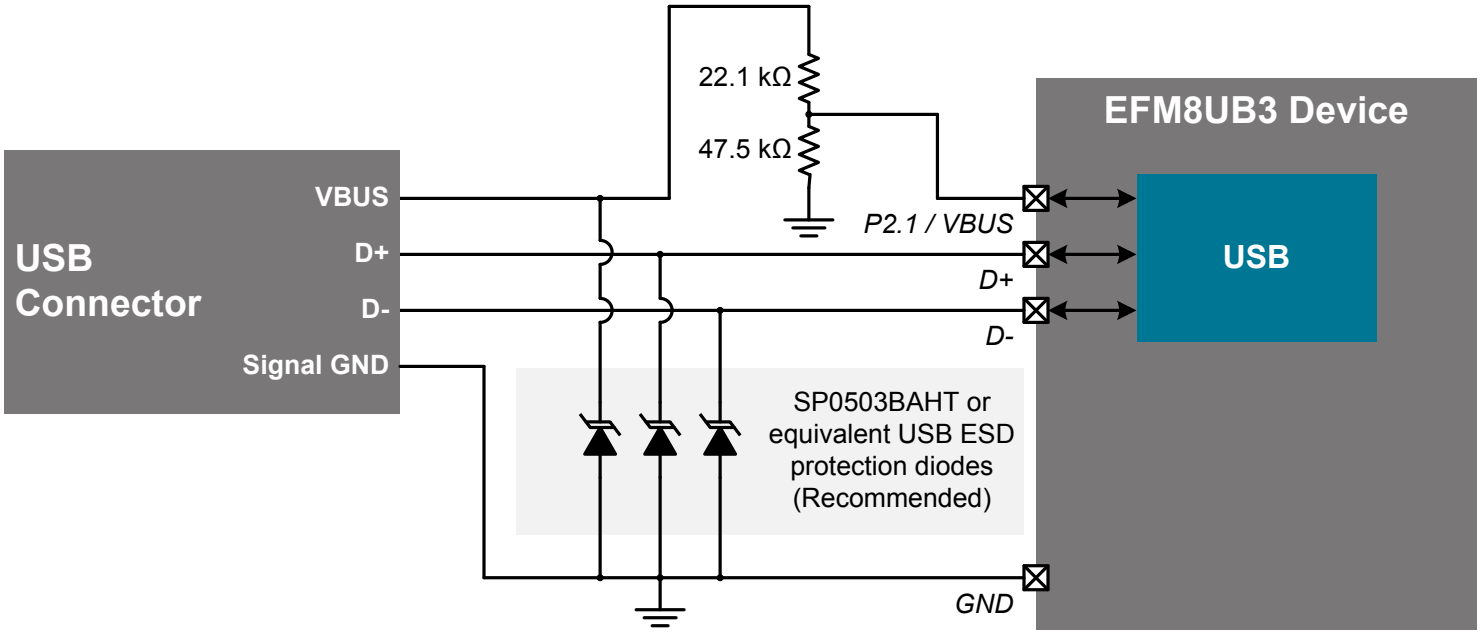


Figure 4.2. Self-Powered Connection Diagram for USB Pins

4.1.2 Power Management

EFM8UB3 supports Snooze mode which is similar to Suspend mode but with regulators in low bias current mode for energy savings.

The EFM8UB2 operating in Suspend mode can only be woken up by USB0 Bus activity. The EFM8UB3 in Suspend or Snooze mode can be woken up by the following events:

- USB0 Bus Activity
- Timer 4 Event
- SPI0 Activity
- Port Match Event
- Comparator 0 Falling Edge
- CLUn Interrupt-Enabled Event

For more information, please see EFM8UB3 Reference Manual on how to use these wake-up sources.

4.1.3 Oscillator and Clocking

EFM8UB2 has two internal oscillators (48 MHz and 80 kHz), while EFM8UB3 has three internal oscillators (48 MHz, 24.5 MHz, and 80 kHz).

The HFOSC0 and HFOSC1 in EFM8UB3 include 1.5x pre-scalers for system clock configuration.

Table 4.1. Oscillators & Clocking Differences

Internal Oscillators	EFM8UB2	EFM8UB3
HFOSC0	48 MHz, ±1.5%	24.5 MHz, ±2%
HFOSC1	—	48 MHz, ±1.5%
LFOSC0	80 kHz	80 kHz
Default System Clock	48 MHz / 4 / 8 = 1.5 MHz	24.5 MHz / 8 = 3.0625 MHz

4.1.4 ADC

The ADC peripheral is different between EFM8UB2 and EFM8UB3 families. The ADC on EFM8UB3 supports a maximum throughput rate of 200 ksps in 12-bit mode or 800 ksps in 10-bit mode while the ADC on EFM8UB2 supports 500 ksps with 10-bit mode.

4.1.5 Voltage Reference

The EFM8UB3 integrates a high-speed internal reference offering two programmable voltage levels, 1.65 V or 2.4 V. It is not routed to an external pin and requires no external decoupling.

The on-chip voltage reference on EFM8UB2 can be configured to output 1.2 V or 2.4 V on the VREF pin.

4.1.6 I/O

The EFM8UB3 supports up to 17 direct-pin interrupt sources with shared Port Match interrupt vector.

The EFM8UB2 has no Port Match functionality.

4.1.7 Programmable Counter Array (PCA0)

The EFM8UB3 family PCA has three independently-configurable channels while the EFM8UB2 family PCA has five independently-configurable channels and integrates watchdog timer.

4.1.8 Watchdog Timer

The EFM8UB3 includes an independent watchdog timer clocked by the low frequency oscillator. The EFM8UB2 watchdog timer is integrated in the PCA0 peripheral.

4.2 Software Compatibility

To support more peripherals, The EFM8UB3 uses three SFR pages (0x00, 0x10 and 0x20) while the EFM8UB2 uses two SFR pages (0x00 and 0xF0). All the common 8051 SFRs are available on all pages. The SFRPAGE register must be set to the appropriate SFR page even for common peripherals between EFM8UB2 and EFM8UB3, such as Timer 4, Timer 5. The table below shows the combined SFR map of the two device families. The SFRs that differ between the two families are highlighted.

Table 4.2. EFM8UB2 and EFM8UB3 Special Function Register (SFR) Memory Map Comparison

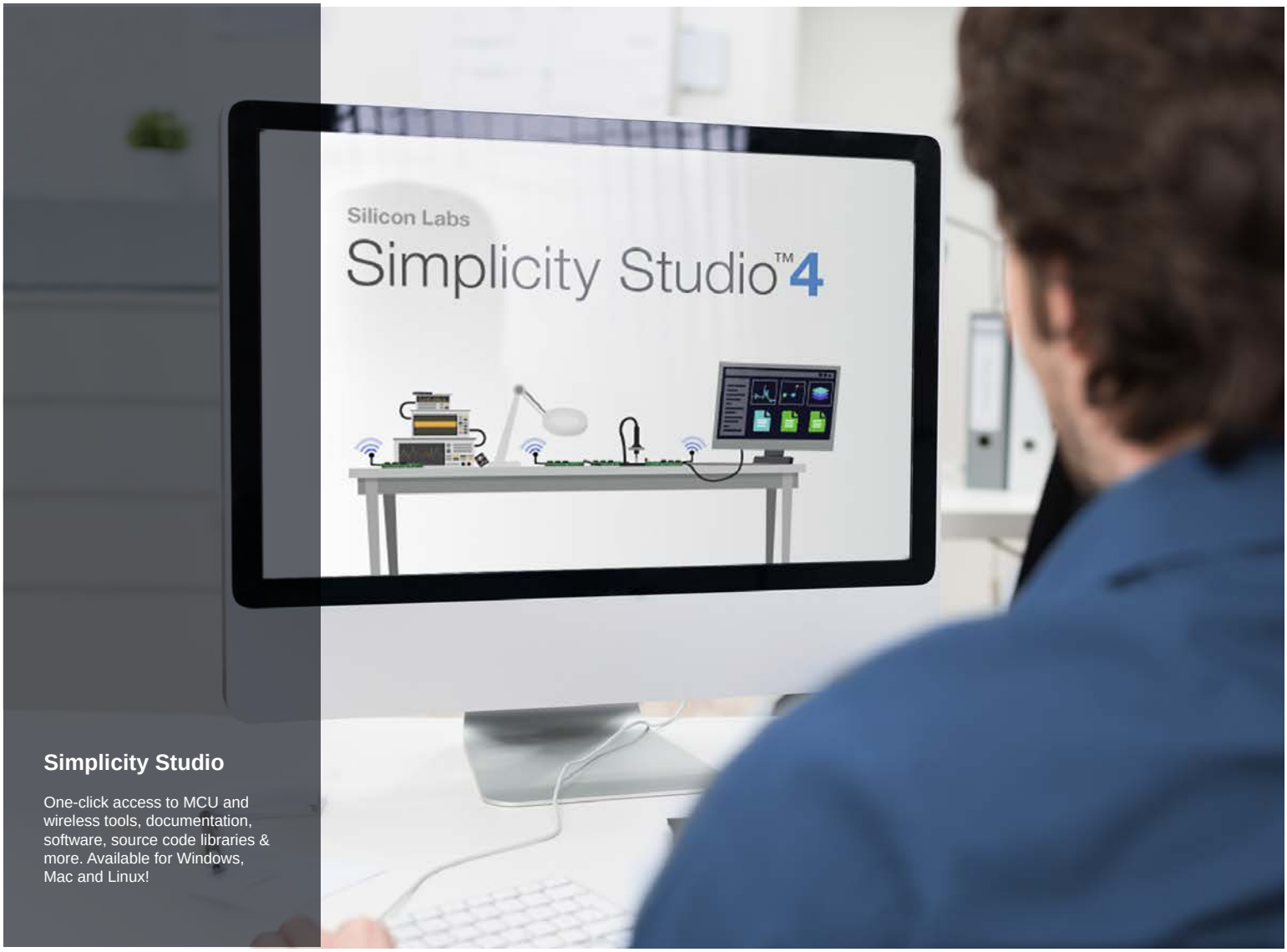
SFR Address									
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	SFR Page
F8	SPI0CN0	—	UART1FCT	P2MAT	P2MASK	P0MAT	P0MASK	—	0x20
	—	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	TMR2CN1	TMR3CN1	TMR4CN1	0x10
	SPI0CN0					P0MAT	P0MASK	VDM0CN	0x00
						PCA0CPL4	PCA0CPH4		0xF0
F0	B	P0MDIN	P1MDIN	P2MDIN	—	—	PRTDRV	SPI0FCT	0x20
		PMR5CN1	IPH	EIP1	EIP2	EIP1H	EIP2H	PCA0PWM	0x10
		P0MDIN	P1MDIN		—	—	PRTDRV		0x00
				P2MDIN	P3MDIN	P4MDIN	EIP1	EIP2	0xF0
E8	CLIF0	—	—	—	—	P1MAT	P1MASK	SMB0FCT	0x20
	ADC0CN0	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	—	—	HFOCN	0x10
						P1MAT	P1MASK	RSTSRC	0x00
						PCA0CPL3	PCA0CPH3		0xF0
E0	ACC	XBR0	XBR1	XBR2	PCON1	—	—	EMI0CN	0x20
		—	—	—			EIE1		0x10
		XBR0	XBR1	XBR2	IT01CF	SMOD1		EIE2	0x00
					CKCON1				0xF0
D8	UART1FCN1	CLOUT0	UART1PCF	—	—	CRC0IN	CRC0DAT	SPI0PCF	0x20
	PCA0CN0	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	—	—	ADC0PWR	0x10
						CRC0IN	CRC0DAT		0x00
						PCA0CPM3	PCA0CPM4	P3SKIP	0xF0
D0	PSW	—	CRC0ST	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR	0x20
		REF0CN	TMR5RLL	TMR5RLH	TMR5L	TMR5H	HFO1CAL	SFRSTACK	0x10
			CRC0ST	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR	0x00
			SCON1	SBUF1			P2SKIP	USB0XCN	0xF0

SFR Address									
C8	—	REG0CN	CLU3CF	CLEN0	—	CLIE0	CRC0CN0	CRC0FLIP	0x20
	TMR2CN0	—	TMR2RLL	TMR2RLH	TMR2L	TMR2H	EIE2	SFRPGCN	0x10
		REG0CN					CRC0CN0	CRC0FLIP	0x00
		REG01CN					SMB0ADM	SMB0ADR	
	TMR5CN0		TMR5RLL	TMR5RLH	TMR5L	TMR5H	SMB1ADM	SMB1ADR	0xF0
C0	SMB0CN0	SMB0CF	SMB0DAT	SMB0FCN0	SMB0FCN1	SMB0RXLN	REG1CN	CLU3FN	0x20
	TMR5CN0	PFE0CN	—	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	HFO0CAL	0x10
	SMB0CN0	SMB0CF	SMB0DAT					P4	0x00
	SMB1CN0	SMB1CF	SMB1DAT						0xF0
B8	IP	CLU1FN	—	CLU1CF	CLU2FN	CLU2CF	USB0CDCN	USB0CDSTA	0x20
		ADC0TK		ADC0MX	ADC0CF	ADC0L	ADC0H	CMP1CN0	0x10
		—	AMX0N	AMX0P				SFRPAGE	0x00
		SMBTC							0xF0
B0	—	CLU0CF	USB0AEC	USB0XCN	—	USB0CF	USB0CDCF	FLKEY	0x20
		LFO0CN	ADC0CN1	ADC0AC		—	—		0x10
						DEVICEID	REVID		0x00
	P3	XOSC0CN	HFO0CN	HFO0CAL	SBRLL1	SBRLH1	FLSCL		0xF0
A8	IE	CLKSEL	—	—	SMB0TC	CLU0FN	USB0ADR	USB0DAT	0x20
			CMP1MX	CMP1MD	CMP1CN1	PSTAT0			0x10
					SMB0TC	DERIVID			0x00
			EMI0CN	—	SBCON1	—	P4MDOUT	PFE0CN	
									0xF0
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	SFRPAGE	0x20
		—	TMR4RLL	TMR4RLH	TMR4L	TMR4H	CKCON1		0x10
		SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT	0x00
									0xF0
98	SCON1	SBUF1	SPI0FCON0	SPI0FCN1	—	UART1FCN0	UART1LIN	—	0x20
	TMR4CN0	CMP0CN1	—	CMP0CN0	PCA0CLR	CMP0MD	PCA0CENT	CMP0MX	0x10
	SCON1	SBUF1							0x00
	SCON0	SBUF0	CMP1CN0		CMP1MD		CMP1MX		
									0xF0

SFR Address									
90	P1	CLU2MX	CLU3MX	SMOD1	SBCON1	SBRLL1	SRBLH1	WDTCN	0x20
		TMR3CN0	TMR3RLL	TMR3RLH	TMR3L	TMR3H	PCA0POL		0x10
							USB0ADR	USB0DAT	0x00
		TMR4CN0	TMR4RLL	TMR4RLH	TMR4L	TMR4H			0xF0
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON0	PSCTL	0x20
									0x10
									0x00
									0xF0
80	P0	SP	DPL	DPH	CLU0MX	CLU1MX	CRC0CN1	PCON0	0x20
					—	IT01CF	—		0x10
							CRC0CN1		0x00
					EMI0TC	EMI0CF	LFO0CN		
									0xF0

Note:

1. **Green** cells denote EFM8UB2 devices only.
2. **Blue** cells denote EFM8UB3 devices only.



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