AN1170: Holdover Using the Si5348 Network Synchronizer Clock

This application note is intended to help users better understand holdover when using the Si5348 Network Synchronizer Clock.

Industry projections show a threefold increase in internet and mobile data traffic over the next several years. This trend continues to drive network operators to transition away from circuit-switch networks to low cost, scalable, high bandwidth, packet-based Ethernet networks to support this growth.

Synchronization is a key element of packet-based Ethernet networks and clock holdover performance plays a critical role in the system. This application note will explore holdover, what it is, how to add it to your application using the Si5348, how to select a proper reference crystal, OCXO or TCXO and the expected holdover performance when using the Si5348.

KEY POINTS

- Network synchronization standards and importance of holdover
- Dual reference Si5348 overview
- How to select a proper crystal, OCXO or TCXO
- Holdover in the Si5348 and how to implement it
- Expected holdover performance and benefits when using Si5348
- Si5348 has superior low jitter and wander performance with excellent holdover characteristics
- Si5348 is G.8262 and G.8262.1 standards compliant
1. Synchronization Standards

There are three main methods for delivering synchronization over packet networks. The first is Synchronous Ethernet (SyncE) which is defined by the Internet Telecommunication Union Telecommunication Standards Sector (ITU-T) G.8262 and G.8262.1. SyncE provides frequency synchronization using physical-layer-based timing. The second approach is to use packet-based timing using Precision Time Protocol, PTP, (IEEE 1588-2008), provides time synchronization as defined by ITU-T G.826x (frequency synchronization), and by ITU-T G.827x (phase synchronization). IEEE 1588 exchanges time stamps between network nodes used to synchronize the local system to an accurate master clock. Lastly, Global Navigation Satellite System, or GNSS, (eg. BeiDou, Galileo, GLONASS, IRNSS/NavIC, QZSS and GPS) can be used to provide both frequency and phase synchronization. This requires an antenna and line of sight visibility to the sky, which can be impractical and less cost effective.

Synchronization standards have defined the term “holdover” so that the network continues to function reliably in the event the synchronization input to a reference clock source is disrupted or temporarily unavailable. These requirements specify the maximum allowed excursions of an output clock in the event an input is disrupted.
2. Holdover and its Importance in Network Synchronization

The distribution clock is responsible for attenuating jitter, wander, and provide synchronous clocks to downstream networks. Within a network, the distribution clock selects the active reference to lock to from the external synchronization links.

Holdover is defined as an operating condition of a clock which has lost its controlling input and is using stored data, in conjunction with a TCXO or OCXO reference, to control its output. The stored data was acquired previously while in locked operation. Holdover ends when the reference clock controlling input returns and the device transitions back to the locked mode.

System requirements for holdover can range from minutes to days and is dependent on the quality of the TCXO or OCXO reference that the PLL is tracking. An example of the importance of synchronization is in a wireless phone application. Adjacent cell towers must maintain frequency synchronization of +/-50ppb, even when in holdover. Exceeding +/-50ppb will affect call hand-offs between the towers and possibly cause a call to drop.

Holdover is a critical element of network synchronization to ensure network continuity during a clock input disruption.
3. Silicon Labs Solution: Dual Reference Architecture

The Si5348 has a “dual reference” frequency stabilized DCO architecture. It requires both a crystal and a TCXO/OCXO reference. Unlike “single reference” PLL clock architectures the Si5348 design does not trade off holdover stability (low frequency) for jitter performance (high frequency). The frequency stability of the Si5348 design combines a crystal reference for superior low jitter and a stable frequency source such as an OCXO or TCXO for superior wander/holdover performance.

Below is a simplified diagram of the dual reference architecture of the frequency stabilized Si5348.

![Figure 3.1. Frequency-Stabilized DCO in the Si5348 Using Two References](image)

Silicon Labs dual-reference Si5348 meets industry and standards performance requirements and has the additional advantage of maintaining low jitter performance in the 12 kHz to 20 MHz integration band.
4. How to Select a Crystal, OCXO and TCXO

It is important to pick a high-quality crystal and reference OCXO or TCXO. The crystal will determine the output jitter performance so selecting one with correct specification is critical. The second reference, an OCXO or TCXO will determine the output frequency accuracy and overall stability.

An OCXO provides better frequency stability given time and temperature variations and are usually Stratum 3E / G.812 Type III or better performance characteristics. These OCXOs have an accuracy of ±4.6 x 10⁻⁶. A typical short-term drift, with no input reference, of less than ±1.2 x 10⁻⁸ in 24 hours.

TCXOs are typically Stratum 3 / G.812 Type IV level performance and provide lower-cost, reduced power, and a smaller size option in systems allowing the relaxed stability requirements. These TCXOs also have an accuracy of ± 4.6 x 10⁻⁶. The short-term drift, with no input reference, is less than 3.7 x 10⁻⁷ in 24 hours.

A TCXO is less expensive than an OCXO and will meet the standards holdover performance requirements for wander generation. An OCXO is more expensive but has the better wander generation holdover performance.

For most SyncE applications an appropriately specified TCXO will meet compliance requirements for holdover period of ≤ 24 hours. For applications where the holdover period requirement is >24 hours, an OCXO is a better choice.

For PTP/1588 applications, such as wireless communications applications, an OCXO provides improved time error performance to meet the tighter frequency and phase requirements.

For assistance to select an appropriate crystal, OCXO or TCXO, and a recommended list of parts for your application, see the reference guide, Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators for more details.
5. Overview of Holdover in the Si5348

The Si5348 is a Network Synchronizer clock with three independently configurable DSPLLs. Any of the 3 DSPLLs (A, C or D) will automatically enter holdover when the selected input clock becomes invalid (i.e., when either out-of-frequency, OOF, or loss-of-signal, LOS, fault monitoring indicators are asserted) and no other valid input clocks are available for selection. Each DSPLL calculates a historical average of the input frequency while in locked mode to minimize the initial frequency offset when entering the holdover mode. The averaging circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window with the stored historical frequency data. Both the window size and the delay are programmable. The window size determines the amount of holdover frequency averaging. The delay value is used to ignore frequency data that may be corrupt just before the input clock failure. Each of the three Si5348 DSPLLs computes its own holdover frequency average to maintain complete holdover independence between the DSPLLs.

When entering holdover, a DSPLL will pull its output clock frequency to the calculated average holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF / REFb pins. If a clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves adjusting the output clock to achieve frequency and phase lock with the new input clock.

The recommended mode of exit from holdover is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is possible that the new output clock frequency will not be the same as the holdover output frequency because the new input clock frequency might have changed. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of ~40 values that are in between. The loop bandwidth, BW, values do not limit or affect the ramp rate selections (and vice versa).

Each of the three DSPLLs target ramp rate on holdover exit, as well as the holdover window, can be programmed independently in CBPro, see Figure 5.2 on page 7.

CBPro’s default Target Ramp Rate on Holdover Exit is 50ppm/sec. For most applications this value is acceptable, but for ultra-stable systems it can be programmed to a different value that best suits the application.

The default CBPro value for the length of data history used in computing the holdover average frequency is 9 seconds (holdover history window). This value provides sufficient holdover history to meet SyncE and IEEE1588 holdover stability requirements, in conjunction with an appropriate reference, when entering holdover. The value can be increased to provide better averaging accuracy, but keep in mind that the system needs to operate with a stable reference for the window size, plus the delay (length of data ignored), before there is sufficient valid holdover history available to enter holdover. If the device goes into holdover before there is valid holdover history the output will freeze at the last valid input frequency which may not be desirable.
CBPro has a holdover history delay default of 2 seconds. For most applications 2 seconds is sufficient to remove potentially bad data from the frequency history averaging which helps to prevent a frequency jump when the part enters holdover. This value is programmable so can be changed to meet the needs of the application.

![Figure 5.2. DSPLL A Configure](image)

6. How to Implement Holdover in the Si5348

Implementing Holdover in Si5348 can be easily done using the ClockBuilder Pro (CBPro) Wizard to configure the device. The first step is to download or update to the latest version of CBPro at: https://www.silabs.com/products/development-tools/software/clockbuilder-pro-software.

Begin by opening CBPro and select “Create New Project” for the Si5348, or open an existing project file.

As you begin going through the 15 Wizard steps keep in mind that the Si5348 has three independently configurable DSPLLs. Any of the 3 DSPLLs (A, C or D) will automatically enter holdover when the selected input clock becomes invalid (i.e., when either out-of-frequen-cy, OOF, or loss-of-signal, LOS, fault monitoring indicators are asserted) and no other valid input clocks are available for selection.

Key CBPro steps to properly configure Holdover

• Steps 6 and 7 of 15 – Use CBPro wizard to setup input clocks and assign them to each DSPLL
• Step 10 of 15 – Hitless Input Switching Assistant (HSW). See Figure 6.1 on page 8 below.
  1. By selecting the HSW for PLLs A, C, D it will determine the optimal settings based on the communication standard selected. The user can enter a custom range if desired.
  2. Select “Yes” if any of the device input clock is generated from an external switch or multiplexer. This option should be check for each PLL using an externally switched clock input.
  3. Select the appropriate Communication Standard that applies. A custom range can also be entered.

Figure 6.1. CBPro Step 10 – Hitless Input Switching

• Step 11A of 15 – DSPLL A Configure
  • If HSW was selected in Step 10 above, Fast Lock and portions of Input Switching & Holdover are greyed out and cannot be changed.
  • Set the desired loop bandwidth for DSPLL B.
  • Reference Figure 5.2 on page 7 - Select the desired ramp rate for holdover exit and desired holdover window size and delay.
• Step 11B of 15 – DSPLL B Configure
  • Keep in mind that DSPLL B is the source generating the ~14 GHz clock source for DSPLLs A, C and D. DSPLL B’s only input clock is the REF input, which is connected to the high stability OCXO or TCXO. The OCXO/TCXO provides the high accuracy and stability, while the DSPLL B’s closed loop and crystal ensure that the ~14 GHz clock source is low jitter.
  • Follow the step to set the target Loop Bandwidth as well as Fastlock Enable and target Fastlock Loop Bandwidth.
• Step 11C and 11D of 15 – DSPLL C/D Configure
  • Repeat step 11A to configure DSPLL C and DSPLL D as desired.
  • Follow remaining Steps 12-15 to complete the configuration.
  • Remember to check and address any Notes, Warnings, or Errors the Wizard identifies before completing the configuration.
• If you need help, go to the Design Dashboard (opening page) and click on “Ask For Help” in the lower right. It will open a window to the Silicon Labs Web page where you can log in to get further assistance.
7. Expected Performance Using Si5348

Customers demand timing products that are both high performance and field proven to reduce risk and shorten design cycle times. In addition, these products must meet the minimum performance requirements of the applicable standards. Si5348 meets the requirements of ITU-T G.8262 and G.8262.1.

ITU’s standard ITU-T G.8262 [Timing characteristics of a synchronous Ethernet equipment slave clock] defines the performance of PLLs to be used in two different types of Ethernet Equipment Clocks (EECs): EEC Option 1, which is based on a 2048 kbps rate and is used in Europe and Asia, and EEC Option 2, which is based on a 1544 kbps and is used in North America.

The OCXO or TCXO reference has a large impact on the compliance test results. Consult the the reference guide prior to selecting an OCXO or TCXO: Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators.

ECC Option 1 Compliance Test Results - Si5348 Meets All Requirements

![Figure 7.1. EEC Option 1 Holdover Test Result](image-url)
ECC Option 2 Compliance Test Results - Si5348 Meets All Requirements

The G.8262 EEC Option 1 and Option 2 Holdover test results, as well as the other measurements in full report, show the Si5348 Rev E is fully compliant with the SyncE timing characteristics defined by the standard.

8. Conclusion

Network providers are implementing Ethernet based networks to meet the 3x increase in internet and mobile data traffic expected over the next several years. These networks are becoming less dependent on GNSS synchronization and the trend is moving towards using SyncE and IEEE1588.

To maintain network reliability these standards have defined holdover performance requirements for the reference clock in the event the synchronization input is disrupted or becomes temporarily unavailable. These requirements make the reference clock a critical element of the overall network.

Si5348 network synchronizer is a multi-DSPLL clock which has a dual-reference architecture that combines a crystal reference for superior low jitter and a stable frequency source such as an OCXO or TCXO for excellent wander and holdover performance.

The ClockBuilder Pro Software Wizard makes implementing holdover and configuring Si5348 easy. A properly specified crystal, OCXO or TCXO used as the references to the Si5348, makes it fully compliant to the ITU and IEEE standards holdover requirements.
9. Related Documents

- AN1077: Selecting the Right Clocks for Timing Synchronization Applications
- AN905: External References: Optimizing Performance
- Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual
- Si5348 Rev E G.8262 Compliance Report
ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

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