AN1223: LGA Manufacturing Guidance

This Application Note presents information regarding Land Grid Array (LGA) based Silicon Labs Modules classified as System in Package (SiP) modules and provides guidance regarding their usage with regards to manufacturing considerations.

SiP modules require special guidance and considerations as part of a customer board manufacturing process. Specifically, SiP modules should not be handled in the same way as standard QFN devices because they are constructed very differently. Proper care needs to be taken with handling, temperature profile and unit profiling, and general set-up to ensure success with the customer board manufacturing.

This document acts as a formal guide to provide overall general awareness and specific guidance for module products.

KEY POINTS

- SiP Module Overview
- Handling considerations
- JEDEC temperature profile and unit profiling
- General manufacturing set-up considerations
- Troubleshooting guidance

Disclaimer

The information presented in this document uses various standards as references and is based on Silicon Labs experience successfully assembling production PCBs using the module products. The user is highly encouraged to use this document as a guide which highlights the recommendations for the assembly process. It is expected that initial results of the SMT process will be evaluated with the understanding that further optimizations may be required for the specific SMT process in place at the assembly location. Optimization decisions should use engineering judgment to adjust and modify the stencil or tool settings in order to achieve the best performance for production line equipment in order to be JEDEC compliant. Silicon Labs confirms unit solderability and qualifies the SMT readiness for all LGA and PCB module based product designs. As Silicon Labs does not have any control over the custom process, tools, equipment used for the custom assembly, It is always recommended to the user to refer relevant IPC/JEDEC standard for detailed information. ALL INFORMATION PROVIDED IN THIS DOCUMENT IS FURNISHED AS IS, WHERE IS, WITH ALL FAULTS AND WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE, AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR PERFORMANCE OR USAGE OF TRADE.

1. SiP Modules

Silicon Labs IoT SiP modules contain system-level components on a substrate inside a package. Because these modules are not constructed the same as a standard QFN component, they need to be handled differently in several aspects of the manufacturing flow and handling.

1.1 Silicon Labs SiP Module Construction

The SiP modules are manufactured with substrate-based Land Grid Array (LGA) package platform technology which has design rules similar to that of BGA package technology. LGA package technology is laminate-based, not leadframe-based. LGA technology is often used in the designs that require routing that cannot accommodate direct wire-bonding from internal device pads to the external package pins. In this way, LGA package technology addresses designs that require internal component attach and multi-die configurations that often result in final SiP designs, such as Silicon Labs SiP modules.

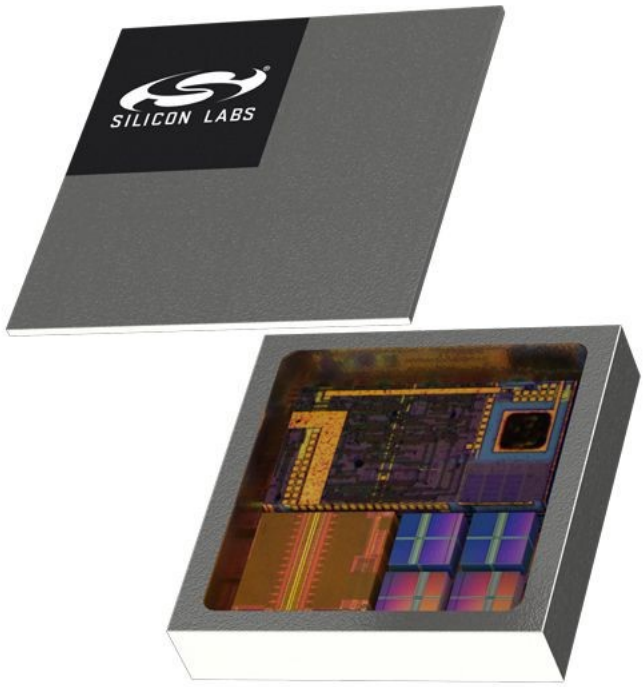


Figure 1.1. Silicon Labs SiP Module Representation

1.2 Difference between QFN and LGA Packages

Despite Silicon Labs SiP module's close appearance to QFN packages, the LGA laminate-based package is quite different in reflow and surface mounting behavior. For high level comparison, QFN package has a standard footprint with predefined pin pad structure and size. On the other hand, the LGA package provides flexibility to have custom footprint which can have irregular pin pad pattern. The LGA's exposed pins for board attach consists of a recessed offset that is defined by the external solder resist material which covers the package surface.

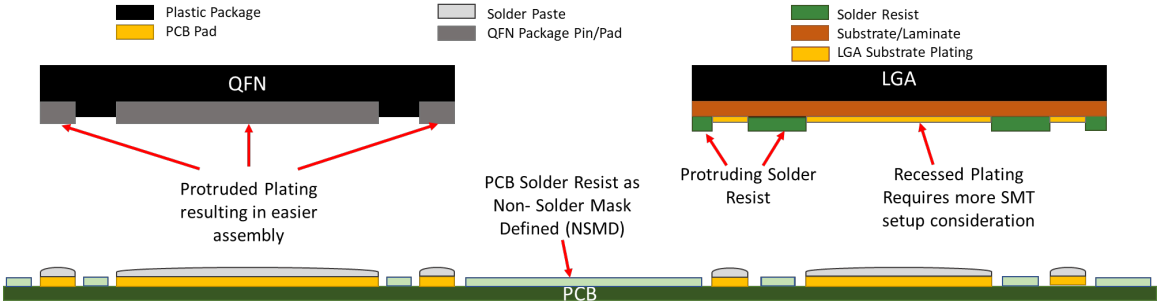


Figure 1.2. Construction Cross-Section Difference between QFN and LGA

In Figure 2.2, the LGA package has recessed pins which are more challenging to reflow, whereas a QFN component's pins protrude slightly aiding in solderability. For this reason, SiP Modules will not always reflow in the same setup or direct manner as a QFN lead-frame-based package. Thus, the Assembly Process Engineer must acknowledge and make adjustments to their board mounting process. During the manufacturing process of a board with a SiP module, consult with the engineers responsible for assembly to make adjustments to assembly process such as solder temperature reflow profile, stencil thickness, aperture opening, etc., based on the specific board design. In some rare instances, the Contract Manufacturer (CM) may suggest changes to the board's PCB layout (such as pad sizes and placement, via and trace positioning, solder mask openings, etc.).

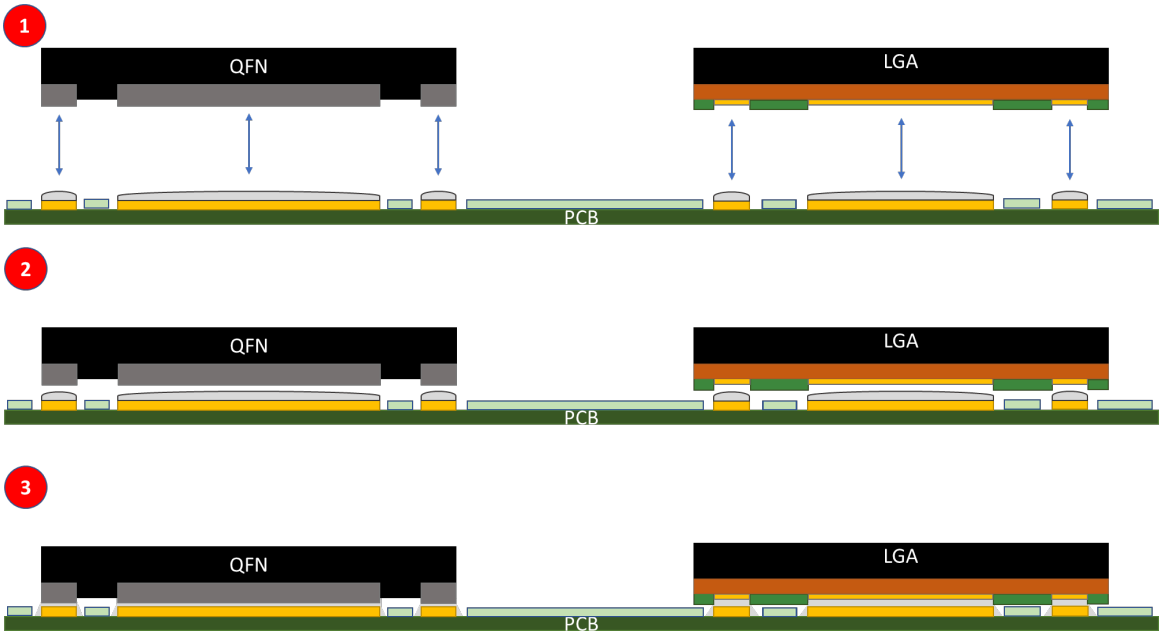


Figure 1.3. Flow for Mounting QFN and LGA Packages on PCB

Figure 2.3 shows the difference between QFN- and LGA-based packages when mounted on PCB. It can be clearly seen that when QFN is mounted on the PCB, the package pins adhere on the PCB pad via the solder joint formed by the melting of the solder paste. This elevates the QFN package from the PCB level. When the LGA is mounted on the PCB, the package pads adhere on the PCB pad via the solder joint formed by the melting of the solder paste, but it should be noted that unlike QFN, the package pads are not visible and are not exposed out to the user.

1.3 Handling

Silicon Labs SiP and PCB Modules have an MSL3 rating (refer to product packaging for MSL label), which requires them to be handled much differently than the standard QFN devices that usually have MSL2 or higher rating. MSL3 rating requires baking to remove moisture if the devices have been cumulatively exposed to humidity beyond **7 days or 168 hours**. Because of this, the assembly process operators need to verify the state of the humidity indicator (HID) card and track closely the cumulative time when the module containers are unsealed, exposing the modules to humidity until reflowed or baked. This cumulative tracking includes instances where the containers were unsealed and resealed. The HID card must be inspected immediately upon opening the module containers to determine if the modules were exposed to excessive humidity. Whenever in doubt, bake the modules as per IPC/JEDEC J-STD-033D standard's guidance to avoid permanent damage to the modules during the assembly reflow.

Figure 1.4. A Pack of Desiccant (left); HID Card Indicating Baking is not Required (right)

As per IPC/JEDEC J-STD-033D, Table 4-1, Note 5 "*The bake times specified are conservative for packages without blocking planes or stacked die. For a stacked die or BGA package with internal planes that impede moisture diffusion the actual bake time may be longer than that required*". As Silicon Labs SiP modules consist of a multi-layer substrate, it is recommended to **bake for 24 hours at 125 °C**.

1.4 JEDEC Temperature Profile

The JEDEC reflow profile is an industry standard that focuses on the different stages of SMT heating that are addressed during component board assembly. Each stage has a range of minimum and maximum temperature and time values that are used as guidelines for optimizing the temperature profile associated with the specific Printed Circuit Assembly (PCA). It should be noted that each PCA is custom and thus requires a unique reflow profile to achieve nominal results over the entire board for a specific assembly process.

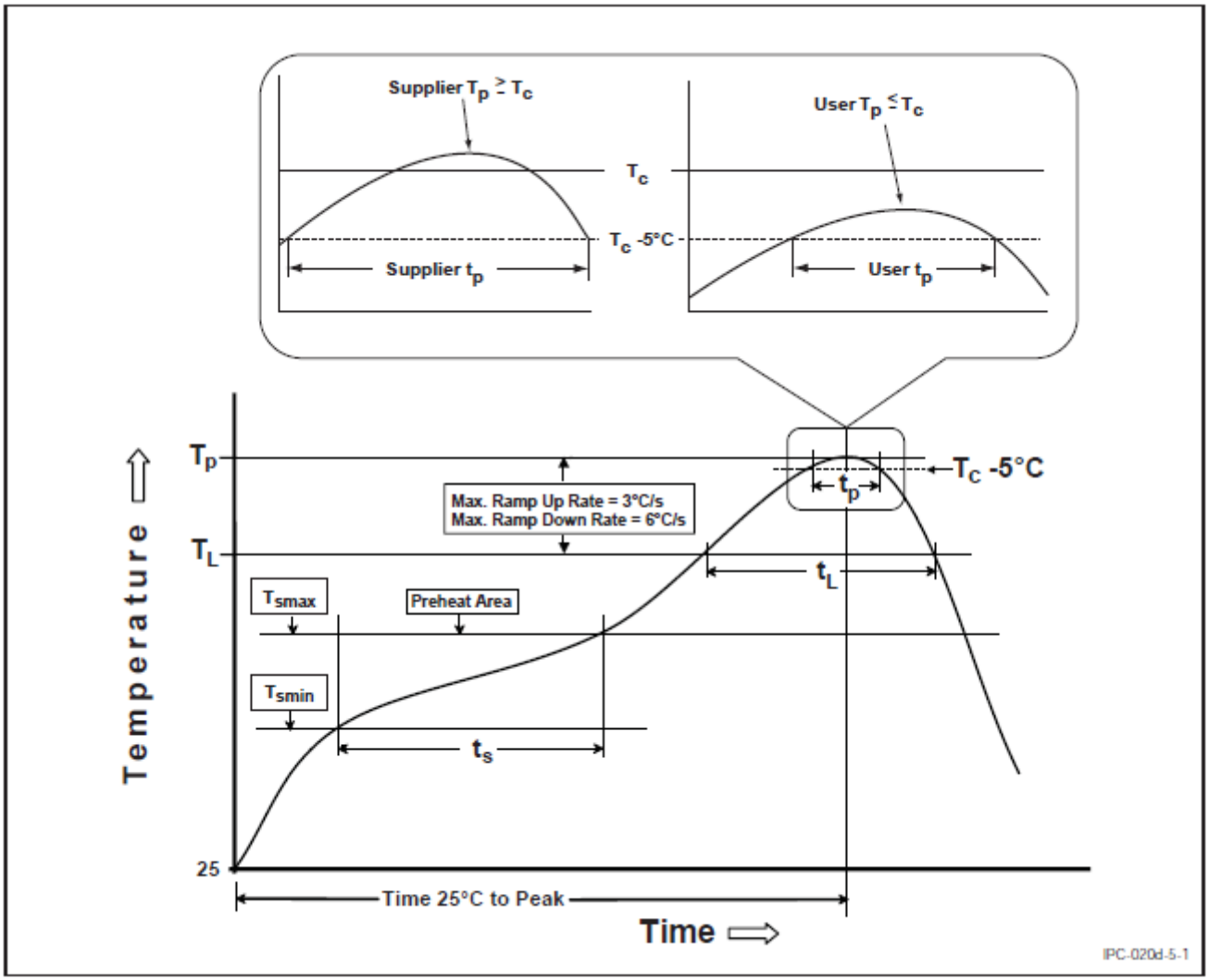


Figure 1.5. Classification Temperature Profile (per Figure 5-1, JEDEC J-STD-020D.1)

The objective of the reflow profile is to allow the solder joints across the board to reach the liquidus temperature of 218 °C and remain above this temperature until all joints have undergone the inter-metallic chemical reflow reaction between the solder and metalized landing pads being joined.

Although Silicon Labs modules are rated to withstand peak temperature of 260 °C, this parameter is not intended to be used as the recommended peak reflow temperature. Instead, for the best yield results, Silicon Labs recommends peak reflow temperature to be limited between 240 °C to 250 °C. In practice, process and board variations will cause the temperature to slightly vary from the set-points, increasing the chances of the modules getting damaged due to over temperature. Thus, 260 °C is not required and should never be targeted during the reflow.

PCAs are designed in various sizes and panels. Large PCAs result in temperature differences at different locations on the PCA. Also, the peak temperature will not be reached at the same time at all locations. Therefore, the time and temperature ranges of the IPC/JEDEC J-STD-020D based profile should be adjusted for the specific PCA being reflowed. Figure 2.6 shows a general reflow profile recommendation from IPC/JEDEC J-STD-020D standard.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p **shall** be within ± 2 °C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Figure 1.6. Classification Reflow Profile (per Table 5-2, JEDEC J-STD-020D.1)

1.5 Unit Profiling

When a new product has to be mounted on the assembly line, the assembly line engineer will start determining the correct oven profile typically tailored for the new product based on their skills, judgment, and experience that fits best with their assembly process. The baseline profile program is generally stored in the assembly line system, which only requires additional tweaks based on multiple factors. It is very important that the oven profile used for this new product is compliant with the JEDEC standard.

A simplified no-clean board assembly line may consist of a solder screen printing tool, component placement tool, SMT reflow oven, and visual inspection equipment. The SMT reflow oven may consist of anywhere from 7-10 heating zones. Thus, every unique assembly line demands a unique unit profile. The unit profile also has to be adjusted based on the type, size, and material of the PCA. Therefore, the assembly line engineer not only has to consider the assembly line variations, but also has to account for unit locations, adjacent components, and PCB metal density to achieve an acceptable JEDEC profile curve.

Parts based on LGA package require special care and should be assembled under a controlled environment. If manufacturing a single board, a single thermocouple on the SiP component is recommended providing accurate profile measurement across the SiP. If manufacturing a panel with several instances of the board, thermocouples should be strategically placed at the main component locations across several areas of the entire board, including the edge locations where the temperature of the critical component such as SiP is continuously tracked and monitored. Figure 2.7 shows an example for the placement of thermocouples when manufacturing a sample panel array of 5x5 radio board instances. The small black squares in the image represent the SiP placed on each radio board and the red numbered circles represent the thermocouples.

If a proper unit profile is not determined, then it is possible that certain locations along the board will differ by as much as 5-7 °C or even more. This may result in certain components staying above liquidus state too long and over-stressing the units. This will not only create poor solder joints but cause internal damage to the part and other critical components.

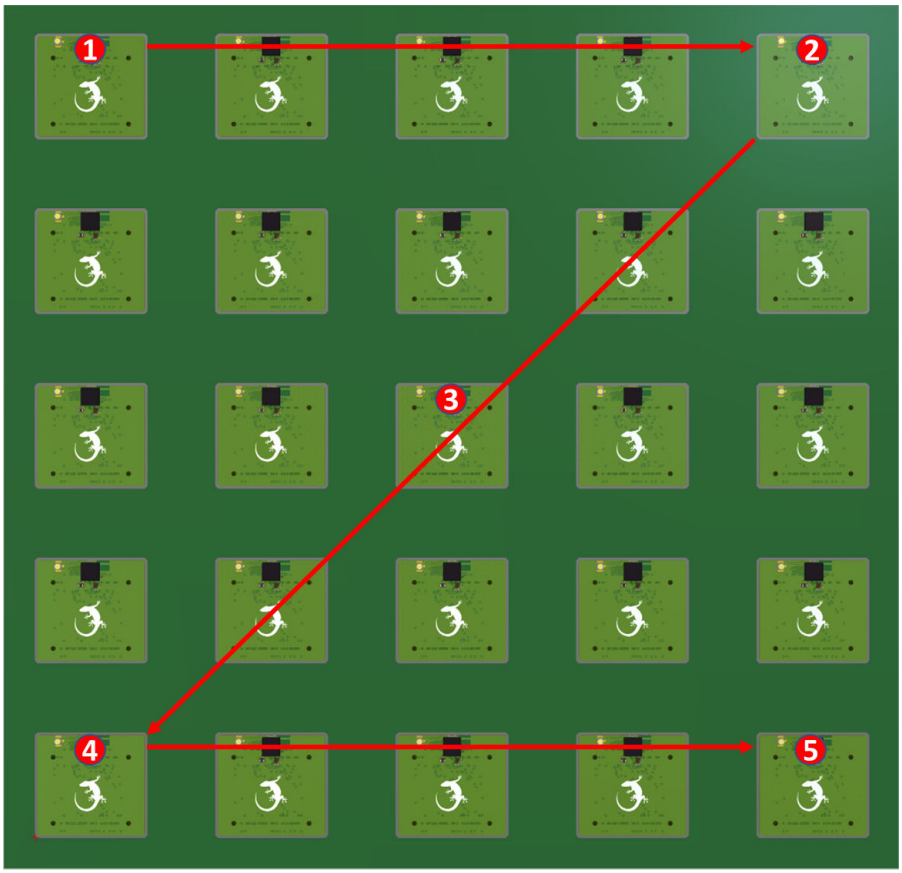


Figure 1.7. Example of Thermocouple Placement in a Panel of 5x5 Array

While determining the unit profile, it is possible that the Assembly Line Engineer will recommend some setup changes such as:

- Stencil thickness
- Aperture opening size
- Type of solder paste

As noted earlier, it is expected for customers to work with their contract manufacturer to make adjustments to solder temperature reflow profile, stencil thickness, aperture opening, etc. based on the specific board.

1.5.1 Reflow Oven Setup Example

Figure 2.8 shows an example of a full oven setup used to reflow a Silicon Labs SiP product.

Solder Paste Type: 96.5Sn/3.0Ag/0.5Cu SAC305 No-Clean Halide Free

Panel Size: 210.00mm x 152.50mm

Setpoints (Celsius)							
Zone	1	2	3	4	5	6	7
Top	132	152	177	197	198	253	259
Bottom	132	152	177	197	198	253	259
Conveyor Speed (cm/min):	44.0						

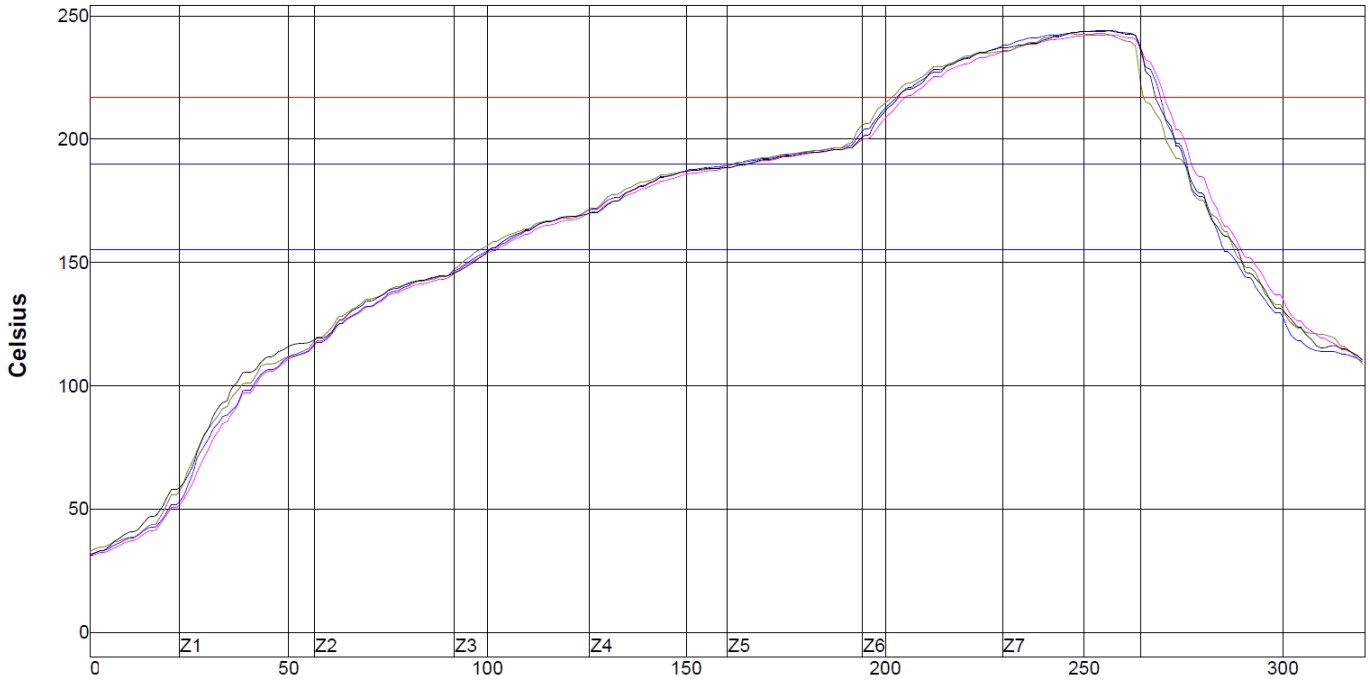


Figure 1.8. Example Profile of Oven with 7 Zones

Seconds

PWI= 41%	Max Rising Slope		Max Falling Slope		Soak Time 155-190C		Reflow Time /217C		Peak Temp	
<TC2>	2.56	11%	-4.20	-10%	63.07	10%	65.15	0%	242.28	-3%
<TC3>	2.57	14%	-4.59	-30%	61.82	6%	66.31	4%	243.78	17%
<TC4>	2.65	29%	-4.82	-41%	64.12	14%	63.24	-5%	242.90	5%
<TC5>	2.67	34%	-4.73	-37%	65.32	18%	64.56	-1%	244.01	20%
Delta	0.11		0.62		3.50		3.07		1.73	

Figure 1.9. Temperature Readings of Thermocouples Placed on the Component in Several Locations across the PCB Panel

Figure 2.9 shows the temperature readings of the thermocouple placed on the components in several locations across the whole PCB panel. The data logger shows the temperature measured by at least 4 thermocouples placed inside the oven. If carefully observed, when the zonal temperature is increased in Zone 1, there is an increase in the delta between the temperature measured by the thermocouples near 100 °C. Whereas when the zonal temperature is increased further in Zone 2, 3, 4, 5, the delta is minimum. This shows that there can be a wide temperature difference at different locations on the PCB panel at the same instance of time. It is important to note from the information produced by the data logger that the maximum temperature setting across any zone is not more than 259 °C (Zone 7). Whereas the device temperature does not exceed more than 245 °C. Thus, it should be noted that the zone temperature is different from device temperature and it has to be made sure that the peak temperature across any device is not exceeding 260 °C.

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.5) (Calculate Slope over 20 Seconds)	0.5	3	Degrees/Second
Max Falling Slope (Calculate Slope over 6 Seconds)	-6	-2	Degrees/Second
Soak Time 155-190C	30	90	Seconds
Time Above Reflow - 217C	30	100	Seconds
Peak Temperature	235	250	Degrees Celsius

Figure 1.10. Profile Process Window

Figure 2.10 shows the range of parameters assigned as the profile process window that the temperature oven setup should satisfy. In the above example, it can be seen that the thermometer readings shown in Figure 2.9 falls satisfactorily within the range specified in Figure 2.10.

2. Troubleshooting Guidance and Awareness

The following sections provide specific examples of issues observed with module manufacturing and guidance for observing and avoiding these issues. This is meant to provide guidance and awareness to customers but more specifically their contract manufacturers.

2.1 SiP Module Assembly Troubleshooting

As mentioned on the prior sections, SiP parts are built on laminate-based LGA package, and many contract manufacturers unknowingly treat these parts as QFN package. This results in unwanted assembly failures where troubleshooting after assembly becomes difficult. This section will help to narrow down the potential causes for the issue and help customers to troubleshoot their boards. Generally, it has been observed that assembly-related issues occur due to the following reasons:

- Violation of MSL rating
- Overheating and over-stressing the SiP component
- Excessive solder at pads
- Insufficient solder at pads
- Vias placed on the pads that are not filled and plated
- Improper solder reflow profile

Whenever an assembly failure is suspected with respect to SiP components, the investigation process should be as follows:

- Take a high-resolution x-ray of the board focused on the SiP (without removing the module from the board). See Section 3.1.1 Solder Reflow Issues.
  - Check whether there are any solder shorts
  - Check whether there are any solder voids greater than 30% of the pad area
  - Check if there are any solder spills
  - Check whether all the pins of the SiP module have contact with their intended land pad
- Depending upon the x-rays, verify whether a proper procedure for compliance to JEDEC standard for MSL rating was met by the contract manufacturer during the assembly or not. If not, then verify whether baking at the correct temperature for the correct duration of time was performed or not.
- Verify that the temperature profile complies to JEDEC standard as mentioned in Section 2.5 Unit Profiling.
- Look for visible stress or damage to the SiP module during the assembly.
- Look for package-to-footprint alignment issues.
  - Is the package lifted on one side?
  - Is the package offset from the footprint?

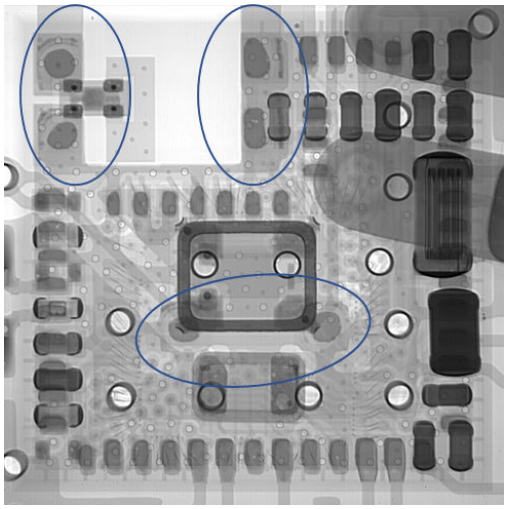
2.1.1 Solder Reflow Issues

It has been observed that a high-quality x-ray of the assembled SiP module can be very helpful in troubleshooting the assembly failures. There are several reflow issues that can be detected with a single x-ray image. The sections to follow provide x-ray images as examples of observations from these specific solder reflow issues.

Removing SiP module from the custom board for scanning x-ray is highly discouraged. To remove the SiP module from the board, application of the external heat will be required, which can damage the SiP further and an x-ray of that module may not provide fruitful results and thus, may not be helpful for troubleshooting anymore.

Some of the unacceptable reflow examples are shown in Sections 3.1.1.1, 3.1.1.2, and 3.1.1.3, followed by a good example of the reflow profile under Section 3.1.1.4.

2.1.1.1 Insufficient Solder



Issue:

Possibly caused by insufficient solder or reflow time above liquidus. Note that unfilled vias were inappropriately located underneath the package that could contribute to excessive unit movement and lift during the SMT process.

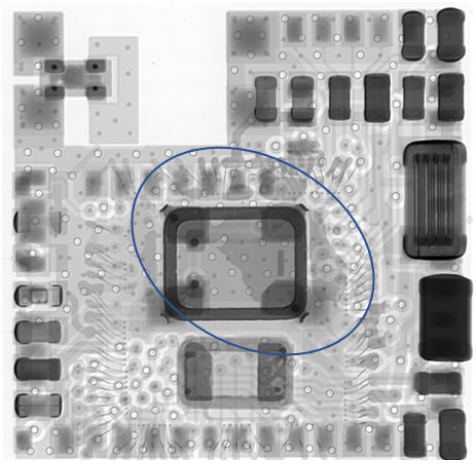
Symptoms:

- SiP does not function electrically as expected.
- SiP does not draw any current.

Solution:

- Verify temperature profile's specification.
- Fill vias and plate them under the package.
- Increase stencil's aperture opening.
- Increase thickness of the stencil.

2.1.1.2 Overheating/Delamination



Issue:

This is substrate delamination often caused by poor MSL handling practices or the material reaching excessive temperatures. The ramp rate of the profile must also be considered.

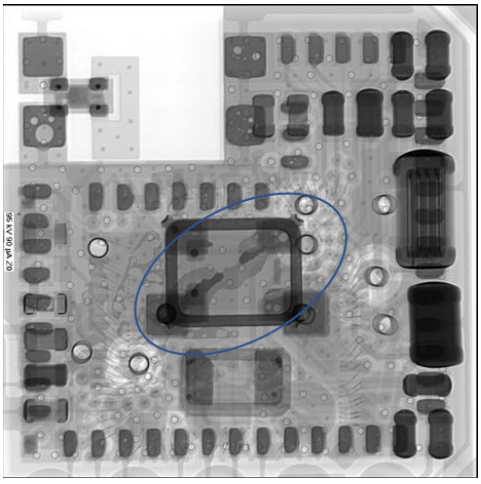
Symptoms:

- SiP overheats when power supply is applied.
- Most of the pads are short-circuited.
- SiP draws too much current.

Solution:

- Verify proper handling of the parts.
- Bake parts whenever in doubt about the MSL violation.
- Verify temperature profile's specification.

2.1.1.3 Improper Wetting



Issue:

Possibly caused by excessive solder quantity, component placement height, and/or long time above liquidous.

Symptoms:

- SiP overheats when power supply is applied.
- Most of the pads are short-circuited.
- SiP draws too much current.
- SiP does not rest flat on the PCB.

Solution:

- Decrease stencil thickness.
- Decrease stencil's aperture opening.
- Verify the amount of solder being applied at the pads.
- Verify height of the SiP when placed on the PCB before assembly.
- Verify temperature profile's specification.

2.1.1.4 Reflow Profile Example

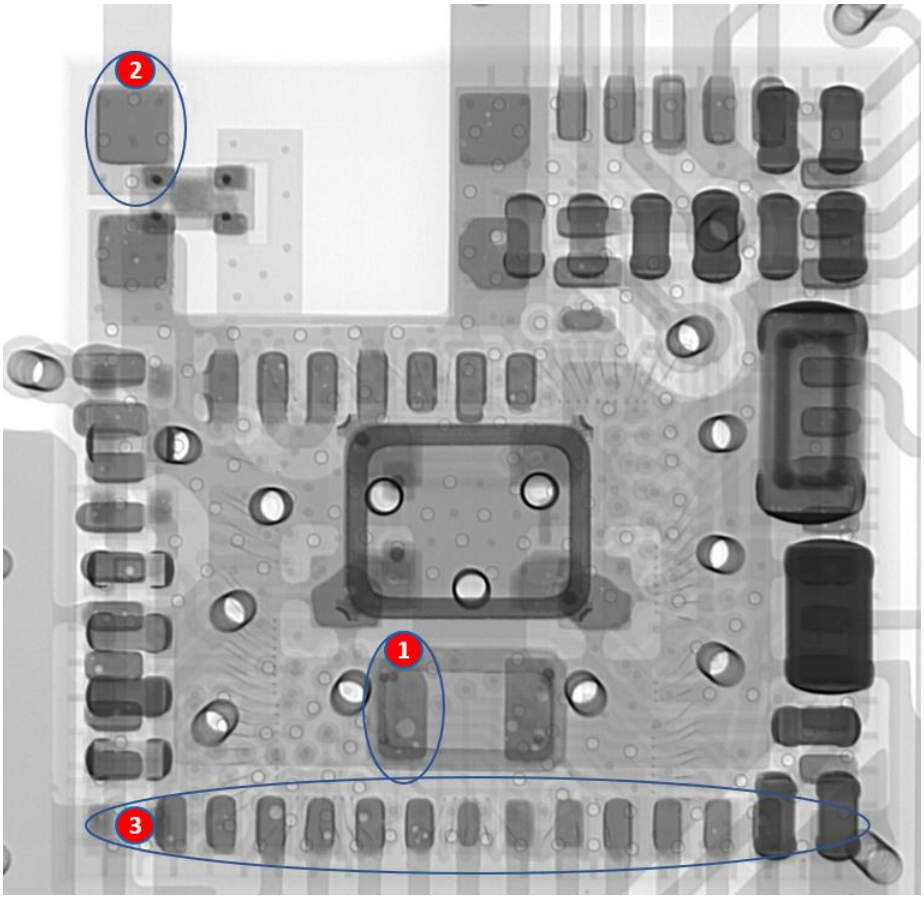


Figure 2.1. X-ray of a SiP Module Properly Soldered to a PCB

Figure 3.1 shows an example of the SiP module soldered properly to the custom PCB. In this image, it can be seen that all of the pads have been aligned and soldered perfectly to the PCB copper pads. It can also be seen that there are no solder spills or solder voids and the solder paste covers almost 100% of the pad after the reflow.

The markings in the image show the following:

1 - Even though there are some solder voids on the pad, solder paste coverage on the pad is still more than 80%, hence this type of reflow can be included under acceptable reflow example.

2 - Antenna pads and similar large copper pads have near to 100% solder paste coverage.

3 - All the pads at the perimeter of the package are perfectly aligned and has correct solder paste coverage.

2.1.2 SiP Module Do's and Don'ts

As discussed earlier, LGA packages can be easily confused as a QFN package. Hence it is very important to keep in mind that LGA packages have slightly different handling and assembling procedure when compared to QFN packages. Some general guidelines and considerations are given below when assembling LGA packages. Inability to follow these guidelines may affect SMT performance and final assembly results.

Do	Don't
Profile several device locations across the panel.	Profile the PCB with the assumption that all locations are at the same temperature.
Focus on a 1-to-1 PCB to Package land pattern perimeter pin design.	Focus on footprint's interior pins as the primary assembly reference point.
Vias underneath the device must be plugged and vias in the pad must be plated.	Use open vias underneath the device.
Address stencil design for paste coverage of 50-70% for large center e-pads.	Use excessive solder paste which exceeds past coverage that will result in solder bridging.
Use stencil thickness of 0.100 mm (4 mils) or 0.125 mm (5 mils).	Over-press units on to solder and board during component placement.
Stay within the recommended JEDEC settings.	Push the temperature near maximum rated reflow temperature i.e., 260 °C.
Reflow using a recently calibrated oven.	Use a hot air gun to attach components.
Follow the qualified JEDEC MSL handling requirements for the product.	Assemble with parts that have exceeded the out-of-bag and out-of-storage JEDEC recommendations. The material will require 24-hour baking at 125 °C before SMT use.
Acknowledge and interpret the Humidity Indicator (HID) card located within each lot shipment.	Assemble lots that have shown to be exposed to moisture. The material will require 24-hour baking at 125 °C before SMT use.
Bake any lots that are questionable for moisture exposure as per JEDEC requirement.	Take unnecessary SMT risks.

2.2 Setup Considerations

For a successful assembly, the Designer and Assembly Engineer have to consider multiple factors, of which a few are given below.

2.2.1 Stencil

The stencil and alignment are critical for the SMT process.

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.100 mm (4 mils) or 0.125 mm (5 mils). A factory may need to evaluate both thicknesses for the best results.
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads. A more conservative approach would be 80% as illustrated in Figure 3.1.
4. Center ground pads or e-pads underneath the device should partition the openings to achieve 50-70% overall past coverage.

2.2.2 Solder Paste

A No-Clean, Halide Free, Type-3 solder paste is recommended. This material type has proven to work well with the Silicon Labs LGA devices.

2.2.3 PCB Land Pattern

The recommended PCB Land Pattern design is often provided within the Silicon Labs product data sheets.

1. This Land Pattern Design is based on IPC-SM-782 guidelines.
2. All metal pads on the PCB are to be non-solder mask defined (NSMD).

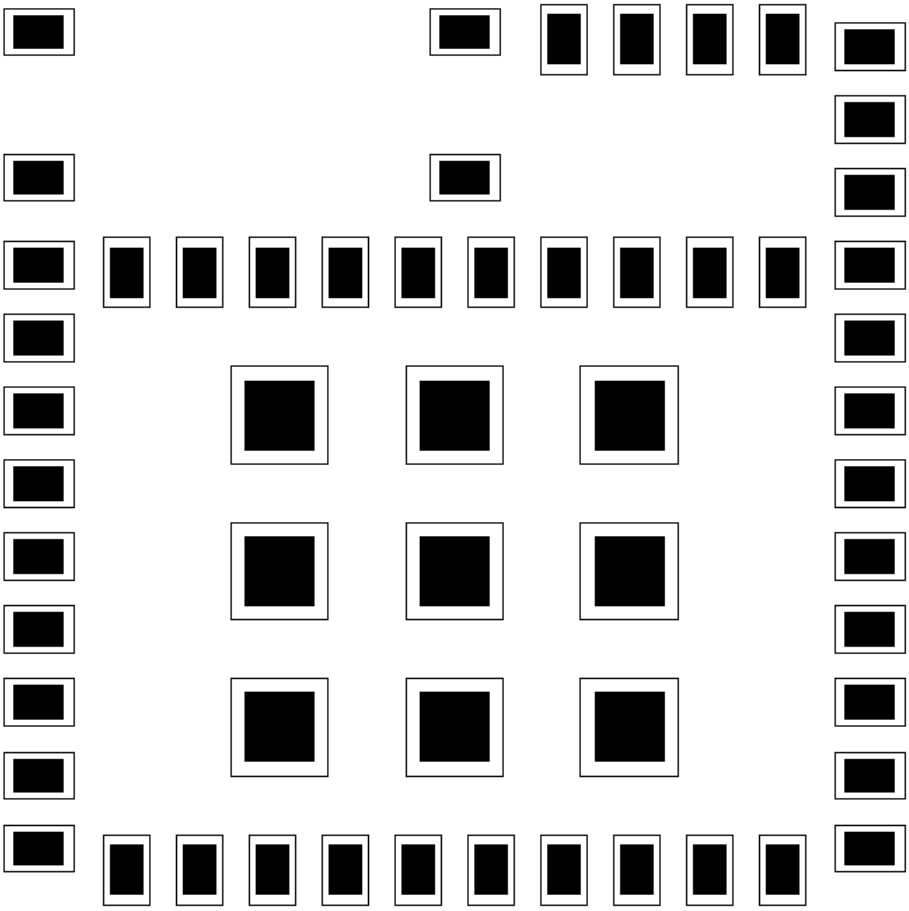


Figure 2.2. Example of PCB Land Pattern with 80% Paste Coverage Overlay

3. References

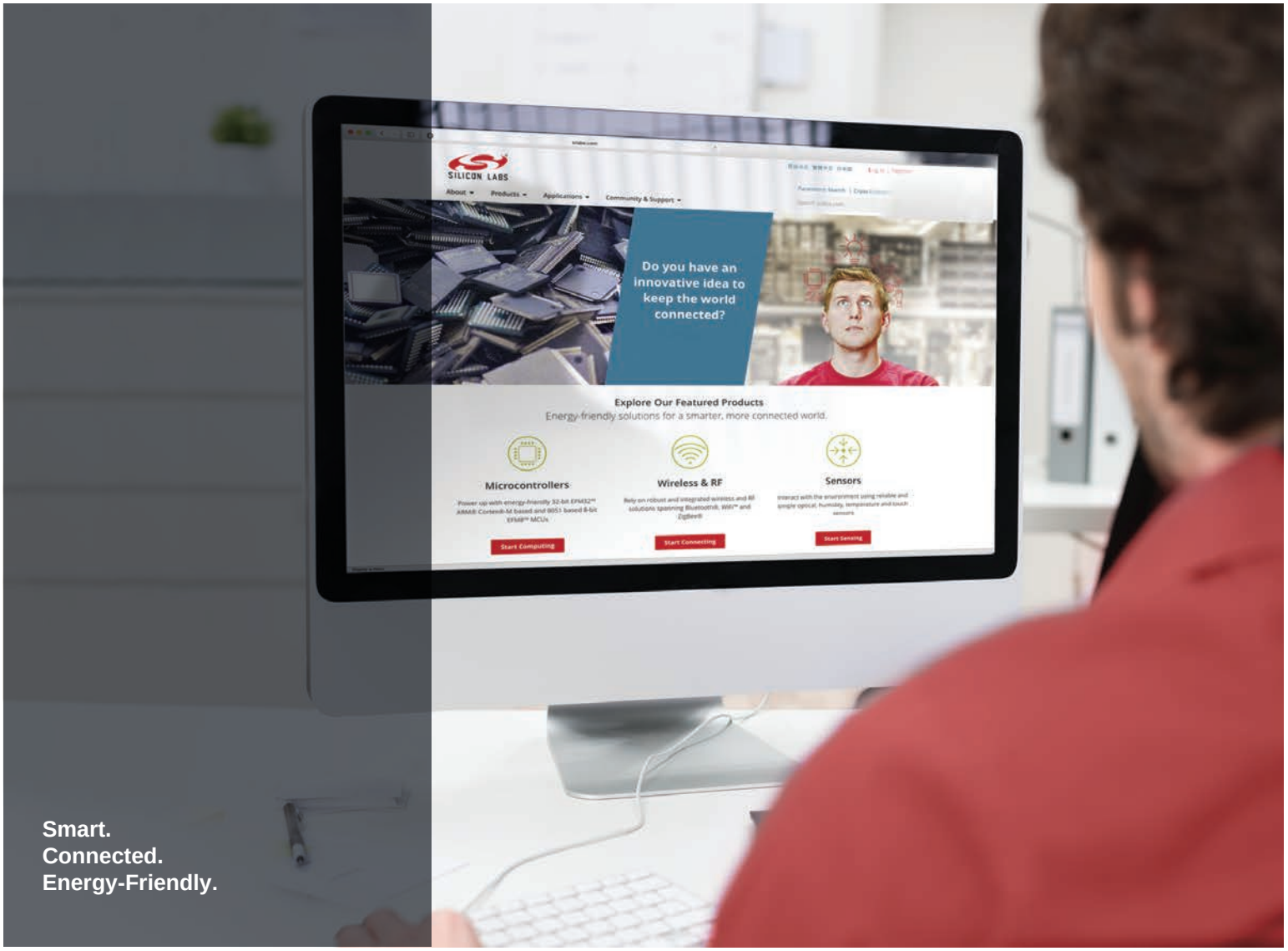
- IPC/JEDEC J-STD-020D - Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- ANSI Y14.5M-1994 - Dimensioning And Tolerancing
- IPC-SM-782 - Surface Mount Land Patterns (Configuration and Design Rules)

4. Revision History

Revision 0.1

October, 2019

- Initial release.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com