



AN1237: Si5332 Design Guidelines for Minimizing EMI

The Silicon Labs' Si5332 any-frequency, low-jitter, family of clock generators has broad appeal in many different products and markets, including data center, communications, broadcast video, and automotive. Available in both standard industrial (-40C to +85C) as well as automotive (-40C to +105C) grade options, the Si5332 can consolidate entire clock trees into a single device, saving board space, BOM cost, and minimizing quartz elements to increase system reliability.

System designers are often challenged with mitigating EMI and emissions in a high-speed design to meet internationally recognized standards, such as CISPR and FCC Part15. This application note introduces features within the Si5332 and PCB design techniques that can be implemented to minimize EMI.

KEY FEATURES

- Clock termination guidelines for best signal performance and minimal EMI.
- Circuit design and PCB layout techniques for minimization of EMI.
- EMI test data using suggested guidelines showing real EMI improvements.

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1. Introduction

Designing products from the start with EMI compliance in mind is a much more efficient process than attempting to “fix” compliance issues after a failing design has been built. This document provides design guidelines to help board level circuit and PCB designers create EMI-optimized Si5332-based designs from the start, thereby increasing the likelihood of quickly securing the required end-product EMI compliance certifications.

2. Clock Termination Guidelines

First, proper clock terminations, for both input and output clocks, are very important. Properly implemented clock termination supports both good signal integrity and EMI minimization.

- For differential clock formats:
 - Clock terminations are usually at the receiver end of transmission line unless format termination requirements dictate otherwise. Always keep terminations as close as possible to respective end of transmission line (i.e., keep source terminations near the source and receiver terminations near the receiver.)
 - Balanced termination is required to keep currents on differential pairs symmetrically out of phase, thereby promoting good field cancellation. Use termination components (typically resistors) with 1% or better tolerance.
- For LVCMOS clocks:
 - LVCMOS receivers are typically high impedance inputs operating **without** receiver termination.
 - It is important to match LVCMOS driver source impedance to PCB trace transmission line impedance. If driver source impedance is lower than PCB trace impedance a series termination resistor should be used. The value of the series source resistor should be chosen such that the driver source impedance plus series termination resistor is equal to PCB trace characteristic impedance. This series resistor should be placed as close as possible to the LVCMOS driver pin.
- General guidelines for both differential and LVCMOS:
 - Do not use a single Si5332 clock output to drive multiple clock receivers, regardless of driver format.
 - Always consult the [Si5332 Datasheet](#) and/or [Si5332 Reference Manual](#) for Si5332 specific input and output clock termination requirements. Do not assume Si5332 termination requirements are the same as other products or devices. Termination requirements will often vary from product to product.

3. General Clock Routing Guidelines for EMI Reduction

Clock signal routing can have the greatest impact on EMI reduction. Improper layout can result in a product that is virtually impossible to pass EMI compliance testing. Observing the following recommended layout design guidelines will help ensure your PCB layout supports best practices for EMI reduction.

- Route **all** clocks using **Stripline** techniques (see example layout in [6.1 Example EMI Test Board Clock Routing Details](#)).
- Perform all clock routing first to get best routing. Use 45 degree or curved turns only. **Keep differential pairs length matched** to avoid path delay skew.
- Use impedance-controlled routing for **all** clocks, both differential and single-ended. Typically, 100 Ω (or 85 Ω) differential, 50 Ω (or 42.5 Ω) single-ended.
- Use ground stitching vias to connect the ground planes along Stripline clock path on outside of differential pair (see example layout in section [6.1 Example EMI Test Board Clock Routing Details](#)).
- Keep the ground path between clock driver and receiver solid. Do not allow isolation cuts to separate the ground return path. Envision the Stripline clock path, including ground layers above and below the clock traces, as a continuous “tunnel” from driver to receiver that can’t be violated.
- Keep other signals as far away as possible or isolated from clock traces. If there is any potential for crosstalk from another signal on the same layer, use isolation grounds if required, but keep clock trace impedance constant. (i.e., there should be no clock trace impedance discontinuities due to other signal or isolation ground runs).

4. LVCMOS-Specific Clock Routing Guidelines

Single-ended LVCMOS clocks are notorious for being a source of EMI. To mitigate EMI due to LVCMOS clocks, it is highly recommended to use the following techniques for maximum EMI reduction

- **Configure all LVCMOS clock drivers as complementary.** In ClockBuilder Pro (<https://www.silabs.com/products/development-tools/software/clockbuilder-pro-software>), chose the “LVCMOS Comp.” driver type. Route both signals exactly as a differential pair following same routing rules as for true differential clocks



- Use one side of complementary LVCMOS pair as the intended LVCMOS clock
- Terminate the unused side of the pair as close as possible to the actual clock input with a capacitor to ground. The capacitor value must be the same as the receiving device's clock input capacitance. Choosing the proper value for this capacitor is important to balance the dynamic currents on each side of “differential” pair.

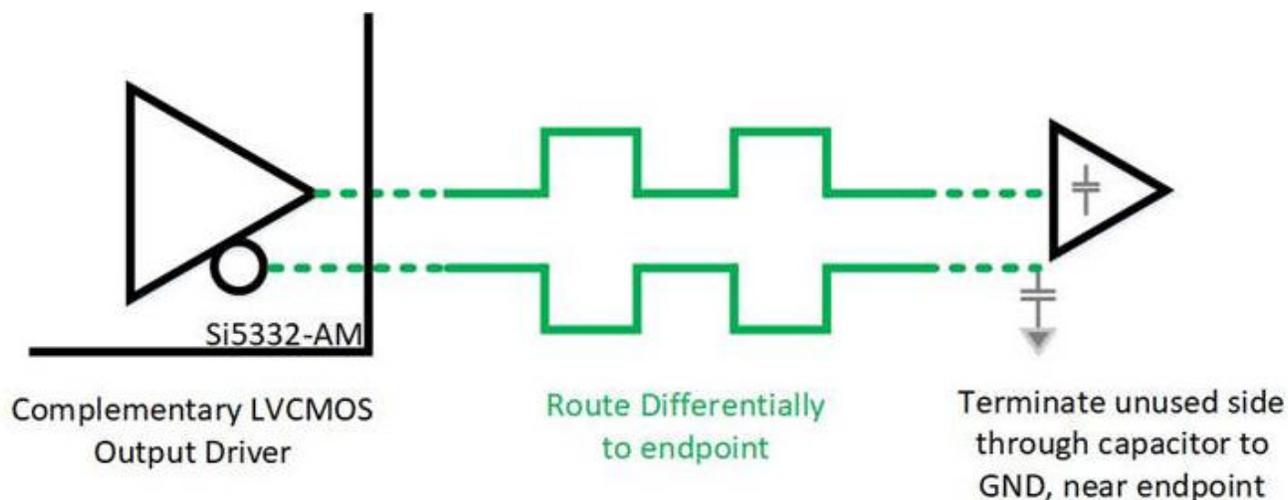


Figure 4.1. Complementary LVCMOS Clock Routing and Termination

5. Use of Balanced Differential Clocks Plus Stripline Routing is Best EMI Reduction Solution

There are many sources describing how use of Differential clocks can reduce EMI, but the key is having the differential pair implemented as a truly balanced differential pair.

See <http://www.emcs.org/acstrial/newsletters/summer10/DesignTips.html> for more information about why truly balanced differential pairs are best. Length matching (minimizing skew) and balanced loading (for matching rise/fall times and amplitudes) is very important to minimize EMI.

Even the best attempts at ensuring the differential pair is truly balanced can still result in some amount of radiated EMI components due to common mode radiation effects. In this EMI study: <http://www.sigcon.com/Pubs/edn/ReducingEMI.htm>, you can learn how common mode radiation can reduce the effectiveness of a differential-only EMI reduction solution.

Both studies point out how common mode radiation issues can become a factor when using simple Microstrip layouts, even if differential signals are used. This is the primary reason why using **Stripline** techniques is recommended instead of Microstrip. Stripline layout can contain residual common mode EMI as well as any differential field imbalance EMI. By combining Stripline clock routing, which provides Faraday cage shielding within the PCB, along with truly balanced differential signal field cancellation, the best of both solutions is realized.

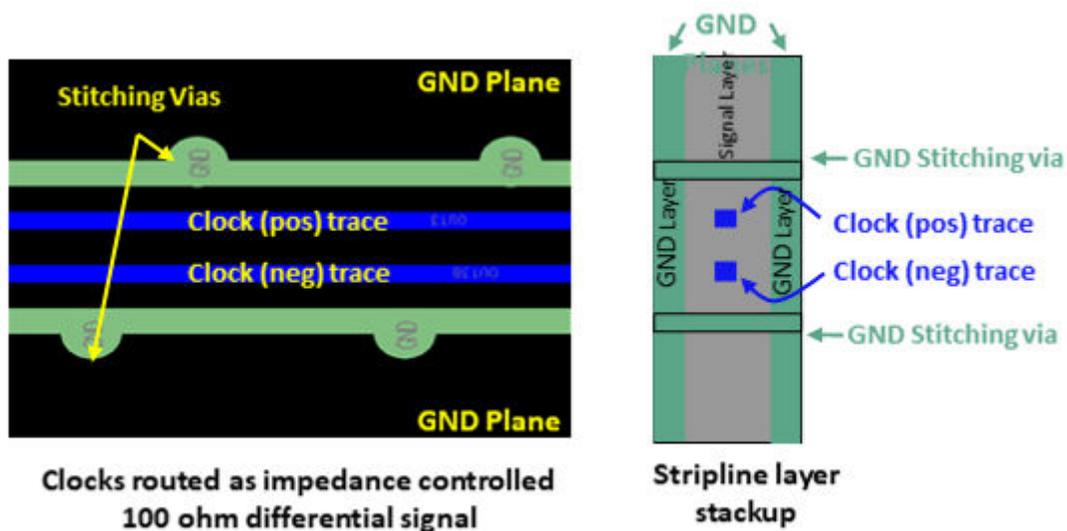


Figure 5.1. Example Stripline Clock Routing

6. Example EMI Test Board & EMI Test Data

To test and validate the suggested design/layout techniques presented in this document, Silicon Labs developed an evaluation board, the Si5332QFN40-AM2-AUTO-EVB, to represent a “real world” scenario. The PCB design comprised the following.

- Si5332-AM2, 8-output clock generator positioned in the middle of the PCB
- Eight clock outputs (combination of LVCMOS and LVDS) routed as balanced differential signals from the clock generator to end-points near the perimeter of the PCB
- Clock traces were routed in various lengths (2.55” to 6.14”) in serpentine fashion to emulate real-world design requirements
- Clocks were routed using Stripline technique and terminated as required at the header endpoint

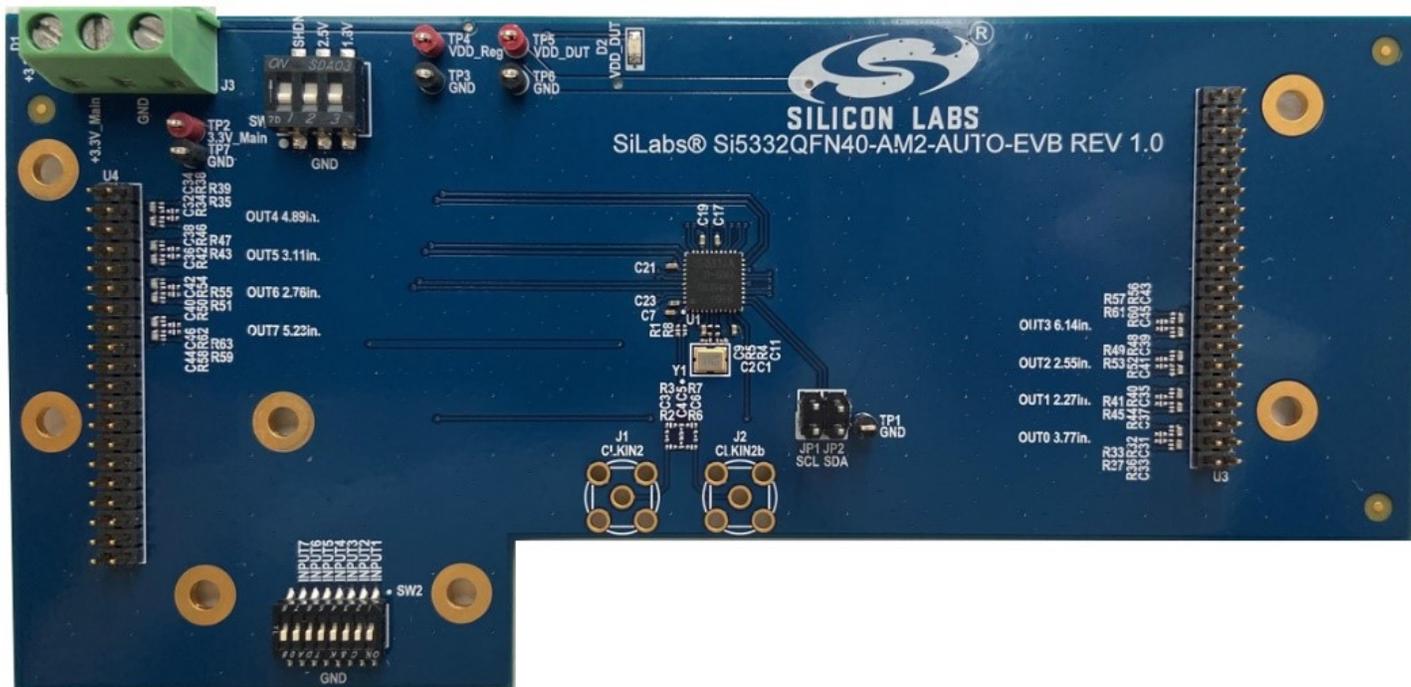


Figure 6.1. Example EMI Test Board & EMI Test Data

The above Si5332 test board was physically designed to fit within an automotive infotainment chassis enclosure (shown below) with the Si5332 test board being the only active circuit within the enclosure. This board + enclosure was tested for CISPR 25 EMI compliance to determine the level of radiated emissions due to the Si5332 clock generator test board independently of other emission sources.

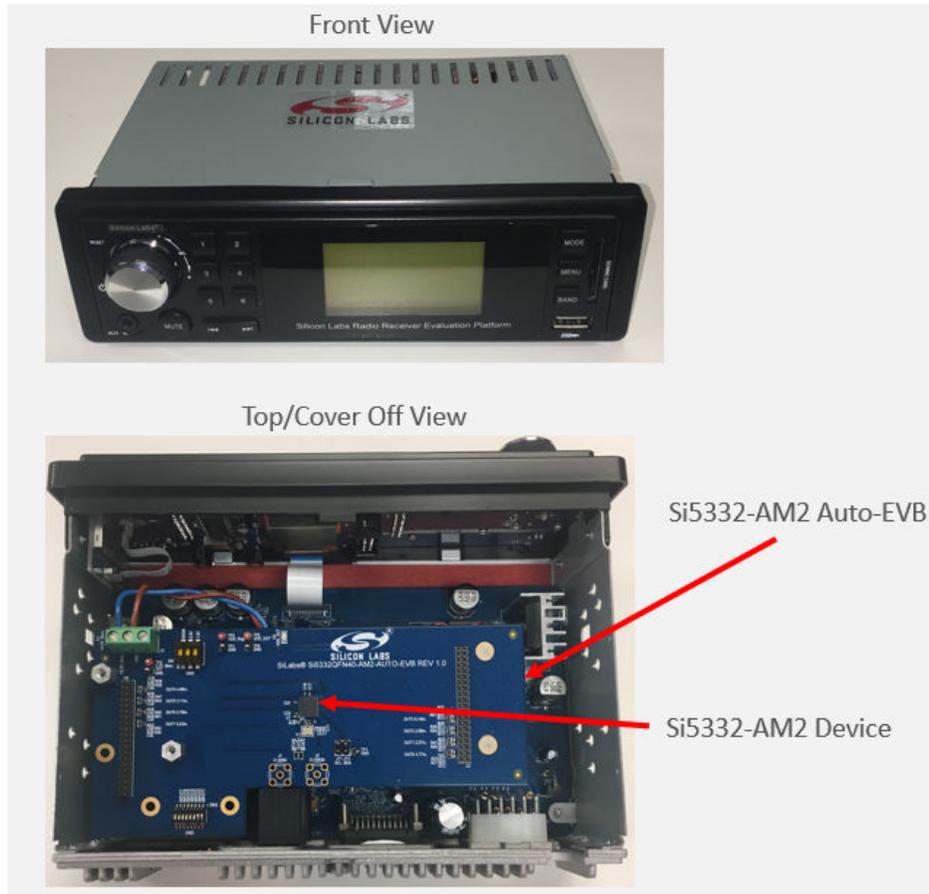


Figure 6.2. Automotive Style Enclosure

6.1 Example EMI Test Board Clock Routing Details

The images below provide a more detailed overview of the Si5332-QFN40-AM1-Auto-EVB board's clock signal layout. The clocks are routed using various lengths and paths towards the headers. The headers are used to simulate device pin loading. The required clock end point terminations can be seen immediately adjacent to the headers at the end of clock traces. Four clocks are routed to left header and four clocks to the right header. All clocks were routed using 100-ohm impedance controlled differential rules. The expanded views below show more detail of the Stripline layer stack-up and stitching vias connecting the ground layers above and below the differential clocks.

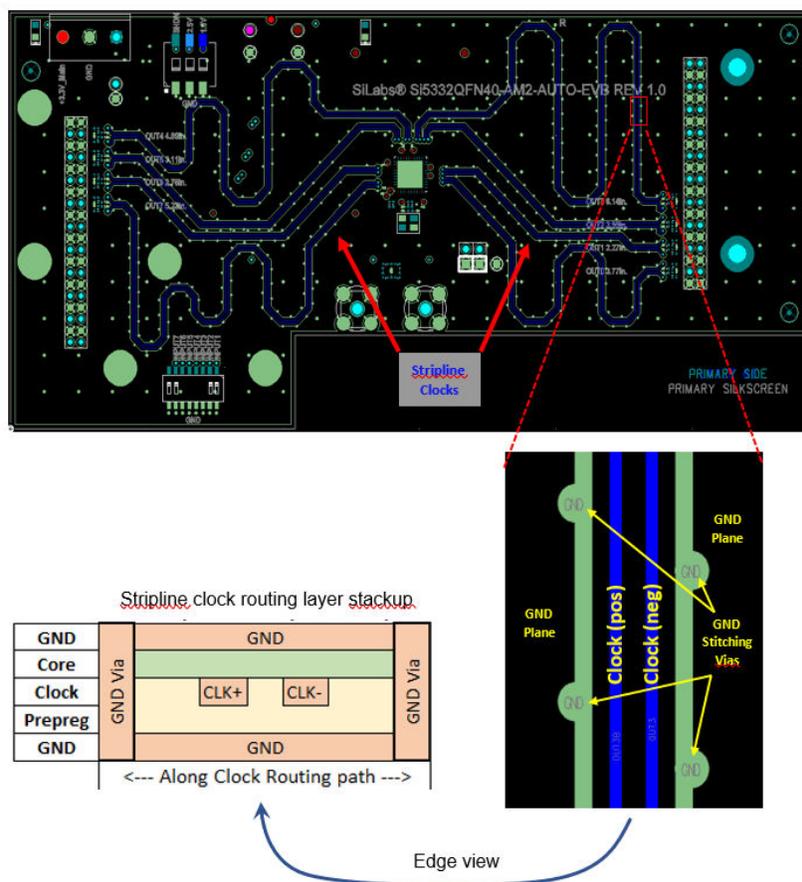


Figure 6.3. Stripline Layer Stackup of the Clock Layers

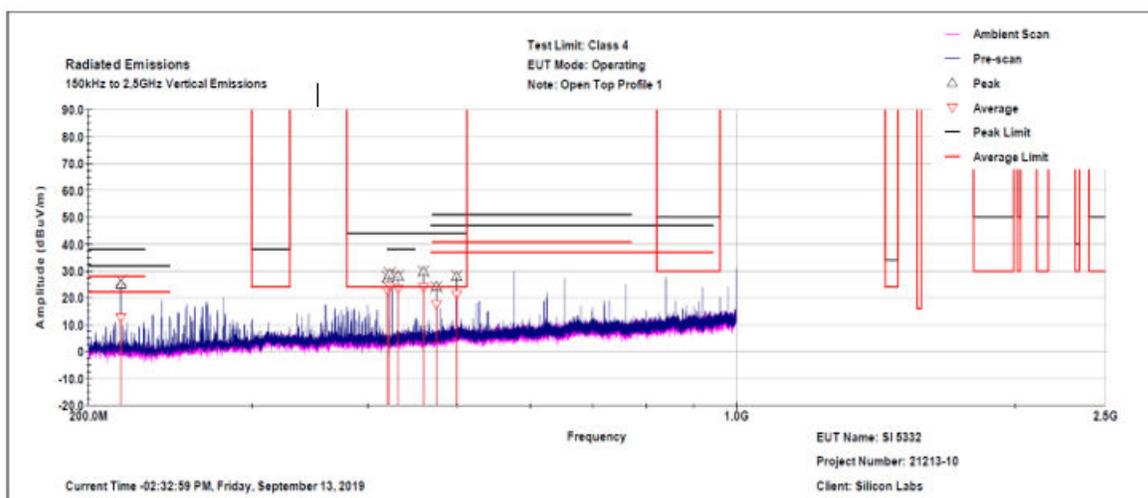
6.2 EMI Test Data

Si5332QFN40-AM2-AUTO-EVB board + enclosure EMI test data was collected at a certified EMI test lab anechoic chamber. Due to test lab limitations, CISPR 25 Class 4 EMI limits were used instead of the most stringent Class 5. Emissions data was collected with an open enclosure (top open, board facing antenna) as well as totally closed enclosure to quantify both the emissions from the board itself as well as the added attenuation provided by the enclosure. The Si5332 device was loaded with 3 different frequency profiles and testing was done using each profile shown below. Profile 1 used single ended LVCMOS, profile 2 used complementary LVCMOS, and profile #3 is an actual existing automotive infotainment system frequency profile and is using a mix of differential and complementary LVCMOS.

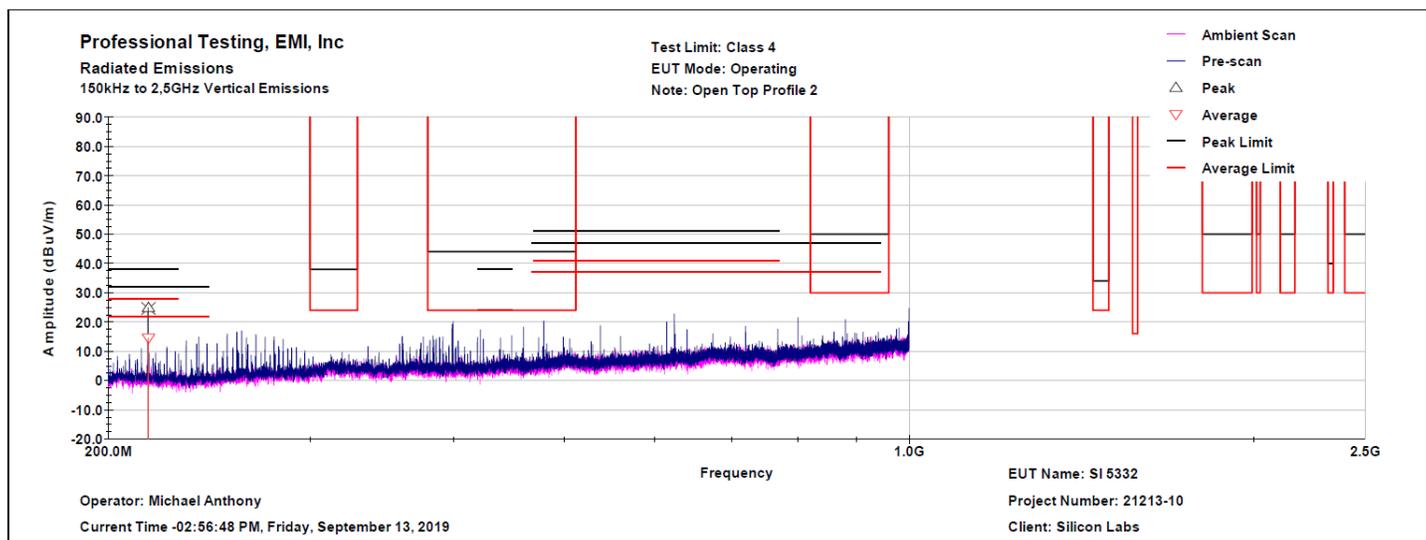


Figure 6.4. Frequency Profiles

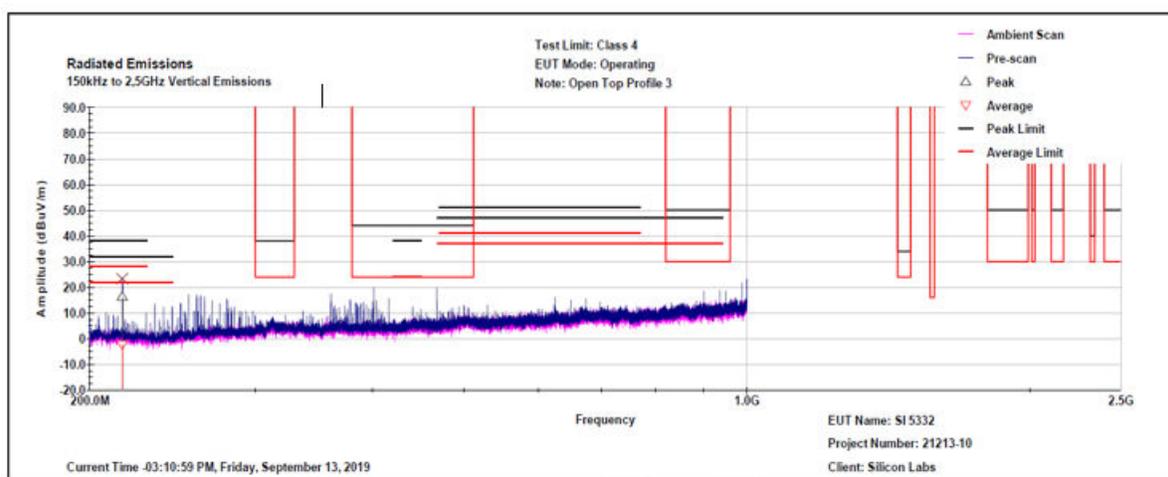
Below are the radiated emissions for profile #1 (single-ended LVCMOS) with the enclosure **top cover open**. Spurs are evidently present and only a few are exceeding Class 4 average spec levels, none exceed the peak spec levels. These are single ended LVCMOS contained in an embedded Stripline “cavity” within the PCB. Spur levels would probably be much higher if these clocks were instead on a surface layer of the board.



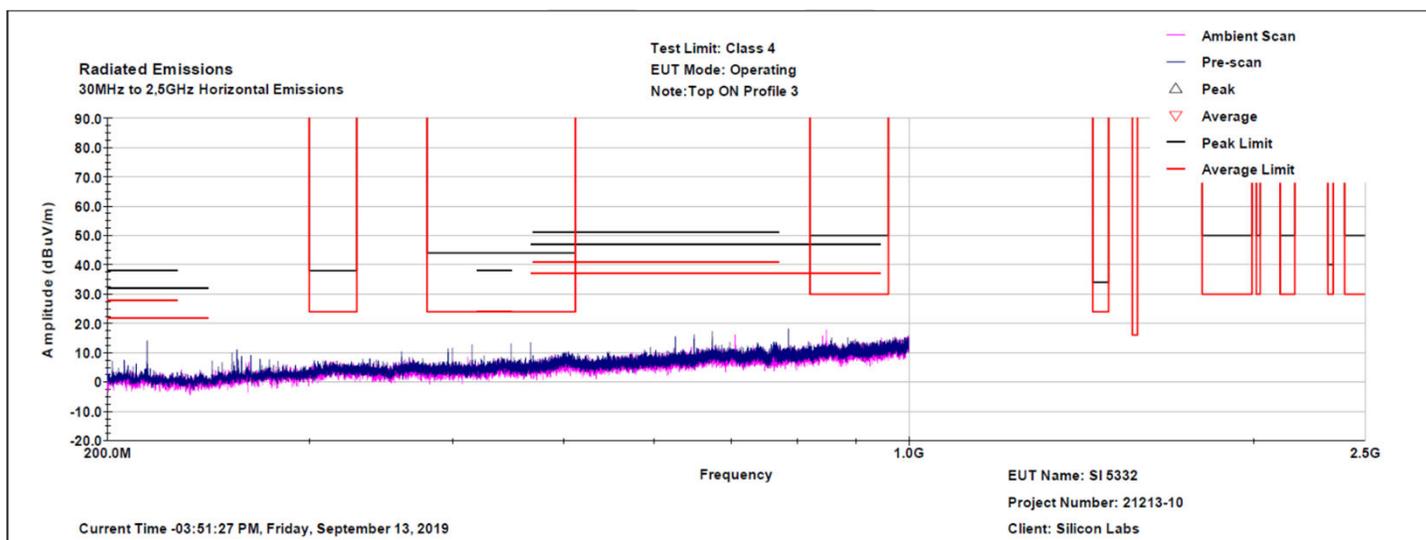
Below is EMI plot for profile #2 (complementary LVCMOS) with enclosure **top open**. Note the reduction in radiated spur amplitude (about 10 dB lower) due to changing to complementary LVCMOS. All DUT mid-band generated spurs are well below limits with a single lower frequency spur that is now well below both peak (**black** levels) and average (**red** levels) limits.



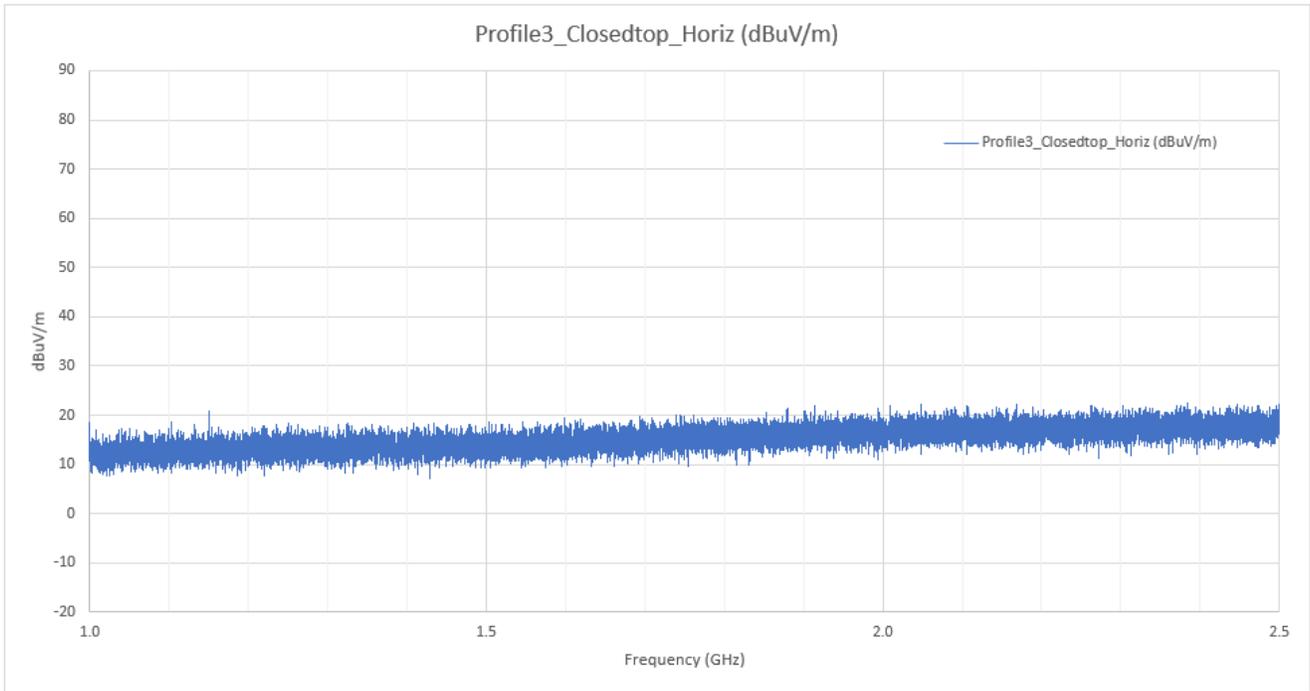
Next is profile #3 with enclosure **top open**. DUT spurs are also well below limits with lower frequency spur much lower in amplitude. This would easily pass Class 4 limits (with ~20 db margin) without the enclosure top cover on.



Finally, below is profile #3 with enclosure **top closed**. This DUT configuration is most representative of an enclosed automotive assembly undergoing EMI testing. Note the improvement (~ 10 dB) from previous plot once the enclosure top is closed.



Below is the captured spectral emission data for same DUT configuration as above, but over 1.0 GHz to 2.5 GHz range. Note the lack of spurious emissions above 1 GHz.



7. Conclusion

The EMI test data presented here supports the conclusion that clocks from a central source, such as the Si5332 clock generator, can be routed across a board to multiple destinations in a manner supporting regulatory EMI compliance. Following the clock circuit design guidelines and PCB layout design guidelines explained in this application note are key to achieving this goal.



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