AN1423: SiWx917 RF Matching and Layout Design Guide

The SiWx917 SoC is a 2.4 GHz Wireless Secure MCU with a comprehensive multiprotocol wireless subsystem. This application note provides a description of the RF matching network designs for both external and internal (TX-RX Direct Tie) RF Switch configurations. The layout design principles are also presented, which should be followed along with the matching guidelines for optimal RF performance.

Refer to the data sheet of the device for additional information regarding the hardware configuration of the SiWx917 SoC.

Note: This application note is referred to as "RF Integration Guidelines" in the data sheet of the device.

KEY FEATURES

- Provides an overview of RF matching procedures for both external and internal (TX-RX Direct Tie) Switch configurations.
- Specifically discusses design procedures for the PA and LNA impedance transformation networks.
- Presents and compares simulation and measurement data.
- Shows the layout design guidelines on the available Silicon Labs Radio Boards.
- Provides measurement data for alternative RF Switch and BPF parts.

1. Introduction

The SiWx917 RFIC is a 2.4 GHz wireless MCU that supports the following protocols:

- 802.11 ax(20 MHz)/b/g/n (ultra-low-power, low-cost, and high-throughput)
- Bluetooth Low Energy (BLE 1 Mbps, 2 Mbps, and long-range modes)

This document provides the technical details and description of the matching solutions applied on the publicly available Silicon Labs reference radio boards. The matching networks discussed in this document are targeted for single-band applications and use SMD 0201 size discrete components in the RF path. The matching networks can be designed with an external RF Switch or with the use of the internal switch, where the TX and RX paths are simply connected after their respective matching networks (TX-RX direct-tie topology).

The layout design of the matching circuit is critical to achieve the targeted TX power, RX sensitivity, and power efficiency while suppressing the harmonic content of the signal. Silicon Labs suggests copying the RF part of the reference PCB designs, or if that is not possible, applying the layout design rules and guidelines described in this application note.

The matching efforts strive to simultaneously achieve the following criteria:

- Provide the desired nominal TX output power level (measured at the connector to the antenna, load).
- Obtain this nominal TX output power at the nominal supply voltage.
- Achieve desired PA output linearity (e.g., good EVM performance) when using the SiWx917's high linear OFDM PA.
- Provide optimal RX Sensitivity.
- Minimize current consumption (i.e., maximize power efficiency).
- Comply with regulatory specifications for spurious emissions (e.g., especially TX harmonics) with the help of an additional Band Pass Filter (BPF).

2. RF Architecture Overview

The device comes in a QFN package with a dimension of 7x7 mm, 84-pin. The pinout is shown in the figure below (the 2.4 GHz RF I/O pins are highlighted with a red box).

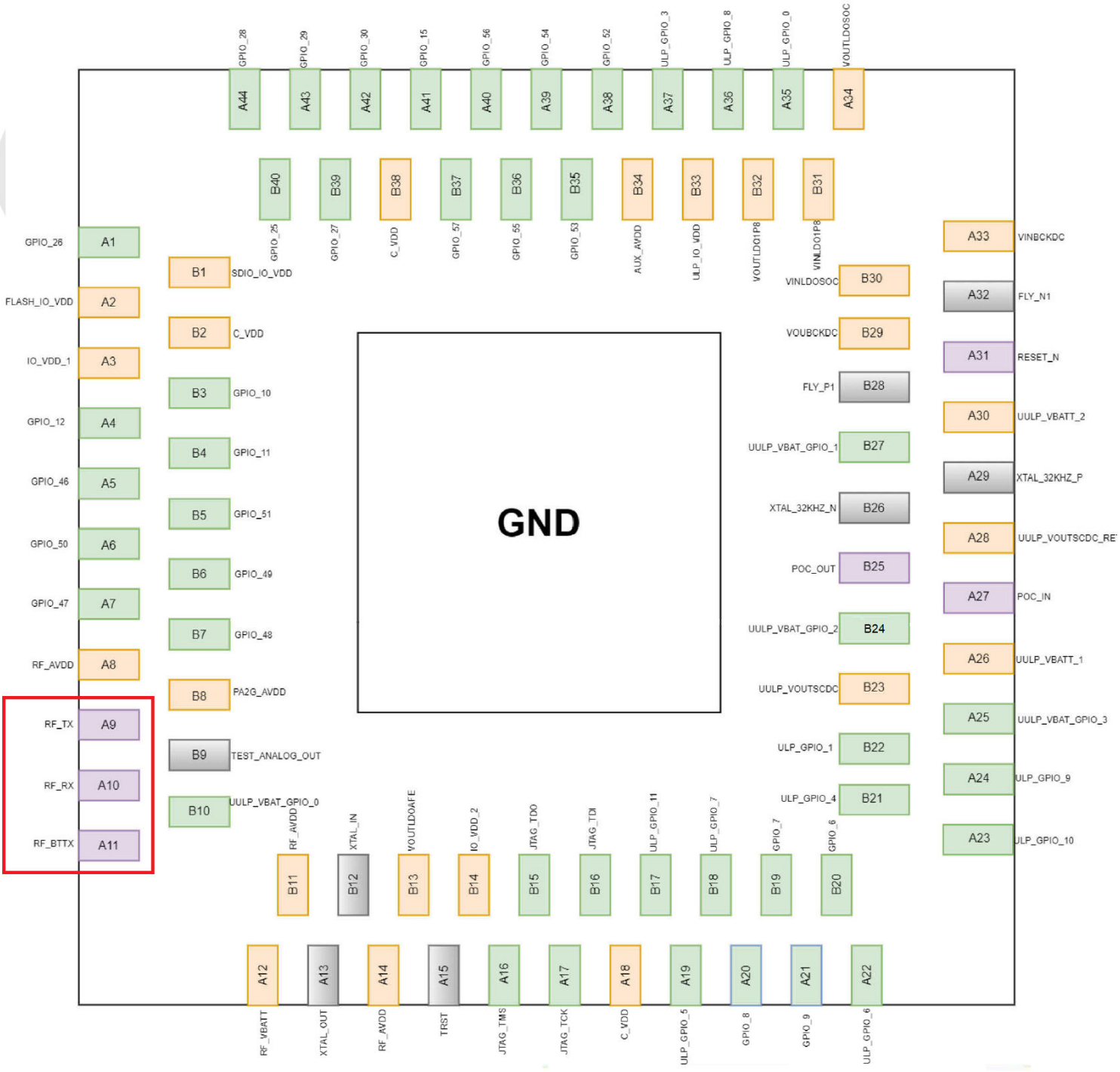

Figure 2.1. SiWx917 QFN84 (RF I/O Pins Highlighted)

The device features a Wi-Fi and BLE transceiver. The bond-outs for the Wi-Fi and the different BLE operational modes are the following:

- Wi-F or BLE/BT for 20 dBm high power: RF_TX and RF_RX serving as the TX and RX ports respectively.
- BLE/BT for 0 dBm low power: RF_RX serving as both the TX and RX ports.
- BLE/BT for 8 dBm high power: RF_BTTX and RF_RX serving as the TX and RX ports respectively.

The block diagram of the 2.4 GHz RF front-end is shown in the figure below. The bond-outs for the different operational modes mentioned above can be verified.

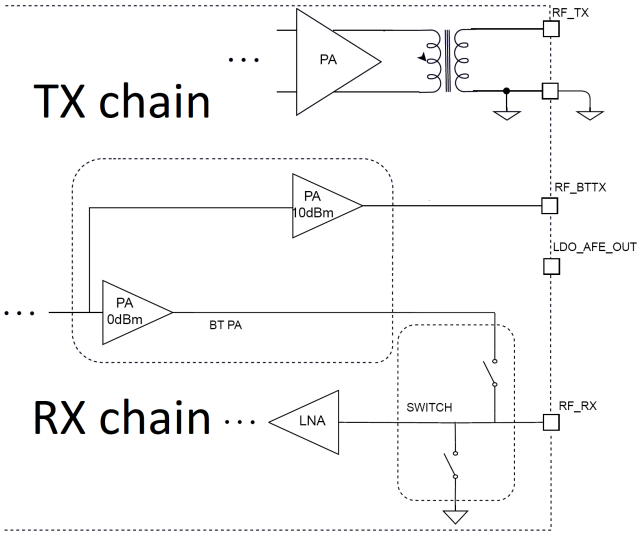

Figure 2.2. Block Diagram of the TX and RX Subsystems

The power supply management of the different power amplifiers (PA) are the following:

- Wi-Fi or BLE/BT for +20 dBm high power: A differential Class-AB mode PA and an internal balun for TX power of +20 dBm with PA (output stage) voltage of 3.3 V (PA2G_AVDD = 3.3 V recommended for maximum output power).
- BLE/BT for 0 dBm low power: A single-ended Class-D mode PA for TX power of 0 dBm with biasing through resistive feedback (RF_AVDD = 1.4 V recommended from the internal dc-dc buck converter).
- BLE/BT for +8 dBm high power: A single-ended Class-AB mode PA for TX power of +8 dBm with open drain output externally biased from VOUTLDOAFE (= 1.1 V) through a choke inductor (RF_AVDD = 1.4 V recommended by the internal dc-dc buck converter).

The LNA in the RX chain is also a configurable subsystem with the following three modes:

- High-power (for Wi-Fi or BLE/BT +20 dBm)
- Low-power (mainly for Wi-Fi standby mode)
- Low-power (for BLE/BT +8 dBm and 0 dBm)

The two different matching topologies (BRD4338A and BRD4340B) with recommended component values are shown below:

1. **All three RF ports used**: 2-element discrete CL and LC matches of the RF_TX and RF_RX ports which connect to an external RF Switch (alongside the RF_BLE_TX port with a 6 – 10 nH inductor connecting to VOUTLDOAFE). The RF Switch requires 8.2 pF dc-blocking capacitors on all its RF ports.

   The matching network of the RF_RX port is simultaneously optimized for the three LNAs and the BLE/BT 0 dBm low-power PA.

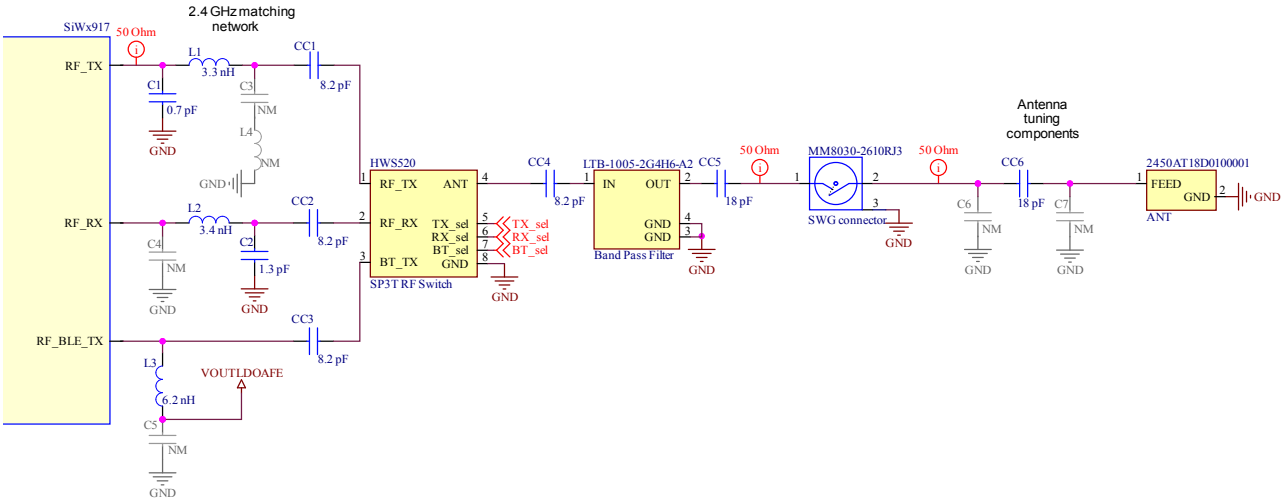

Figure 2.3. RF Schematic of the BRD4338A Radio Board (with External RF Switch)

Table 2.1. Recommended Component Part Numbers

Reference Designator	Component Value	Part Number	Manufacturer
L1	3.3 nH	LQP03TQ3N3B02D	Murata
L2	3.4 nH	LQP03TQ3N4C02	Murata
L3	6.2 nH	LQP03HQ6N2H02	Murata
C1	0.7 pF	GRM0335C1HR70WA01D	Murata
C2	1.3 pF	GRM0335C1H1R3WA01D	Murata
CC1, CC2, CC3, CC4	8.2 pF	GRM0335C1E8R2BA01D	Murata
CC5, CC6	18 pF	GRM0335C1H180GA01	Murata
Band Pass Filter		LTB-1005-2G4H6-A2	Mag.Layers
SP3T RF Switch		HWS520	Hexawave

2. **RF_TX and RF_RX used**: 2-element discrete CL and 1-element L matches of the RF_TX and RF_RX ports, which connect to one another in a common Direct Tie point with a shunt C matching capacitor (the switching logic is controlled internally).

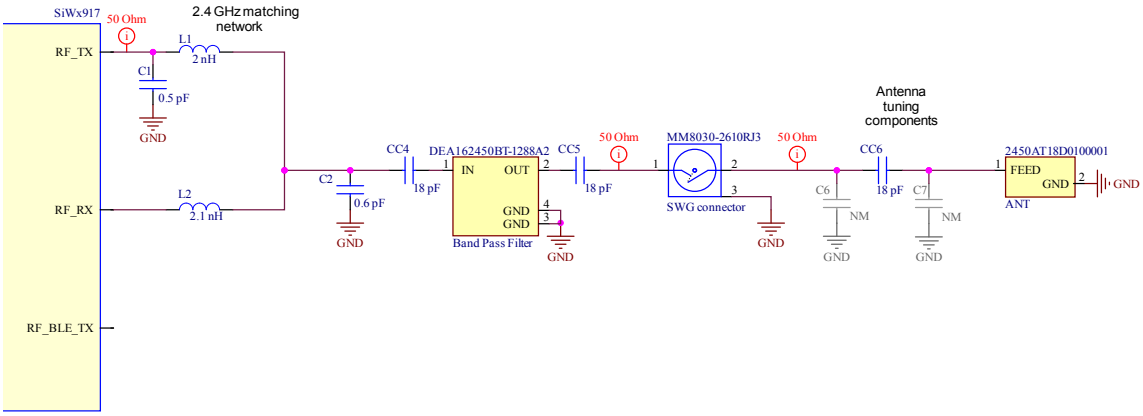

Figure 2.4. RF Schematic of the BRD4340B Radio Board (Direct Tie)

Table 2.2. Recommended Component Part Numbers

Reference Designator	Component Value	Part Number	Manufacturer
L1	2.0 nH	LQP03TN2N0B02D	Murata
L2	2.1 nH	LQP03TN2N1C02D	Murata
C1	0.5 pF	GRM0335C1HR50WA01D	Murata
C2	0.6 pF	GRM0335C1HR60WA01D	Murata
CC4, CC5, CC6	18 pF	GRM0335C1H180GA01	Murata
Band Pass Filter		DEA162450BT-1288A2	TDK

In both matching networks, a Band Pass Filter (BPF) is used in the common single-ended path following the matching networks (or the RF Switch) to suppress the out of band frequency contents of the signal even in the low frequency domain (e.g., in case the SoC is used in the proximity of a GPS transmitter).

The recommended BPF for the Direct Tie matching network is DEA162450BT-1288A2 due to its more robust 2nd harmonic suppression.

The impedance transforming effect of the external RF Switch and BPF are also thoroughly investigated in this application note in the later chapters.

3. RF Matching Design Step I. –with External RF Switch

The 2.4 GHz RF matching design consists of the following steps:

1. Determine the optimum termination impedance for the PA.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the PCB have a major effect, so tuning/optimization of the design is required. An optional EM simulation can be done here, but simulations with well-estimated PCB parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

Notes:

1. The first step has been performed by Silicon Labs and is an attribute of the internal PA (see Table 3.1 Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz on page 8). These determined values can be used as a basis for custom matching network designs and there is no need to re-measure them by the user.
2. Steps 2 to 5 are only necessary if the matching network and layout design are different from the recommendations in this application note. If the reader follows these matching and layout guidelines strictly, RF performance is expected to be close to that of the Silicon Labs radio boards, and simulation/bench tuning may not be needed.
3. As the RF Switch and BPF have a characteristic impedance of 50 Ω, this chapter focuses on designing the TX and RX matching networks - that precede those components - to transform the SiwX917 PA output impedance to 50 Ω. Then, the RF Switch and BPF can be placed at the output of the matching networks without any major design concerns in terms of impedance transformation due to their 50 Ω characteristic impedance. However, most components are not perfectly ideal, and the PCB traces that follow the RF Switch and BPF are also not exactly 50 Ω, which means that there can be impedance transformations introduced by the RF Switch and BPF, which will be presented in later chapters.

3.1 Determine the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the 2G4RF_IOP pin if 50 Ω termination is applied at the antenna port.

The RF_TX and RF_RX port terminations determine the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver and receive maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX and vice versa in RX mode. The two metrics mentioned translate to high TX output power and good RX sensitivity. Maximizing the harmonic suppression property of the TX matching network is not the highest priority as the BPF provides that property, but the chosen low BOM cost, low-pass matching network topology also enhances the filtering at high frequencies.

The ideal termination impedance of the RF_TX and RF_RX pins are determined by load pull testing to satisfy the PA design criteria.

The RF_TX and RF_RX port output impedance measurements have been performed by Silicon Labs.

Table 3.1. Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz

Operation mode \ Pin	RF_TX	RF_RX
TX	65 + 10j Ω	6 + 30j Ω
RX	200 + 220j Ω	23.5 – 16.5j Ω

The optimum termination impedance of the RF_TX and RF_RX pins can be approximated as the the complex conjugates of the values in Table 3.1:

Table 3.2. Optimum Termination Impedance of the RF_TX and RF_RX Pins @2.45 GHz

Operation mode \ Pin	RF_TX	RF_RX
TX	65 - 10j Ω	-
RX	-	23 + 16.5j Ω

Notice that Table 3.1 contains the measured output impedance of the ports in their disabled state (TX port impedance in RX mode and vice versa). This information is particularly important when designing the Direct Tie matching network, as the inactive TX or RX paths must show high enough impedance to the signal in the other operational mode to ensure lossless signal transmission between the active RF port and the antenna (or vice versa). Therefore, these so-called “off-mode” port impedances will be used in the Direct Tie matching network simulations.

3.2 Choose the RF Matching Topology

The two recommended topologies are presented in Section 2. RF Architecture Overview.

The matching network design procedure in this chapter is presented for the matching network with the RF Switch (BRD4338A). The Direct Tie matching network (BRD4340B) will be detailed in Section 4. RF Matching Design Step II. – with Internal RF Switch (TX-RX Direct Tie Connection) , as that requires more theoretical considerations.

3.3 Initial Design with Ideal, Loss-Free

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free, ideal capacitors and inductors are used and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization.

Using the free tool Smith V4.1, the matching network can be simulated, but only with a real port impedance. As the SiWx917 RF port impedances are complex (65 + 10j Ω for the TX and 23 – 16.5.j Ω for the RX port), a different approach to the simulation must be used. Two methods can be used, which are demonstrated for the TX port below:

- **Method 1**: Consider the 50 Ω for the source to be the ANT port. Place a 65 + 10j Ω load and consider it to be the SiWx917 TX input port, which results in a 65 + 10j Ω point in the Smith-chart. The matching procedure is then to transform this impedance to the center (50 Ω) point by placing discrete components between the source and load. This method is applicable because if the output impedance of the matching network is a complex conjugate matched to antenna termination (50* Ω = 50 Ω), the input impedance of the matching network is – consequently – also a complex conjugate matched to the SiWx917 TX input port (which is essentially the design goal). This method is recommended as the matching network is displayed “left to right” as on the schematic.
- **Method 2**: Consider the 50 Ω for the source to be the SiWx917 TX input port even though it is not 65 + 10j Ω. Place a 50 Ω load and consider it to be the ANT port, which results in a centered point in the Smith-chart; the matching procedure is then to transform this impedance to the goal 65 – 10j Ω point by placing discrete components between the source and load.

The two matching methods for the **TX** path are demonstrated in the figures below:

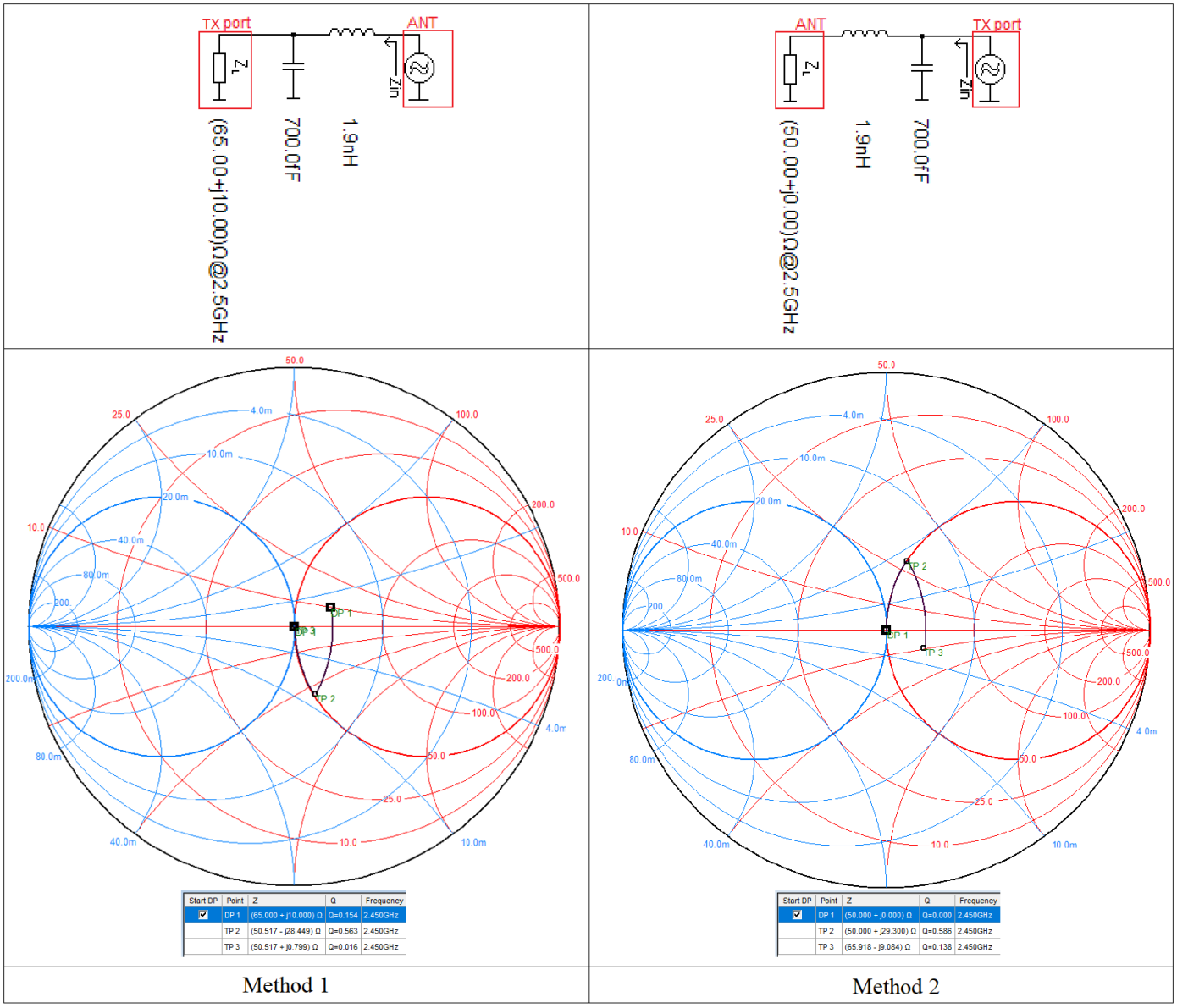

Figure 3.1. The Two Matching Methods for the TX Path

The two matching methods for the **RX** path are demonstrated in the figures below:

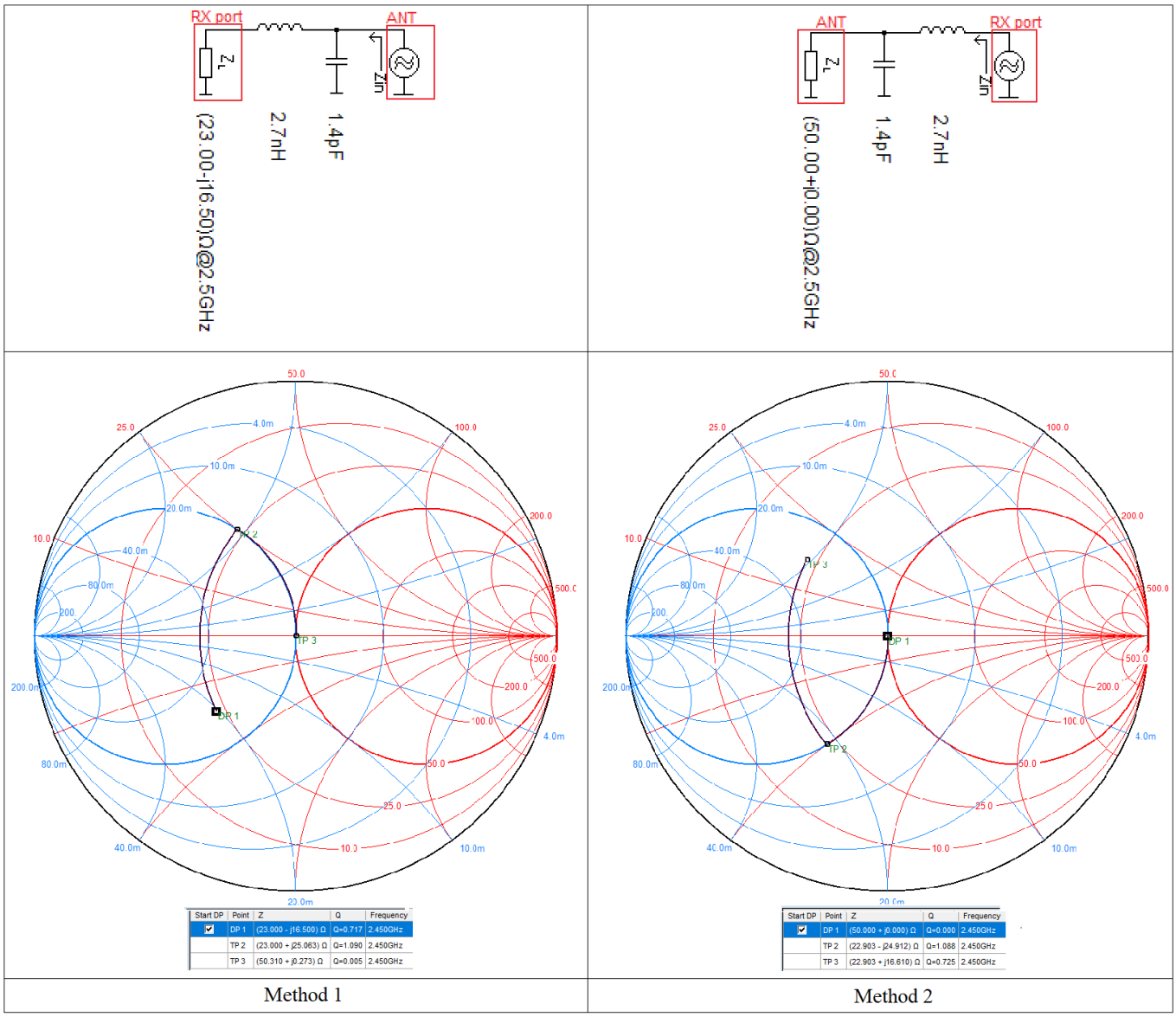

Figure 3.2. The Two Matching Methods for the RX Path

3.4 Design with Parasitic and Losses

3.4.1 Effects of SMD Discrete Parasitics and Losses

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the used SMD components and the PCB parasitic effects need to be considered during the matching network design. The SMD components at these high-frequency ranges behave as a resonator. A capacitor can be realized by a series RLC resonant circuit, while an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L-C components and can have considerable series parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. For more details, refer to the SMD manufacturer website at www.ds.murata.co.jp, in regards to the appropriate SMD equivalent circuits.

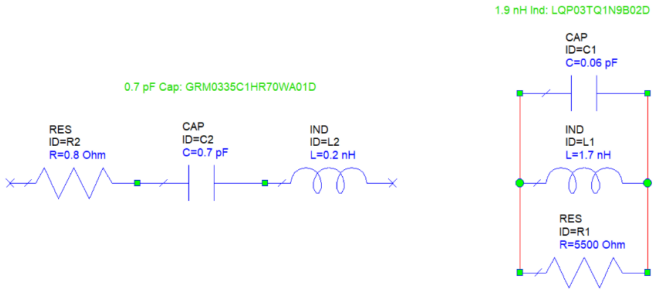

Figure 3.3. Equivalent Circuits of Real SMDs at the Fundamental Frequency (2.45 GHz)

The SPICE circuit models above can be replaced with the S parameter files of the components, which can also be found on the Murata website.

Whichever method is chosen, the simulation results are expected to get closer to real-life circuit behavior. Therefore, optimization of the component values at this step is required. See how SMD parasitics detune the TX and RX matching networks in the figures below (matching procedure Method 1).

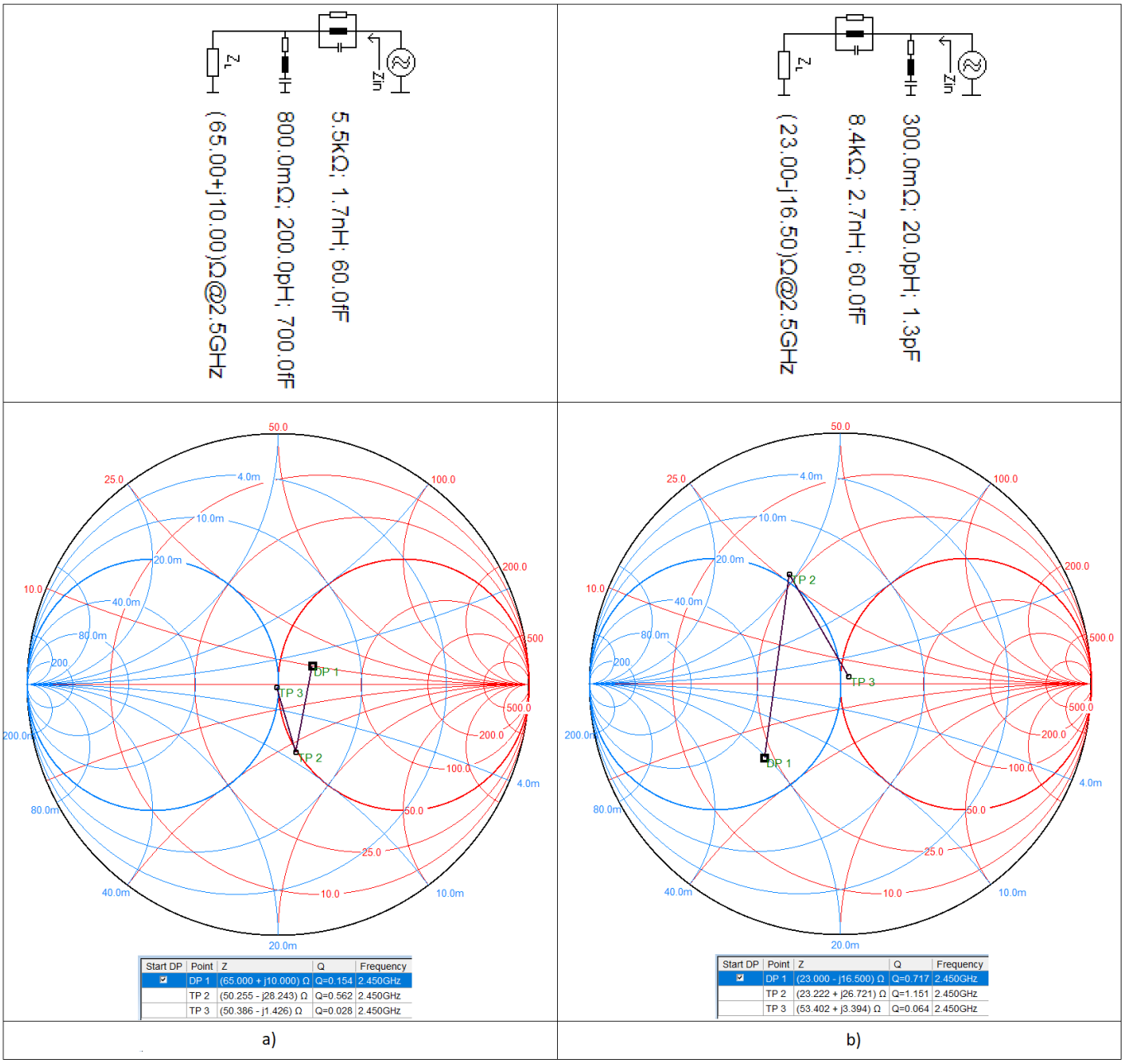

Figure 3.4. Detuning Effect of the SMD Parasitics a) TX Match b) RX Match

As shown in the figure, the SMD parasitics do not significantly detune the impedance in the simulations.

3.4.2 Rough Estimation of PCB Parasitics

3.4.2.1 Lumped Element Model

In addition to the discrete parasitics, the following PCB trace parasitics also have significant effects:

- Series inductances (denoted by Ls)
- Parallel capacitances (denoted by Cp)
- Losses (not prominent with short traces)

These trace parasitics usually enforce the further decrease in values of matching elements (series inductance and parallel capacitance). There are three approaches to simulating PCB parasitics: lumped element, distributed element, and EM-based. Since the trace lengths in the match are usually shorter than 1 mm (much lower than the wavelength at 2.4 GHz), even the simple lumped element method provides good accuracy. The most accurate is the EM-based method, but that usually requires expertise and expensive CAD tools.

As the distance between the TOP and the 1st inner GND layer is 70 µm (instead of the traditional 350 µm), the 1st inner GND layer is closer to the traces than the TOP layer GND pour on the sides. The consequence of this is that the RF traces can be considered as microstrip lines instead of grounded coplanar waveguides (CPWG), as the EM field is concentrated more between the RF trace and the GND layer than between the RF trace and the TOP layer GND pour on the sides, thus the propagation mode can be considered a microstrip instead of CPWG. The trace inductances and capacitances can therefore be calculated for either type of transmission line of the two, as they transform to each other for such geometries as explained above. One can confirm the statement above by changing the gap distance between the RF trace and the side GND pour in the calculator; it does not affect inductance or capacitance per mm if the first inner GND layer is closer to the RF trace.

The PCB layout parasitics are calculated using Grounded CPW calculator.

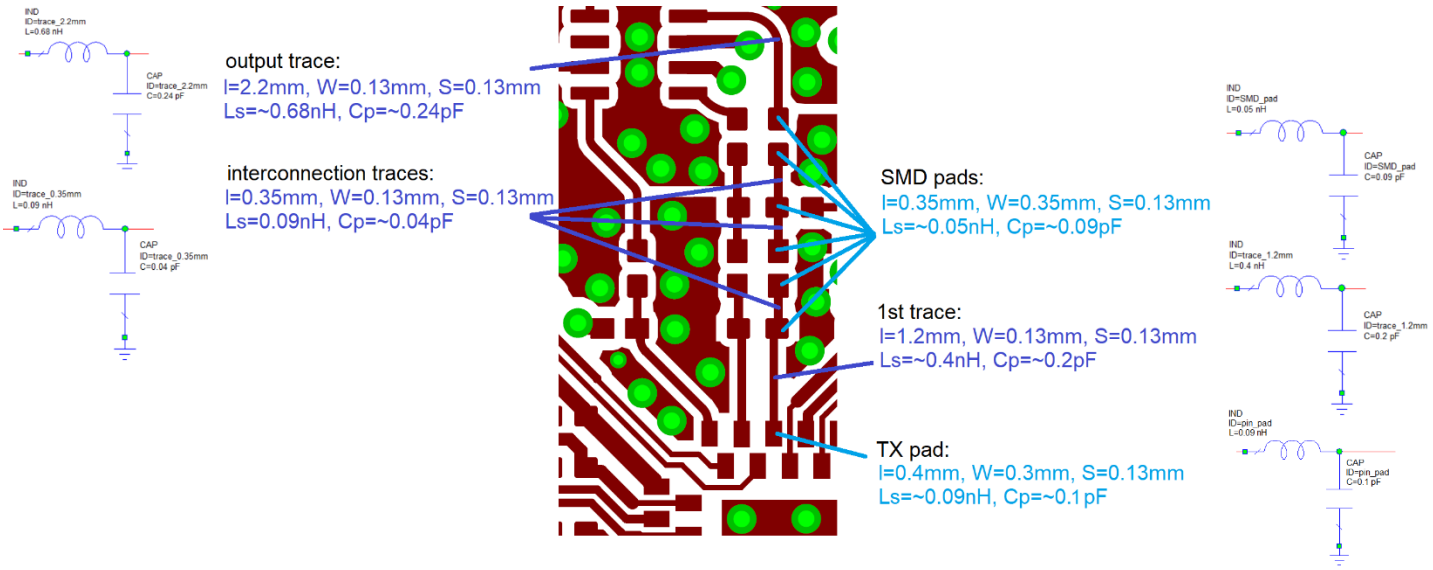

Figure 3.5. Calculated PCB Layout Lumped Element Parasitics of the TX Path on Radio Board BRD4338A

Using the C = 0.7 pF and L = 1.9 nH component values determined above in the ideal and SMD parasitic simulations, it will be evident that the PCB layout detunes the matching network significantly, as can be seen in the simulation figures below.

The AWR Design Environment simulations in this chapter will show multiple ZIN input impedance points on the Smith-chart for both the TX (left) and RX (right) paths:

- Parasitic free simulation (repeat of Figure 3.1 The Two Matching Methods for the TX Path on page 9 and Figure 3.2 The Two Matching Methods for the RX Path on page 10)
- SMD + PCB layout parasitics simulation with lumped parasitics (Figure 3.5) and EM-solver based parasitics (Figure 3.7 Model for the EM Simulation of the SMD and PCB Layout Parasitics in CST Studio Suite on page 15 later) for the TX, and accordingly, for the RX paths.

Both the RF pin side and termination side ZIN input impedances are plotted for a full picture on the quality of the match. It is worth mentioning that by theory, a perfect match on the pin side of matching network also means a perfect match on the termination side, while a mismatch on the pin side (quantized by the mismatch loss) results in a similar mismatch on the termination side. Note that the ZIN impedance points with similar mismatch loss are aligned on a circle (~VSWR circles) around the goal impedance, which means that the mismatch caused by a component change in the matching network is described by the radial distance of the Smith-chart point from the goal impedance. This occurrence explains why there can be a visually large Smith-chart point transformation around a circle on the termination side compared to the visually small transformation on the RF pin side (in certain cases). The radial change always remains around the same.

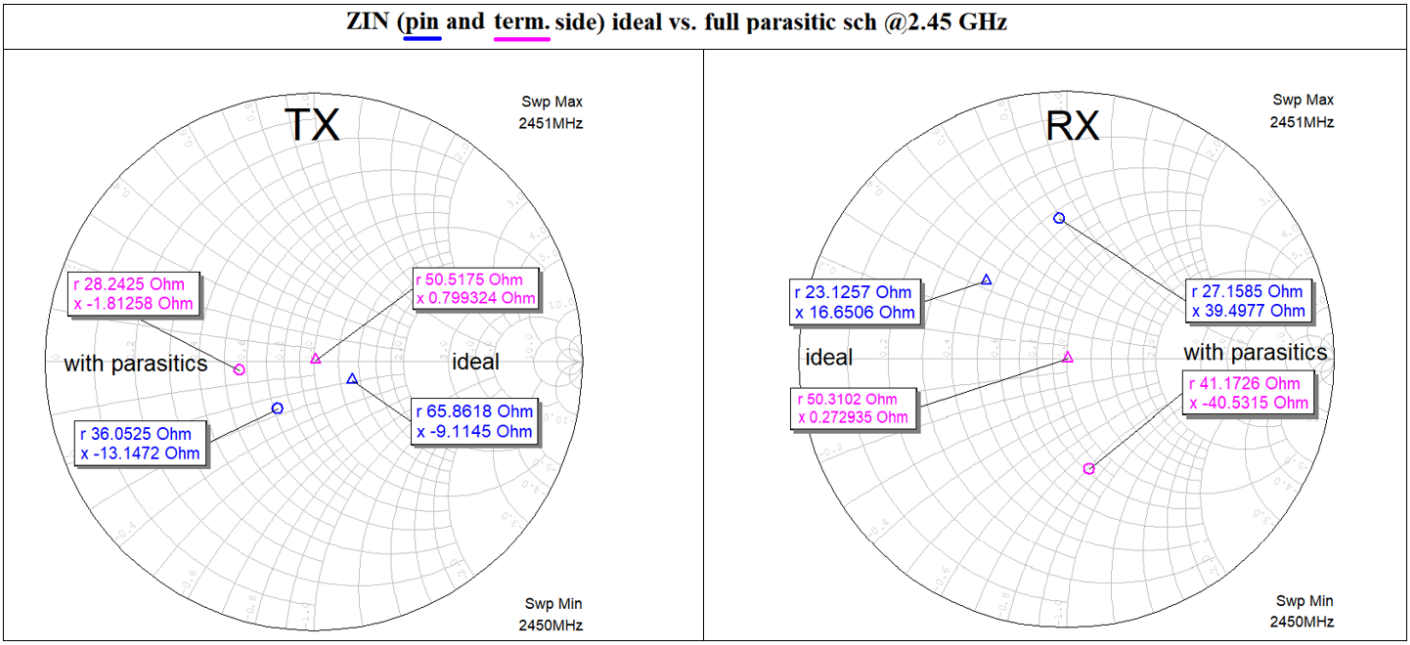

Figure 3.6. Impedance Transforming Effect of the SMD and PCB Layout Lumped Element Parasitics on BRD4338A (with Initial Simulated Values)

The simulation results show that the PCB layout parasitics detune both the TX and RX matching networks from their design impedance goals when using the component values determined by the ideal or SMD parasitic simulations.

The parasitics simulations above suggest that it is necessary to change the component values. Section 3.5 Conduct RF Bench Testing and Tuning – Effects of the RF Switch and BPF will show that using the recommended components of BRD4338A shows simulation results that align with the VNA measurements.

Before the VNA measurements are presented, the EM simulation method is shown which inherently takes the layout parasitics into account.

3.4.2.2 EM Solver Method

EM solvers (e.g., CST Studio) are powerful tools, not only for antenna design or EM field distribution simulations, but for matching network designs. An advanced technique with the help of such a software is the following:

1. Simulate the PCB layout with SMD component 3D models. Set up 50 Ω lumped ports at the place of SMD components, RF Switch, BPF, and the TX, RX, ANT ports.
2. Run the simulation (solver of choice) and export the simulated CST Touchstone file into AWR.
3. Place the matching network components (ideal, lumped parasitics, or Murata S parameter file), RF Switch, and BPF S parameter models (if available) and TX, RX, ANT terminations to the appropriate ports.
4. Tune the matching network to see the goal TX and RX port impedances of Table 3.2 Optimum Termination Impedance of the RF_TX and RF_RX Pins @2.45 GHz on page 8.

With this method, the PCB layout parasitics are an intrinsic property of the S-parameter Touchstone file.

The EM simulations were performed in the fundamental 2.4 – 2.5 GHz band.

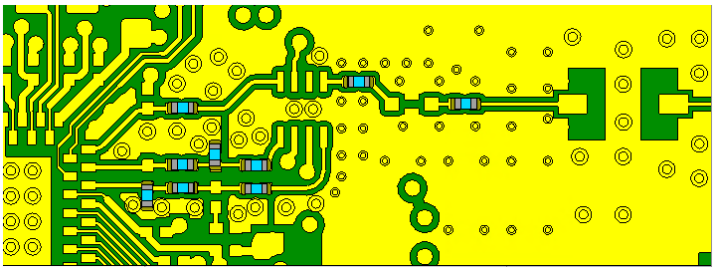

Figure 3.7. Model for the EM Simulation of the SMD and PCB Layout Parasitics in CST Studio Suite

A part of the AWR schematic is shown in the figure below that shows the RX and TX ports, and the TX matching components (with Murata S-parameter files). This schematic is for the TX matching network; hence the TX (on) and RX (off) ports are given values according to the TX mode operation values of Table 3.1 Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz on page 8. Note that this section covers the matching network with the external RF Switch, so the TX matching network is practically completely isolated from the RX port. Hence, the RX (off) port impedance value does not impact the TX simulation, unlike in the Direct Tie matching network configuration (see Section 4. RF Matching Design Step II. – with Internal RF Switch (TX-RX Direct Tie Connection) later).

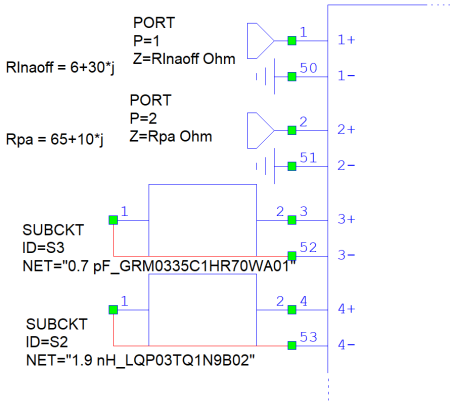

Figure 3.8. Section of the CST Touchstone File in AWR, with the TX (on) and RF (off) Port Impedances and Component S-parameter Models

The EM solver method simulations are visualized alongside the results of the ideal and full parasitic simulations and the ideal matching network (Figure 3.9 EM Solver Method Compared to the SMD + Layout Lumped Element Parasitics, and Ideal Simulations (with Initial Simulated Values) on page 16 is the logical continuation of Figure 3.6 Impedance Transforming Effect of the SMD and PCB Layout Lumped Element Parasitics on BRD4338A (with Initial Simulated Values) on page 14):

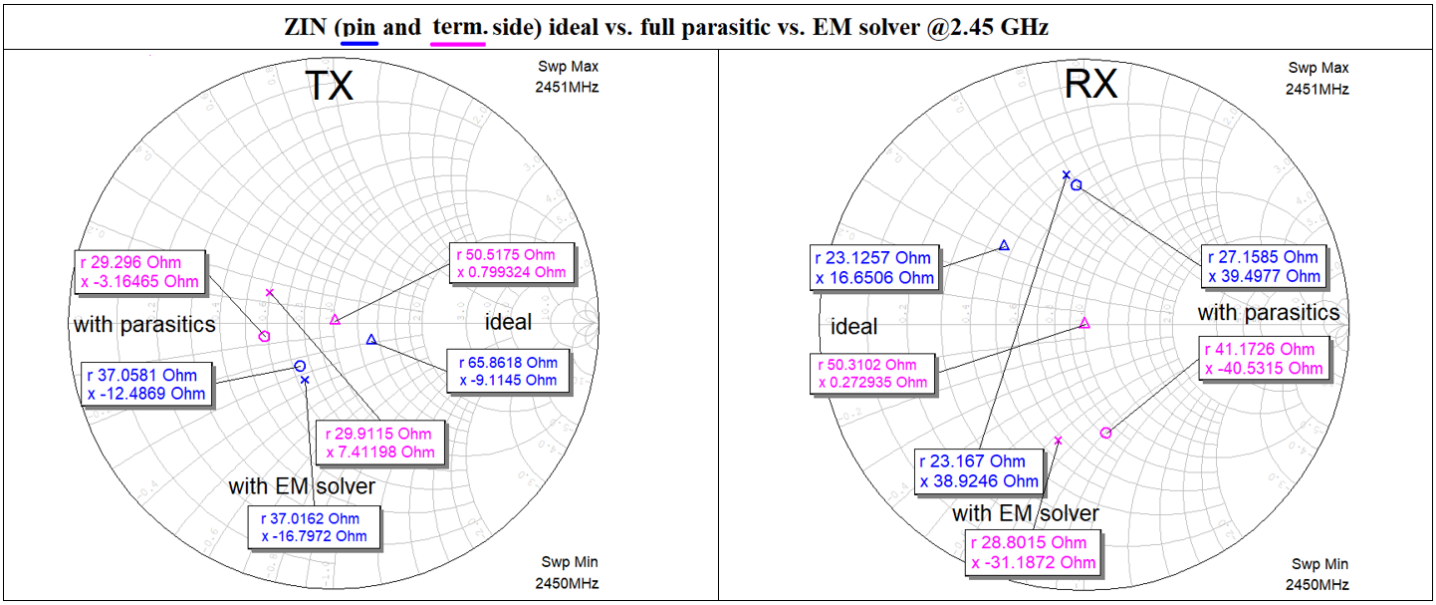

Figure 3.9. EM Solver Method Compared to the SMD + Layout Lumped Element Parasitics, and Ideal Simulations (with Initial Simulated Values)

The EM solver method simulations confirm the accuracy of the lumped PCB parasitics in Figure 3.5 Calculated PCB Layout Lumped Element Parasitics of the TX Path on Radio Board BRD4338A on page 13, and that the ideal component values are far from optimal due to the detuning effect of the PCB layout parasitics.

3.4.2.3 Analysis of the PCB Layout Parasitics using Transmission Line Theory

The significant impedance transformation effect of the PCB layout parasitics shown above can be investigated using the EM solver method, or for an even more reliable result, with VNA impedance measurements.

The interconnection PCB traces transform impedance because their characteristic impedance (Z0 =~ 50 Ω) differs from their output termination impedance. This effect is negligible for a single interconnection trace but accumulates for the whole matching network and becomes relevant.

Ideally, for the trace not to transform impedance, every trace should have a characteristic impedance that is equivalent to its termination impedance as that way, the trace is practically nonexistent in terms of impedance transforming effect. However, as the discrete matching components transform the 50 Ω ANT termination step by step, rotating it on a Smith-chart up and down (until the design goal is reached), the termination impedance that certain interconnection traces see are usually complex numbers. Therefore, these relatively lossless traces (R = G = 0) with fully real Z0 = 50 Ω introduce a slight transformation that accumulate for the whole matching network and become relevant.

To obtain the RF properties of an interconnection trace with properties of:

- Z_0: characteristic impedance
- βl: electrical length of the trace that defines the impedance transformation of the transmission line when $Z_L \neq Z_0$,

the EM solver simulations or the VNA measurements can be used for a z_{IN} input impedance measurement. After that z_0 can be calculated using the following well-known equation for terminated transmission lines:

$$z_{IN} = z_0 \frac{z_L + jz_0 \tan(\beta l)}{z_0 + jz_L \tan(\beta l)}$$

Notice that with a single Z_{IN} input impedance simulation or VNA measurement with a chosen Z_L termination, both Z_0 and βl are still unknown. Consequently, a 2nd simulation or VNA measurement is necessary with a different Z_L. It is then possible to solve the equation system of two for Z_0 and $\tan(\beta l)$. A general recommendation is to choose Z_L = 50 Ω for the 1st and Z_L = 0 Ω for the 2nd measurement.

The equation system can be solved with a Python script for Z_0 and with the help of the *sympy* library. The trace properties can be maintained (either using the EM simulations or VNA measurements):

- Z_0 = 47 Ω
- βl = 20°

The results translate into a well-designed, short (but not negligible) Z_0 = 50 Ω trace.

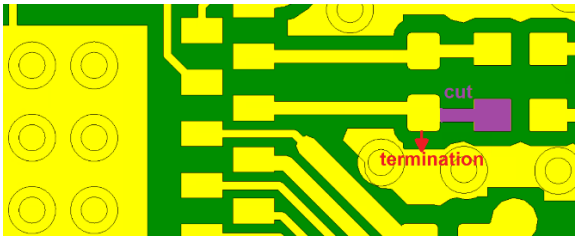

Figure 3.10. Termination Placement for Determining the Transmission Line Properties of the 1st Trace (with Simulation or Measurement)

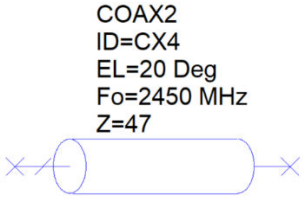

Figure 3.11. Transmission Line Model of the 1st Trace

The accuracy of the transmission line characterization can be verified by replacing the lumped element models of the 1st trace (TX pad + 1st trace + capacitor pad) with a single COAX2 element with Z_0 = 47 Ω and electrical length (EL) = 20° at 2.45 GHz. The lumped parasitic simulated input impedances of the TX and RX matching networks of Figure 3.6 Impedance Transforming Effect of the SMD and PCB Layout Lumped Element Parasitics on BRD4338A (with Initial Simulated Values) on page 14 do not change significantly, confirming a successful transmission line characterization of the 1st trace.

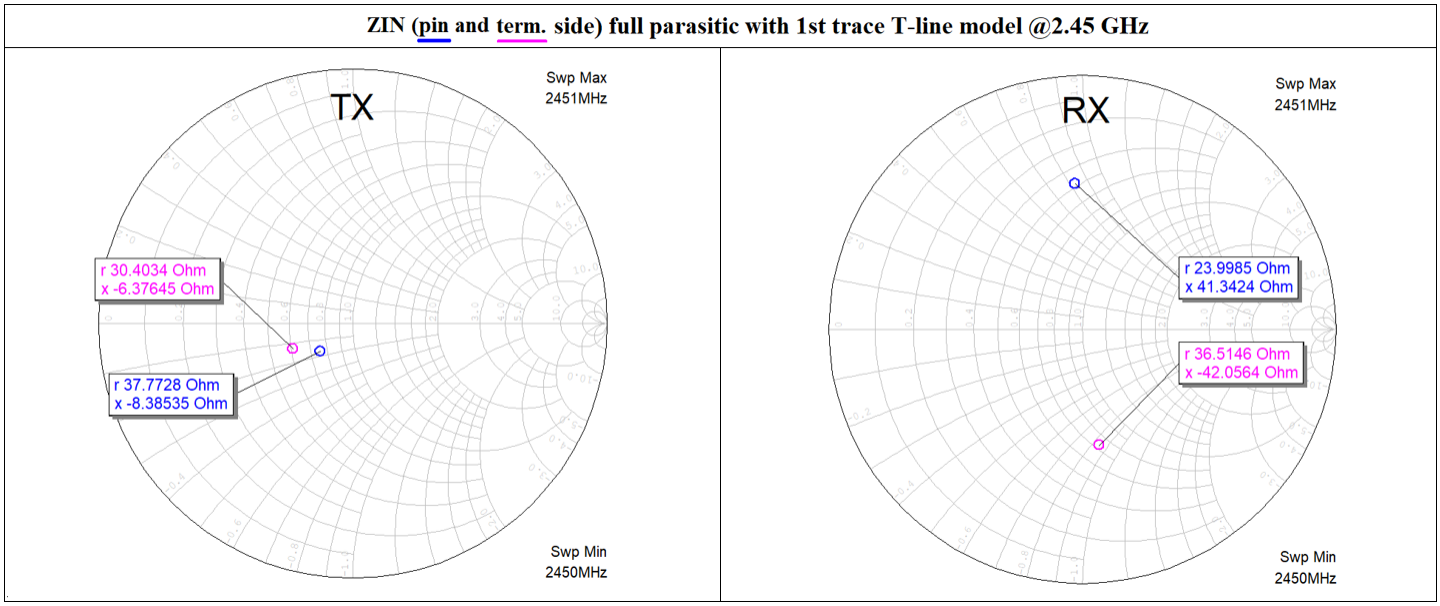

Figure 3.12. SMD and Layout Lumped Element Parasitics Simulation with 1st trace Replaced with Transmission Line Model (TX and RX Matching Networks)

This method is particularly useful if the manufactured PCB detunes the matching network unpredictably, in a way that the CPWG calculations or even the EM simulations do not predict. The interconnection traces can then be characterized by measurement, which allows the option to include them in the simulations that can emulate the measured unexpected behaviors, and the matching network can be tuned around them.

3.5 Conduct RF Bench Testing and Tuning – Effects of the RF Switch and BPF

As shown in Figure 3.9 EM Solver Method Compared to the SMD + Layout Lumped Element Parasitics, and Ideal Simulations (with Initial Simulated Values) on page 16, the simulations suggest that the PCB layout parasitics have a significant detuning effect for both the TX and RX matching networks. In this chapter, the recommended TX and RX matching networks are presented with measurements. Parallel to that, the simulations are also tested with the recommended values, confirming the simulation accuracy compared to the VNA measurements.

The recommended TX and RX matching networks are the following (from Figure 2.3 RF Schematic of the BRD4338A Radio Board (with External RF Switch) on page 5):

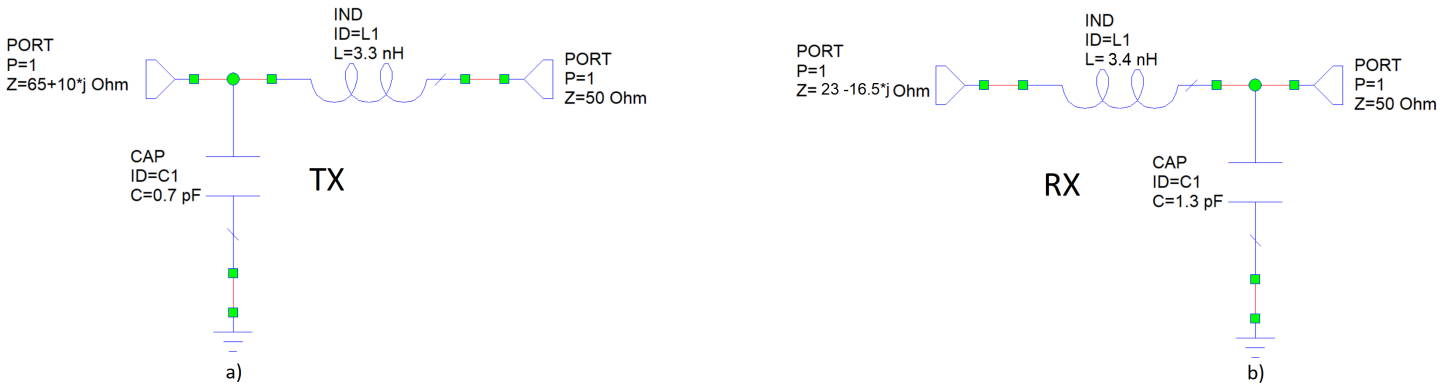

Figure 3.13. Recommended TX and RX Matching Networks (BRD4338A)

The recommended matching networks are different from the ideal simulated values suggested (especially for the TX), as expected after the analysis of the SMD and PCB lumped parasitics and EM solver simulations.

The input impedance measurements are performed by connecting a 50 Ω RF probe called “pigtail” onto the TX and RX pin pads of the IC while the IC is removed. The outer shield of the probe is firmly soldered onto the exposed GND under the IC to provide a clean RF current return path. The VNA is calibrated with its “port extension” function to the end connection point of the pigtail to eliminate the impedance transforming effect of the 50 Ω pigtail (coaxial transmission line).

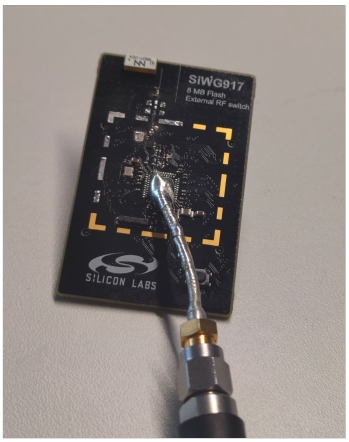

Figure 3.14. Setup of VNA Matching Network ZIN Input Impedance Measurement (TX Matching Network)

The matching network input impedance measurements in this chapter are divided into four categories:

1. Without RF Switch and BPF (RF Switch input termination)
2. With RF Switch (BPF input termination, BPF removed)
3. With RF Switch and BPF I. (BPF output termination)
4. With RF Switch and BPF II. (SWG coaxial connector termination)

The terminations for the different measurements are shown in figure below (all components that follow the terminations are removed):

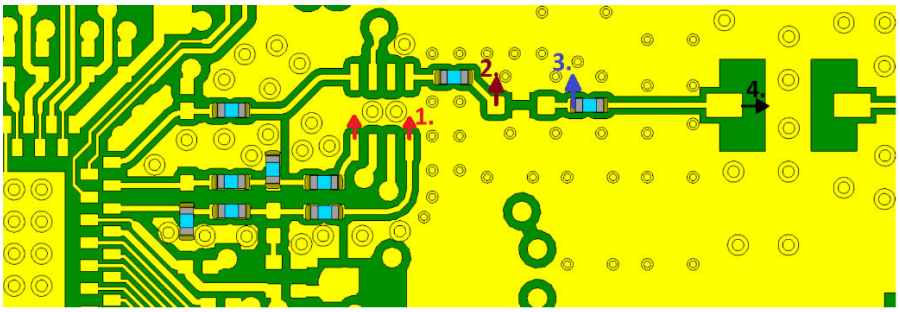

Figure 3.15. 50 Ω Terminations for the Four Different Matching Network Input Impedance Measurements

The measurements were performed within the following parameters:

- In the 2 – 3 GHz frequency domain for an accurate characterization on the fundamental frequency (2.4 – 2.5 GHz)
- Up to 13 GHz for harmonic suppression properties

S-parameter models provided by the manufacturer of the RF Switch and BPF were used in the simulations.

3.5.1 Without RF Switch and BPF (RF Switch Input Termination)

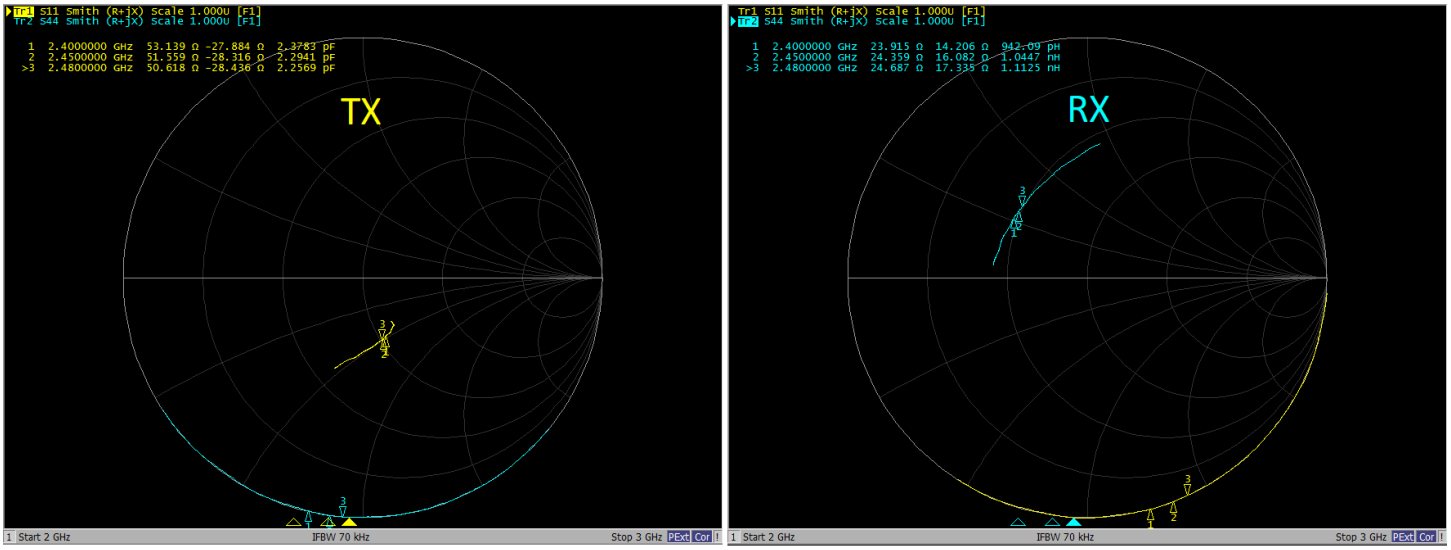

Figure 3.16. Matching Network ZIN Input Impedance Measurements without RF Switch and BPF (Recommended Matching Values)

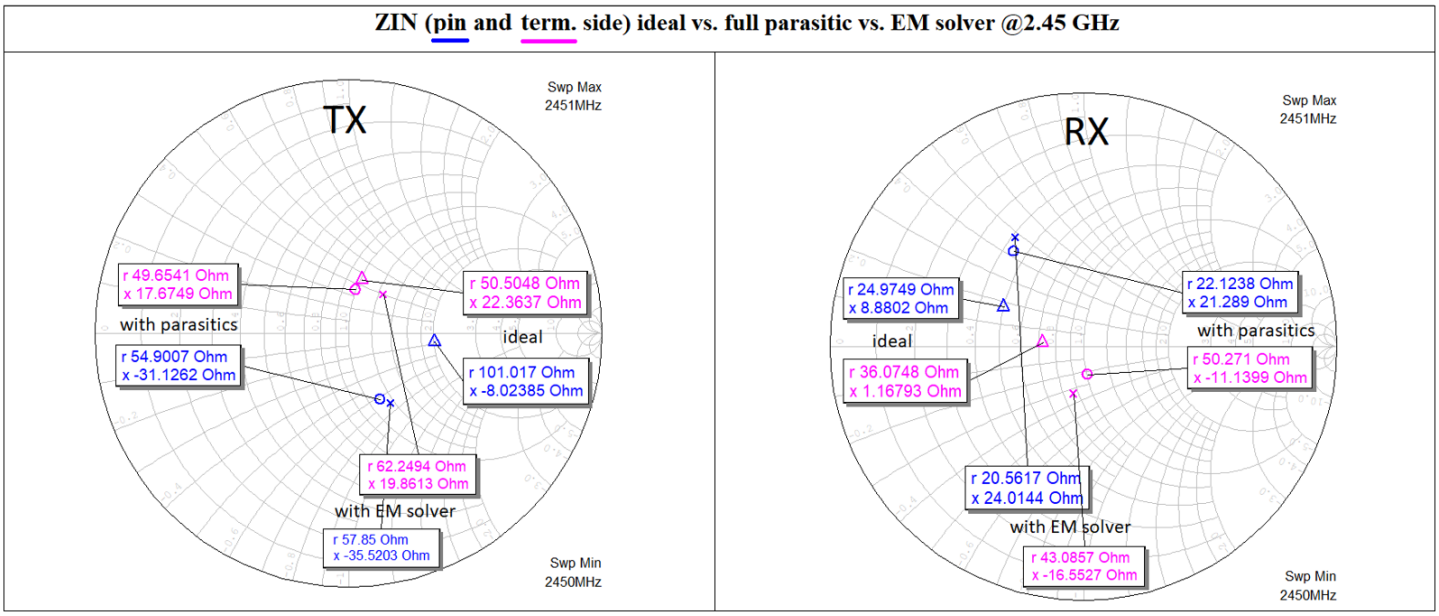

Figure 3.17. Matching Network ZIN Input Impedance Simulations without RF Switch and BPF (Recommended Matching Values)

Comparing the figures above shows that the measurements with the recommended TX and RX matching network values correlate well with simulation results. The results with ideal component simulations are also displayed which again show that the PCB parasitics have a significant effect.

Notice that the measured (and simulated) TX and RX matching network input impedances are slightly off, particularly for the TX matching network. This is because the final design is a result of optimization in terms of output power, power efficiency, and low harmonics. Moreover, the finals design must take the impedance transformation of the RF Switch and BPF into account later on in the RF path (as shown in the next subchapter).

The harmonic suppression property of the TX match is shown below:

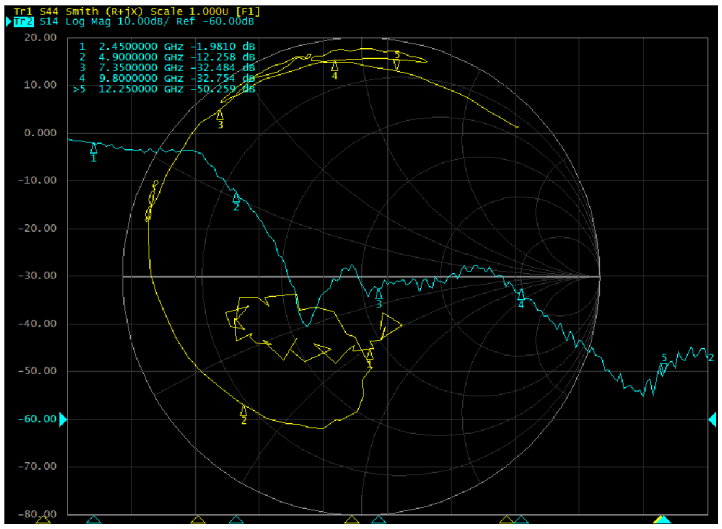

Figure 3.18. Matching Network ZIN Input Impedance (Yellow) and S21 Transfer Characteristics (Blue) Measurements up to 13 GHz

The figure above suggests that the TX matching network is designed to show low pass filter properties even without the BPF.

The simulations using the full parasitic (lumped SMD + layout) model show similar properties:

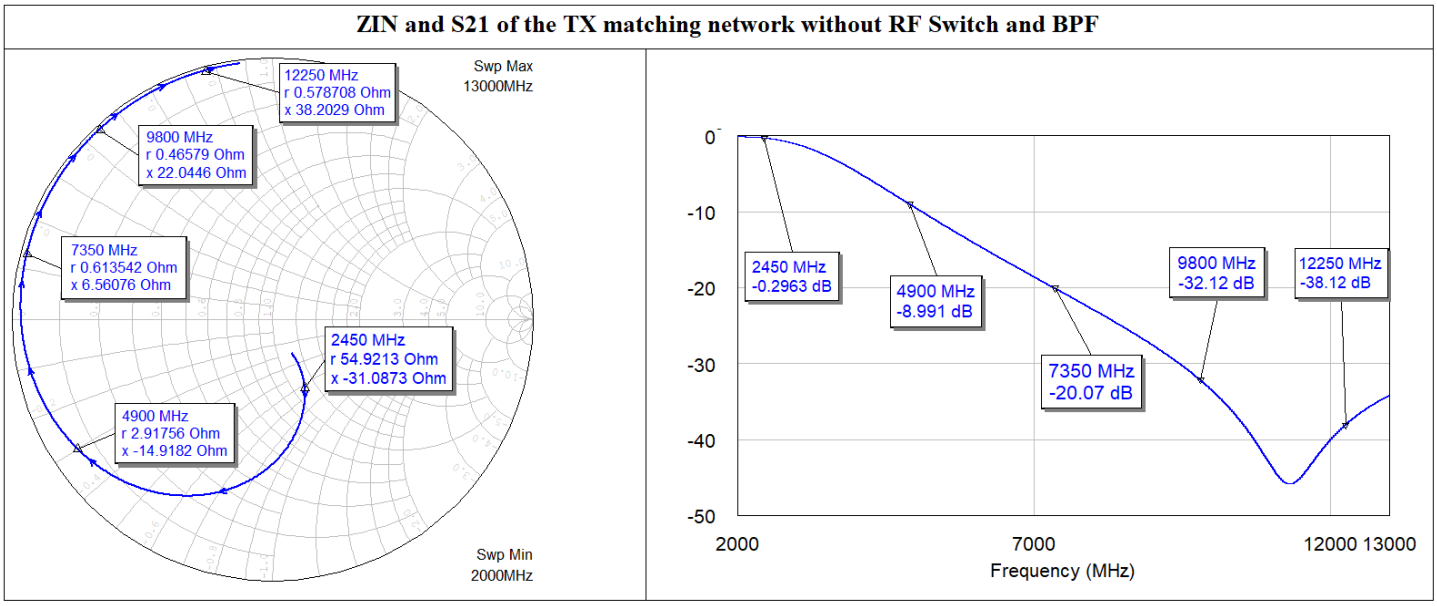

Figure 3.19. Matching Network ZIN Input Impedance and S21 Transfer Characteristics Simulations up to 13 GHz

Note: The S21 measurements required terminating the TX matching network with a 2nd port of the VNA, which introduced small "jumps" in the measurement plots. The ZIN measurements were compared to that with a wideband 50 Ω load as the termination, which showed similar curves (but straight), so the measurements are considered accurate despite the "jumps".

3.5.2 With RF Switch (BPF Input Termination, BPF Removed)

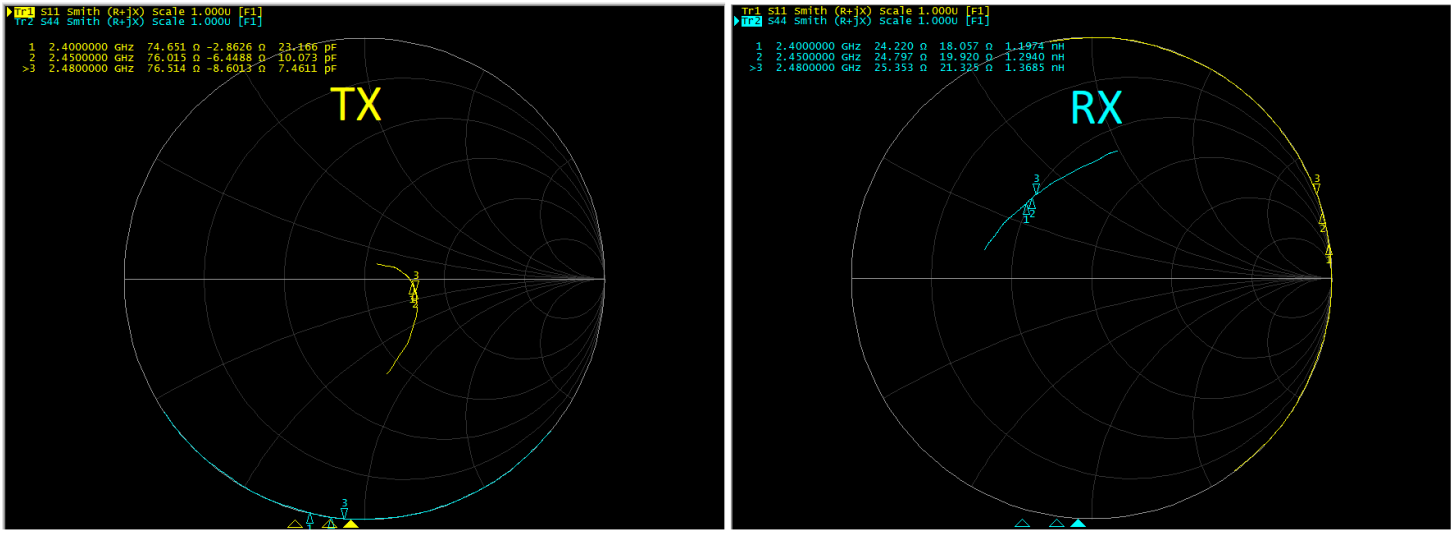

Figure 3.20. Matching Network ZIN Input Impedance Measurements with RF Switch (Recommended Matching Values)

The RF Switch transforms the impedance measurement compared to Figure 3.16 Matching Network ZIN Input Impedance Measurements without RF Switch and BPF (Recommended Matching Values) on page 21, especially for the TX path. The magnitude of the transformation is significant; however, the impedance measurement gets closer to the design goal.

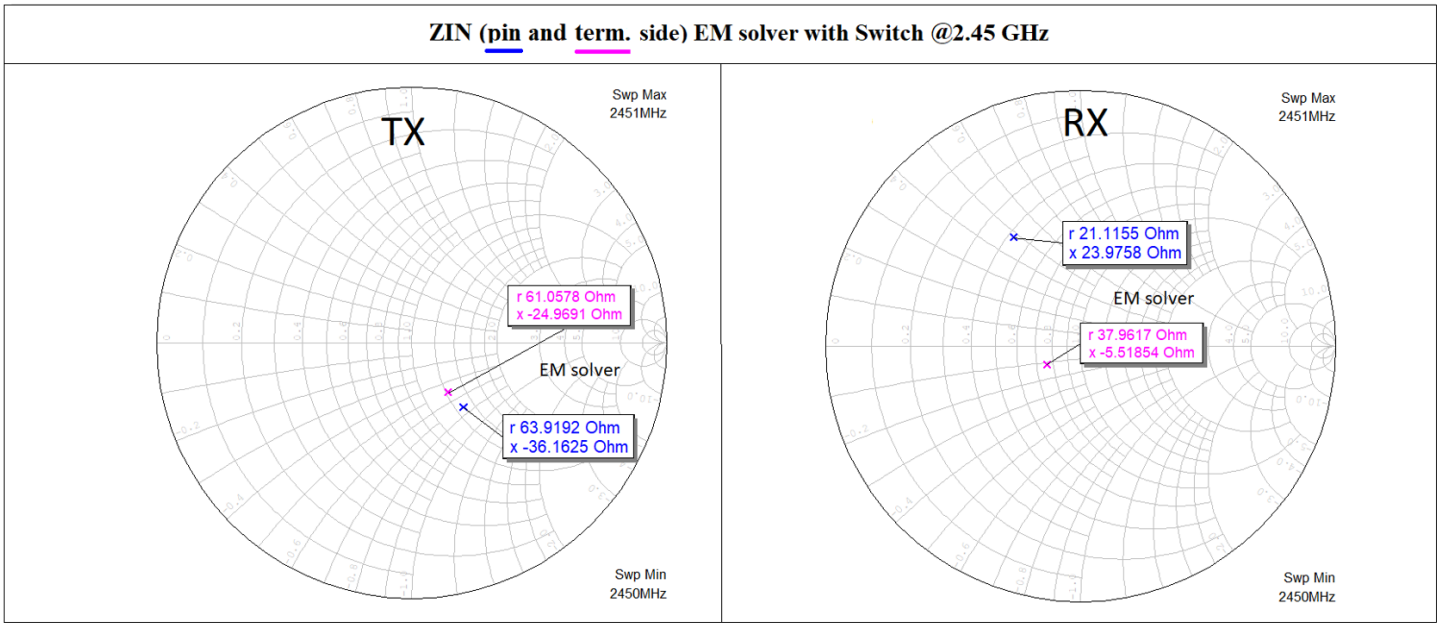

Figure 3.21. Matching Network ZIN Input Impedance Simulations with RF Switch (Recommended Matching Values)

To trace back the root cause of the RF Switch transformation in the measurements, the actual termination impedance that the RF Switch sees was investigated. A value of 46-7j Ω (instead of an ideal 50 Ω) was measured on the VNA, which is attributed to the transformations of the short traces (and 8.2 pF DC-block capacitor) between the output of the RF Switch and the 50 Ω termination resistor of the measurement. However, a similar value is seen in the EM simulations, which rules out that the deviating results are not attributed to vastly different terminations on the output of the RF Switch in the measurements vs. in the simulations.

The most plausible reason for the discrepancy is that the manufacturer's test board - that the provided S-parameter file was characterized on - was a standard 4-layer PCB with 350 µm distance between the TOP and the 1st inner layer, whereas the thickness of BRD4338A is only 1/4 of that, leading to different RF Switch characteristics than in the provided S-parameter file.

However, it is worth investigating the behavior of the RF Switch in the simulations with radically different 50 Ω terminations because we can get a closer understanding of how an RF Switch behaves in terms of impedance transformation. In the EM simulation, the output impedance of the TX matching network is 62.2 + 19.9j Ω (Figure 3.17 Matching Network ZIN Input Impedance Simulations without RF

Switch and BPF (Recommended Matching Values) on page 21 pink point) and after inserting the RF Switch and shifting the termination point to the output of the RF Switch, the impedance point changes to 61 – 25j Ω (Figure 3.21 Matching Network ZIN Input Impedance Simulations with RF Switch (Recommended Matching Values) on page 23 pink point).

The substitute figure below shows the insertion of the RF Switch into the system with the input port termination value exactly as determined by the EM simulation. The trace (and 8.2 pF DC-bloc capacitor) between the RF Switch is replaced with a COEX2 element with Z_0 = 39 Ω and electrical length (EL) = 18° at 2.45 GHz (the parameters are calculated with the method presented in Section 3.4.2.2 EM Solver Method).

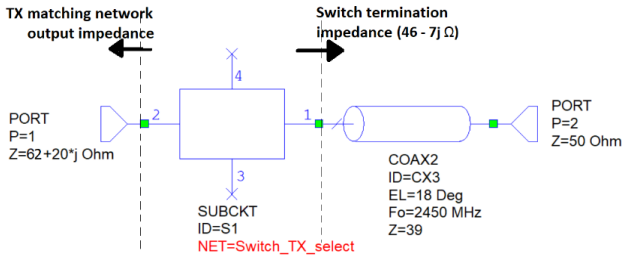

Figure 3.22. Equivalent Model of the Termination Impedances from the Perspective of the RF Switch with T-line Model of the Trace between the RF Switch and the BPF (TX Mode)

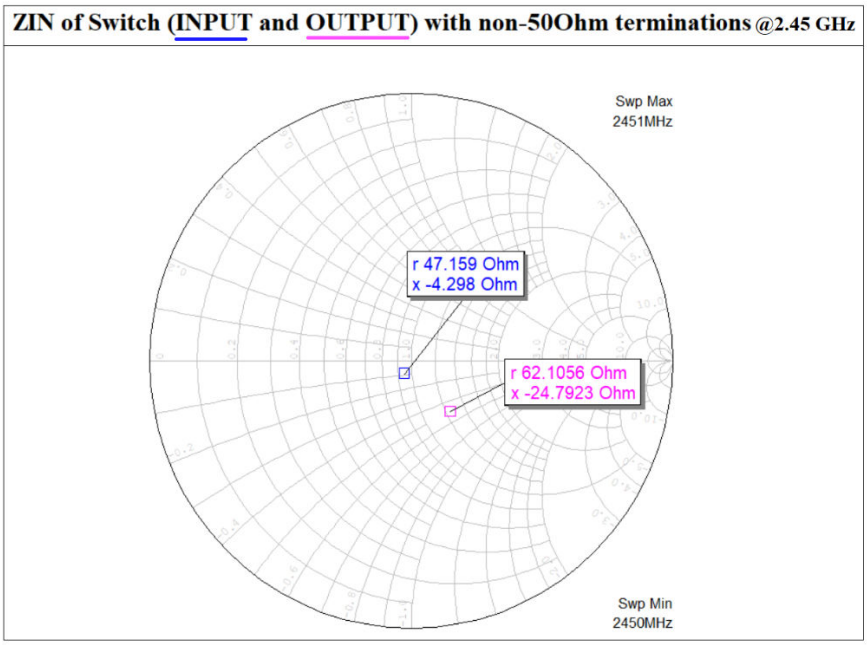

Figure 3.23. ZIN of RF Switch Ports (TX Mode)

Comparing the output impedance points of the figure above to that of Figure 3.17 Matching Network ZIN Input Impedance Simulations without RF Switch and BPF (Recommended Matching Values) on page 21 (TX mode), the model above is proven to be accurate. This suggests that to minimize unwanted impedance transformations, it is especially important that the RF Switch is placed into a 50 Ω environment. Otherwise, Switch and the traces transform impedance (see pink point).

The RF Switch in the measurements can also be characterized by comparing Figure 3.16 Matching Network ZIN Input Impedance Measurements without RF Switch and BPF (Recommended Matching Values) on page 21 to Figure 3.20 Matching Network ZIN Input Impedance Measurements with RF Switch (Recommended Matching Values) on page 23 and applying the same logic as above.

The investigations above lead to the following observation confirmed by trial-and-error simulations:

- The RF Switch S-parameter file acts as a COAX2 element with Z_0 = 55 Ω and electrical length (EL) = 20° at 2.45 GHz.
- The RF Switch in the measurements acts as a COAX2 element with Z_0 = 120 Ω and electrical length (EL) = 172° at 2.45 GHz. For the RX path, as the RF Switch in the measurements does not introduce significant transformation, so the RF Switch can be considered as described by its S-parameter model.

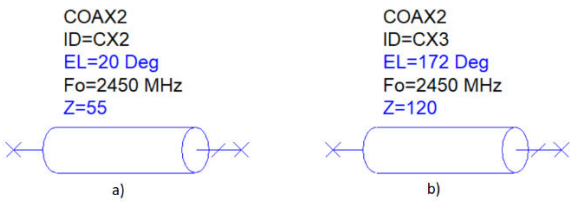

Figure 3.24. Transmission Line Model of the Switch in the a) Simulation with S-parameter File b) Measurements (TX Path Only)

Notes:

1. Despite the detailed analysis of the RF Switch behavior in the simulations, it is important that the final input impedance design goal is obtained with consideration of the complete RF front-end (with RF Switch and BPF) via the bench tuning measurements.
2. The fact that the RF Switch in the measurement introduces different transformations on the TX and RX paths shows that trial-and-error measurements at the end stage of the matching network design are always necessary.

3.5.3 With RF Switch and BPF (BPF Output Termination)

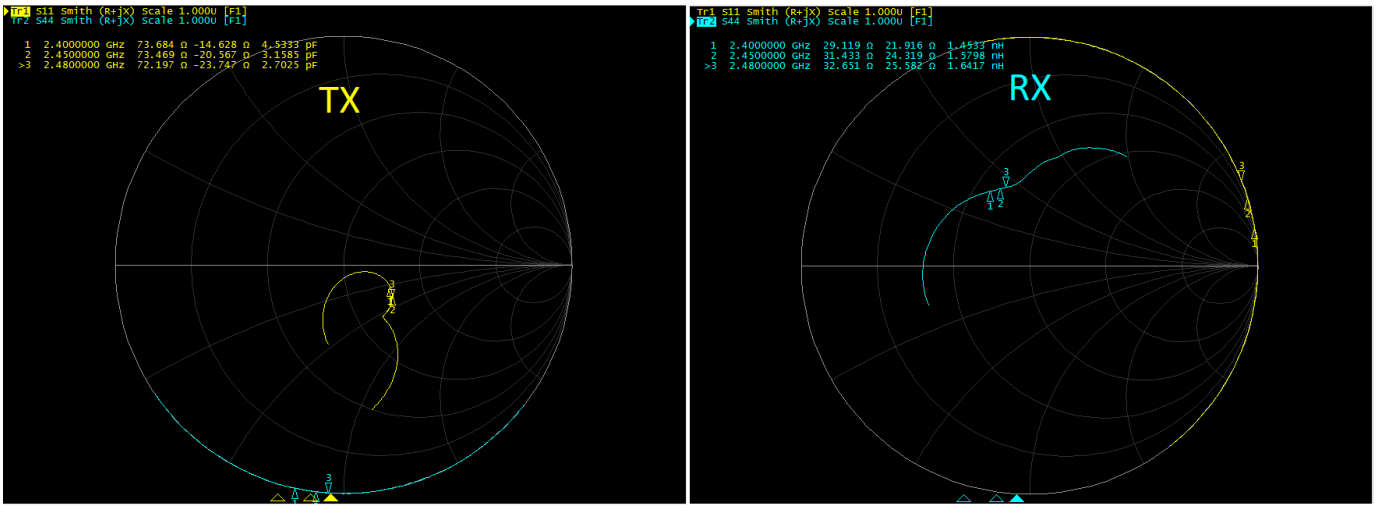

Figure 3.25. Matching Network ZIN Input Impedance Measurements with RF Switch and BPF with Termination on the Output of the BPF (Recommended Matching Values)

The BPF transforms the impedance measurement compared to Figure 3.20 Matching Network ZIN Input Impedance Measurements with RF Switch (Recommended Matching Values) on page 23. Here, an effect on the RX path is also noticeable.

After a similar analysis to that of RF Switch in 3.5.2 With RF Switch (BPF Input Termination, BPF Removed), the BPF can be characterized by trial-and-error simulations:

- The BPF S-parameter file acts as a COAX2 element with Z_0 = 55 Ω and electrical length (EL) = 72° at 2.45 GHz.
- The BPF in the measurements acts as a COAX2 element with Z_0 = 46 Ω and electrical length (EL) = 100° at 2.45 GHz. This transformation effect applies for both to the TX and RX matching networks.

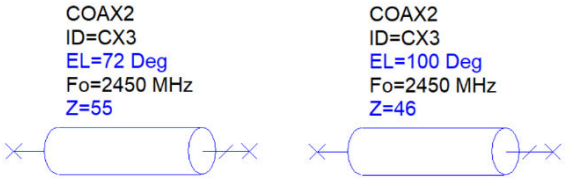

Figure 3.26. Transmission Line Model of the BPF in the a) Simulation with S-parameter File b) Measurements

Note that EL = 90° would mean a “half circle” transformation on the termination of the BPF, which implies that both characterizations produce a transformation almost as large as that, but on circles with radiuses that are slightly different. Consequently, both the S-parameter and the measured BPF models are sensitive to a non-50 Ω termination impedance, rotating it significantly on the Smith-chart.

3.5.4 With RF Switch and BPF Filter (SWG Coaxial Connector Termination)

As the conducted measurements with a Spectrum Analyzer are performed at the RF connector, this is the measurement that must show a matching network ZIN input impedance closest to the design goal.

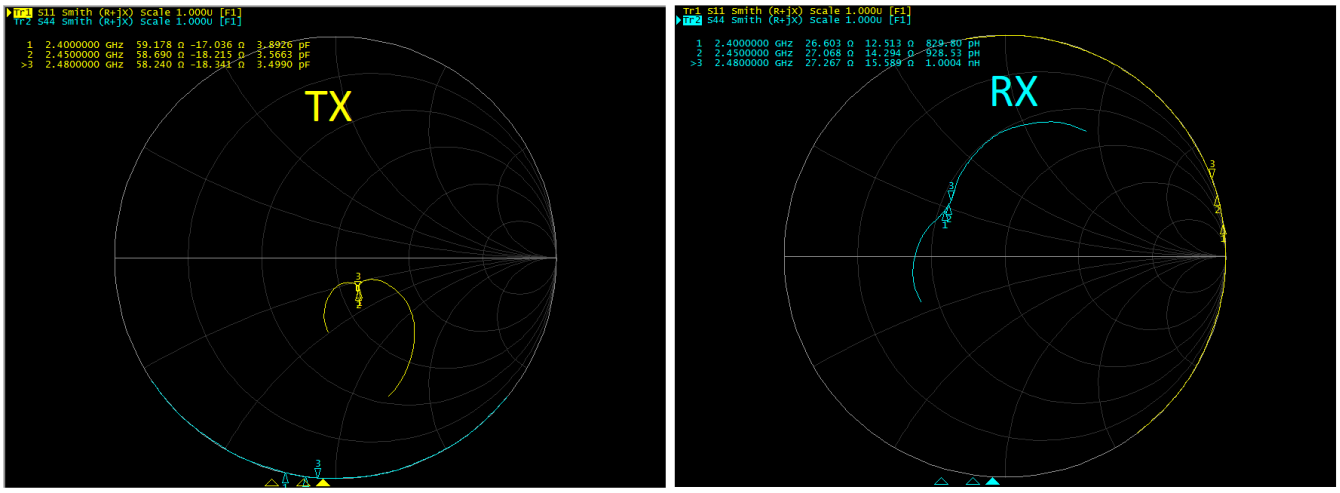

Figure 3.27. Matching Network ZIN Input Impedance Measurements with RF Switch and BPF with Termination at the Coaxial Connector (Recommended Matching Values)

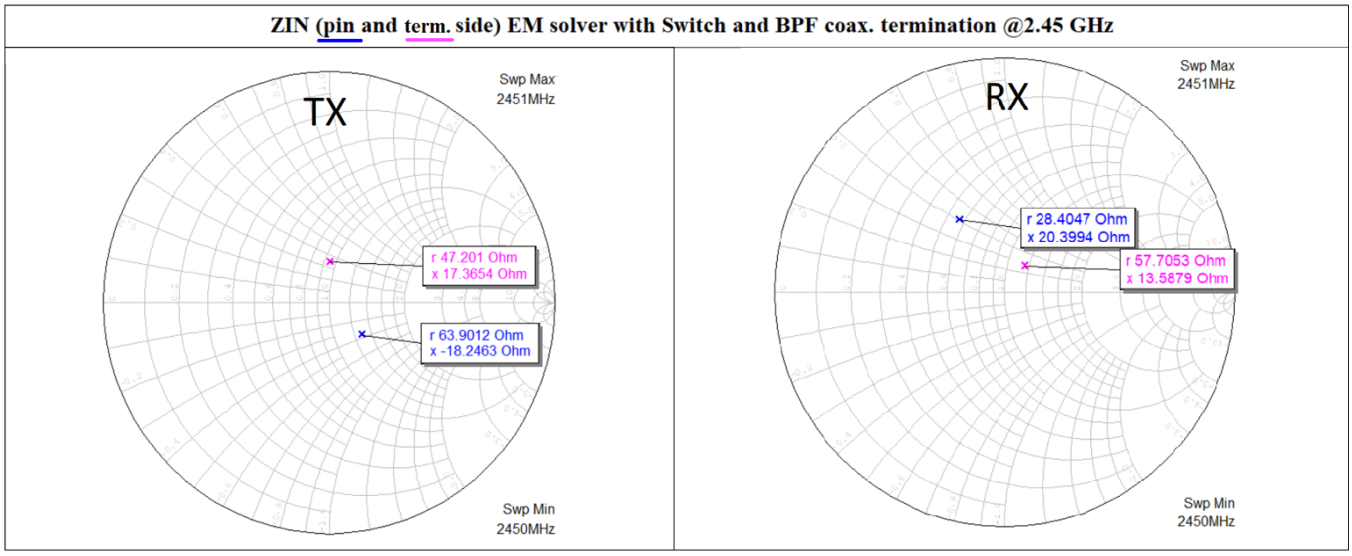

Figure 3.28. Matching Network Input ZIN Impedance Simulations with RF Switch and BPF Substitute T-line Models from the Measurements with Termination at the Coaxial Connector (Recommended Matching Values)

The simulations using the substitute transmission line models of the RF Switch and the BPF (determined from the measurements) are relatively well aligned with the measurements.

The measured and simulated harmonic filtering property of the complete TX path (with RF Switch and BPF) can be seen in the figures below:

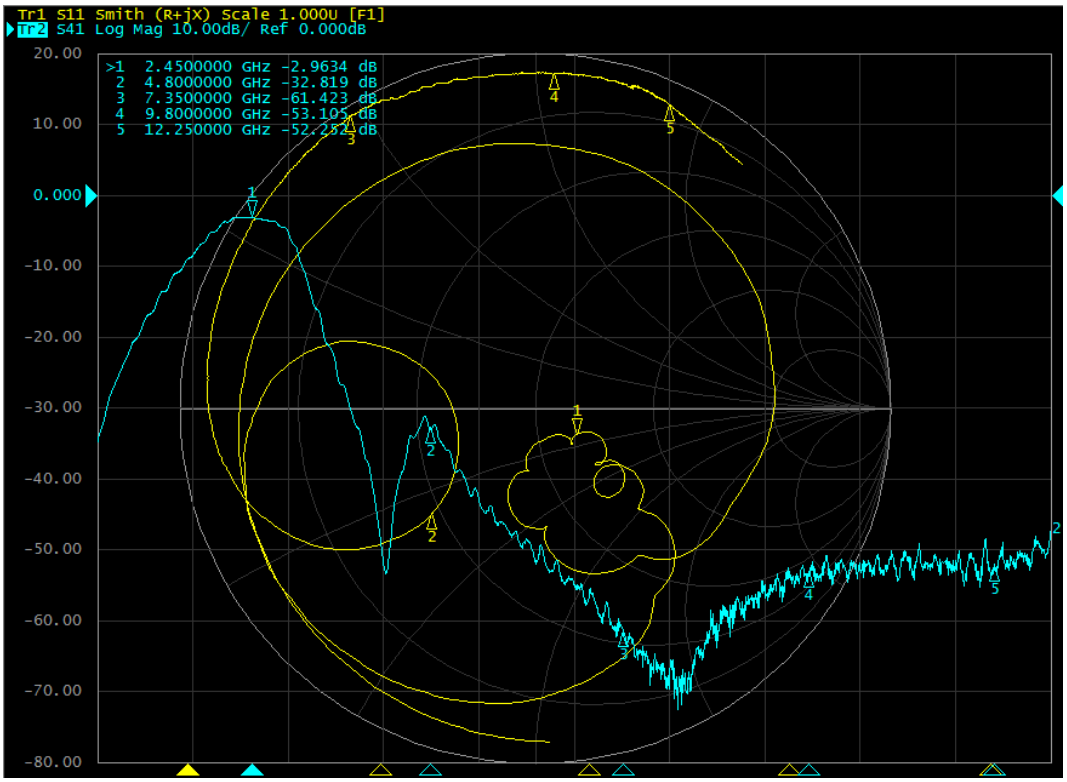

Figure 3.29. Matching Network ZIN Input Impedance and S21 Transfer Characteristics Measurements with RF Switch and BPF up to 13 GHz

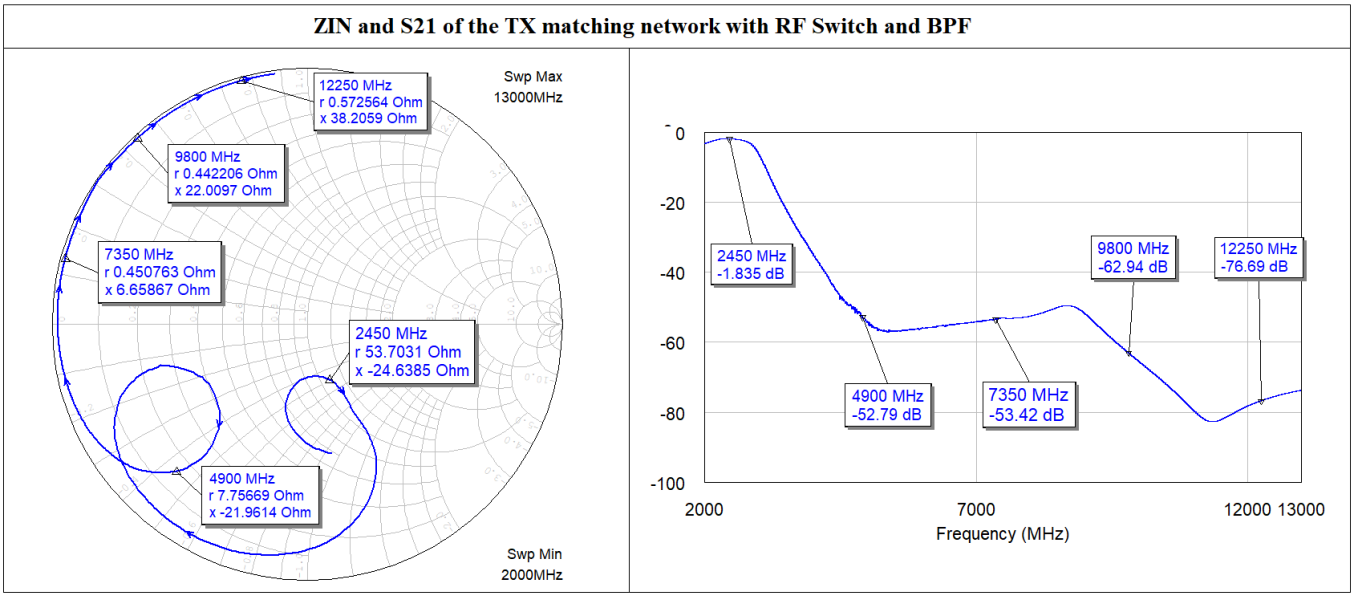

Figure 3.30. Direct Tie Matching Network ZIN Input Impedance and S21 Transfer Characteristics Simulations with BPF Up to 13 GHz

4. RF Matching Design Step II. – with Internal RF Switch (TX-RX Direct Tie Connection)

Silicon Labs reference radio boards use the so-called TX-RX direct-tie matching topology, which means the TX and RX paths are directly connected to each other to interface to a single-ended 50 Ω antenna without the need of any external RF switch in the RF path.

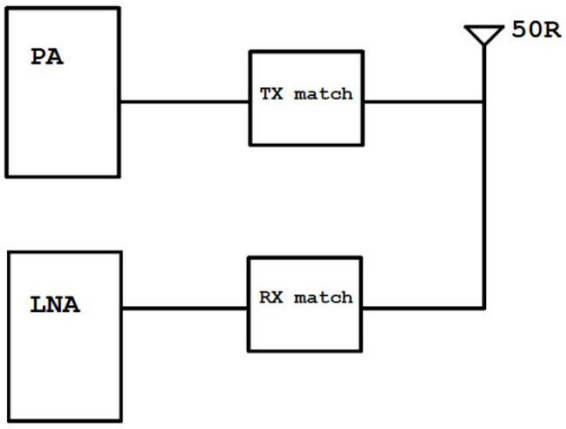

Figure 4.1. TX-RX Direct-tie Matching Network Topology

Similarly, as with the Switch matching network, the TX and RX matching networks function as an impedance transformer only (the TX low-pass filtering function is accomplished mainly by the BPF). In transmit mode, the LNA port is shorted to the GND by an internal switch (with a small series resistance) to protect the LNA, which results in a low impedance RX port. The input of the RX match (looking from the ANT side) needs to show high impedance (hence transform the low RX port impedance to higher) under these conditions to deliver the power to the antenna. Additionally, the TX match transforms the impedance between the optimal PA load impedance and 50 Ω antenna, while the input impedance of the TX match at the harmonics (typically, at least at the 3rd harmonic) should be high to enhance the harmonic suppression.

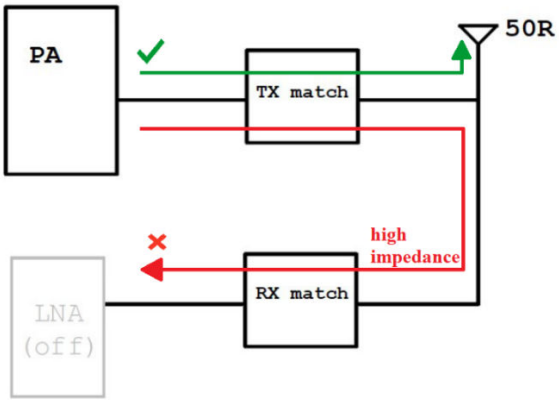

Figure 4.2. Effective Matching Circuit in TX Mode (Optimal Signal Transmission Marked)

In receive mode, the PA operates in off mode, where the PA impedance is high. Under these conditions, the output of the TX match should show high impedance to transfer the received power towards the LNA.

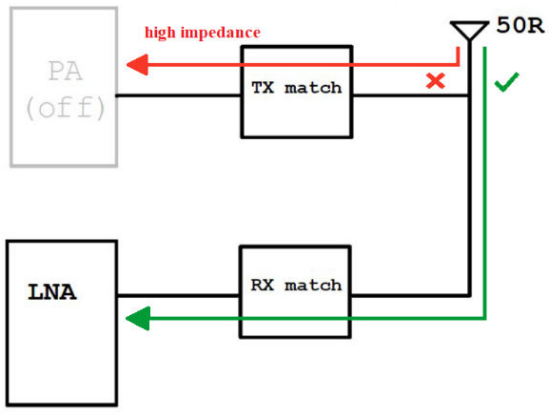

Figure 4.3. Effective Matching Circuit in RX Mode (Optimal Signal Transmission Marked)

The design goal ultimately is to see ideal transfer characteristics in both TX and RX modes between the active port and the antenna. While this goal scenario fundamentally yields high impedance looking back into the inactive port, it is also worth displaying this property (or the "isolation" between the active and inactive ports) for confirmation and a better understanding of the behavior of the Direct Tie matching network.

The measured TX (PA) and RX (LNA) on and off mode port impedances are the following (repeat of Table 3.1 Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz on page 8):

Table 4.1. Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz

Operation mode \ Pin	RF_TX	RF_RX
TX	65 + 10j Ω	6 + 30j Ω
RX	200 + 220j Ω	23.5 – 16.5j Ω

Analyzing the port impedances above demonstrates that there will be a tradeoff between TX and RX performance in the Direct Tie matching network configuration. This effect manifests in a lower than ideal impedance looking backwards from the antenna port to the disabled port. This is because:

- For matching at 2.45 GHz, the series inductors are usually relatively small in value (compared to, for example, the 868 MHz sub-GHz Direct Tie matching network of the EFR32FG23). This introduces a slightly lower than ideal series impedance to the matching network to begin with.
- By adding one shunt capacitor to the series inductor (either in LC or CL structure), the impedance looking back at the matching network decreases.

The two points above imply that:

- TX operation is good, as the RX matching network is a single inductor. Therefore, TX performance is comparable to what it would be if the RX path were completely detached from the Direct Tie point (~high impedance).
- RX operation is compromised, as the TX matching network is a CL structure. Therefore, the TX path is a shunt load at an RX mode, which has an impedance detuning effect. Even if the RX match is optimized by taking this shunt load into account (hence matched to the design goal value), the shunt off-mode TX path will "steal" some of the received signal from the antenna. This occurrence is an inherent drawback of every Direct Tie matching network, however, the RF performance degradation is usually negligible.

The simplified (no lumped PCB and SMD parasitics) simulation setup for the TX and RX simulations is shown below:

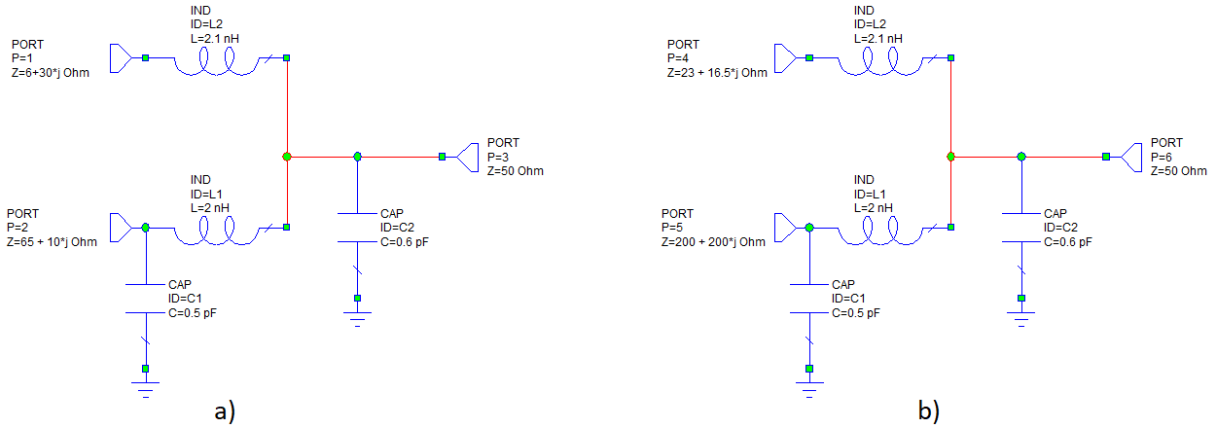

Figure 4.4. Direct Tie Matching Network Simulation Schematic in a) TX b) RX Mode (Ideal Components)

The figure below shows the TX and RX input impedance measurements with a termination at the Direct Tie connection. To emulate the off-mode impedance of the inactive port, the inactive port is terminated with a series RL component that shows the off-mode impedances seen in Table 4.1 Measured Output Impedances of the RF_TX and RF_RX Ports during Operation @2.45 GHz on page 29.

- In the TX measurement, the RX port termination is R = 6 Ω, L = 2 nH.
- In the RX measurement, the TX port termination is R = 6 Ω, L = 15 nH.

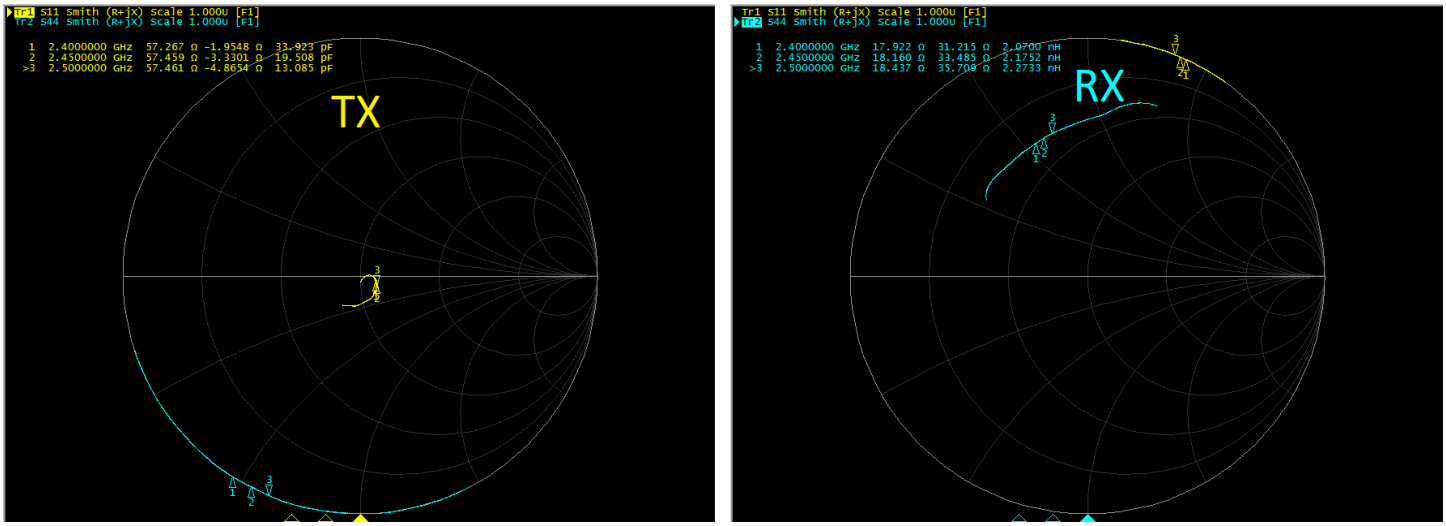

Figure 4.5. Direct Tie Matching Network Z_{IN} Input Impedance Measurements for the Direct Tie Matching Network without BPF (Recommended Values)

The EM solver method simulations are also visualized alongside the results of the ideal and the lumped full parasitic (SMD + layout) models. Both simulations were setup for Radio Board BRD4340B (see Section 3.4.2.2 EM Solver Method for the description of these two methods).

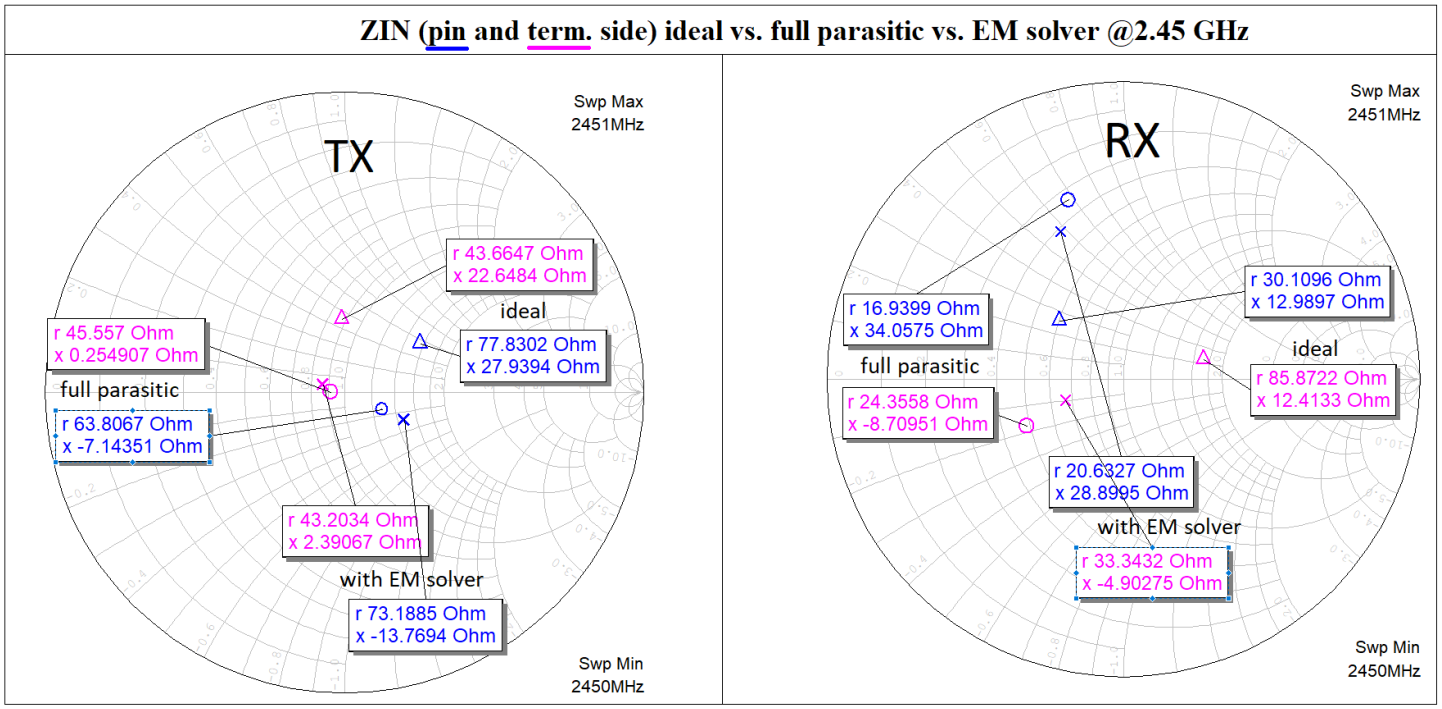

Figure 4.6. Direct Tie Matching Network Z_{IN} Input Impedance Simulations for the Direct Tie Matching Network without BPF (Recommended Values)

The results show that the SMD and layout parasitics again have a significant effect on the matching network input impedance. The TX match in the simulations comes close to the design goal with the measurements showing an impedance that is slightly smaller than that. On the other hand, the RX match in the simulation aligns well with the measurements.

The unfavorable loading effect of the inactive path in TX and RX modes can be demonstrated e.g., in the simulations by displaying the impedance looking back at the inactive path (while disconnecting the active path from the Direct Tie point) or plotting the transfer characteristics (isolation) between the active and inactive port in the unaltered matching network (Direct Tie connection):

1. **TX mode (RX off)**

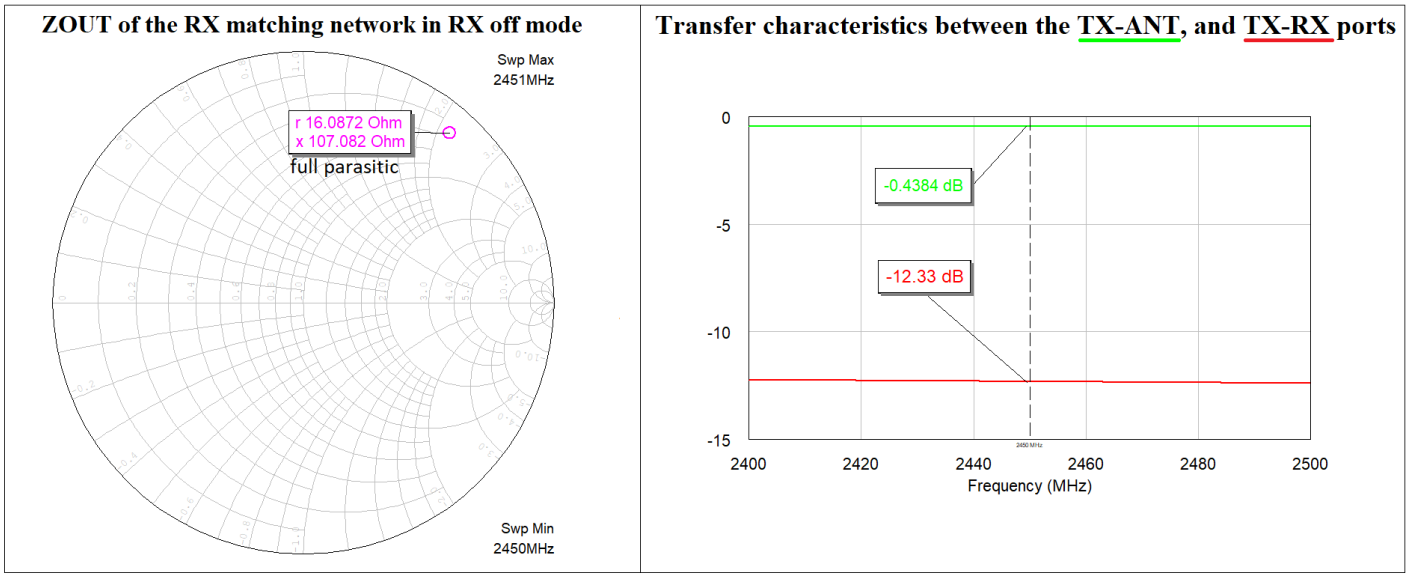

Figure 4.7. Loading Effect of the Inactive RX Path in TX Mode in Simulations

Figure 4.5 (left), Figure 4.6 (left), and Figure 4.7 show that TX matching network in the simulations and measurements satisfy all criteria of the Direct Tie design:

- Close to complex conjugate match at the active TX port and also at the antenna port.

- Relatively large impedance looking back at the inactive RX port from the antenna port (while disconnecting the active TX path from the Direct Tie point), or equivalently, adequate isolation between the active TX and inactive RX ports in the unaltered matching network.

All in all, lossless transmission is expected between the active TX port and the antenna port.

2. RX mode (TX off)

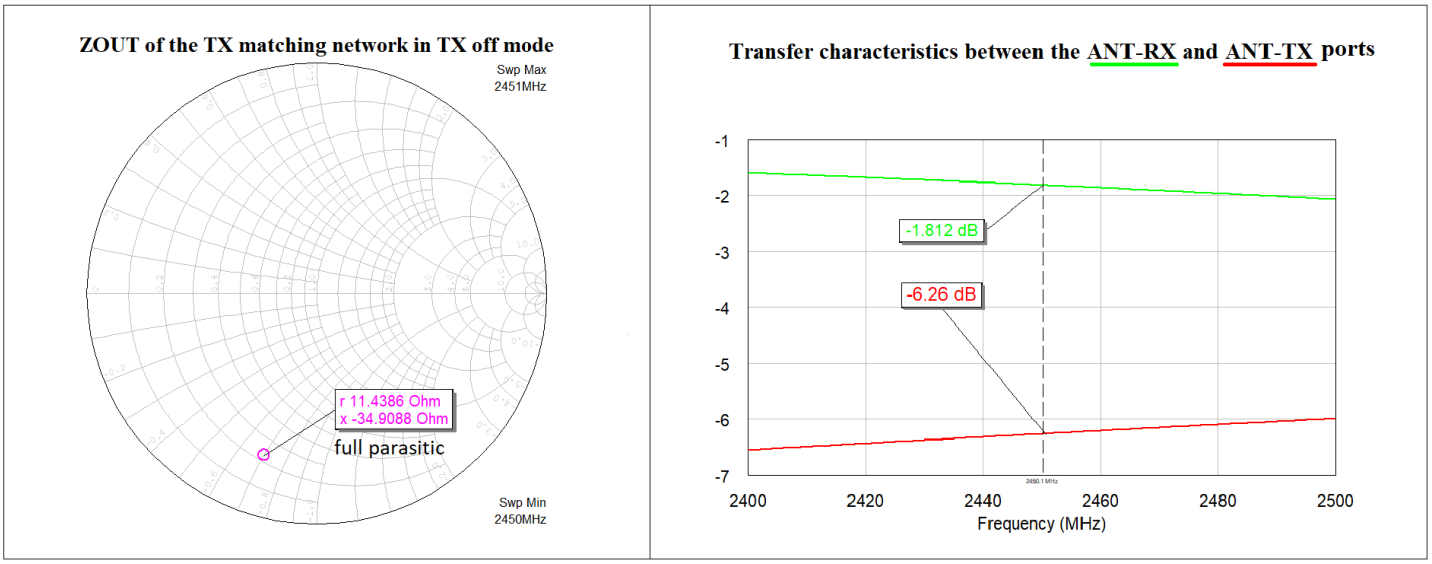

Figure 4.8. Loading Effect of the Inactive TX Path in RX Mode in Simulations

Figure 4.5 (right), Figure 4.6 (right) and Figure 4.8 show that RX matching cannot fully satisfy all criteria of the Direct Tie design:

- Not a complete complex conjugate match at the active RX port and at the antenna port.
- Not large enough impedance looking back at the inactive TX port from the antenna port (while disconnecting the active RX path from the Direct Tie point), or equivalently, lower than ideal isolation between the antenna port and inactive TX port in the unaltered matching network.

All in all, not a completely lossless transmission between the active RX port and the antenna port.

The harmonic filtering property of the TX path in the measurements and simulations can be seen in the figures below:

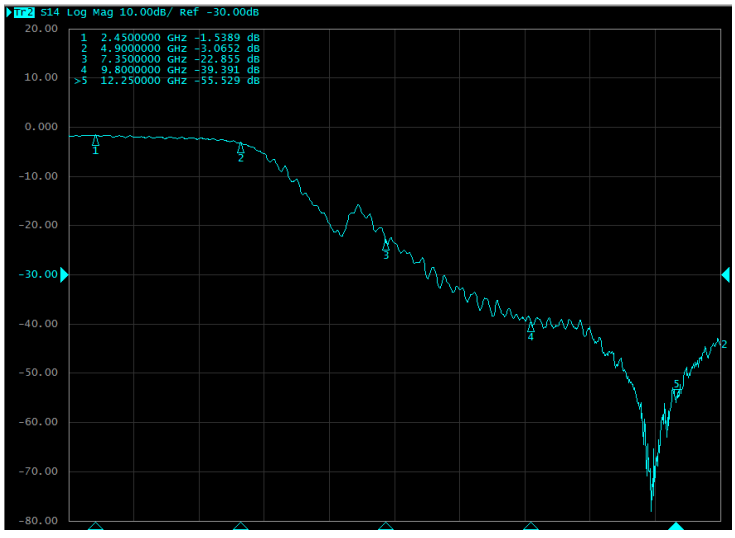

Figure 4.9. Direct Tie Matching Network S21 Transfer Characteristics Measurement without BPF up to 13 GHz

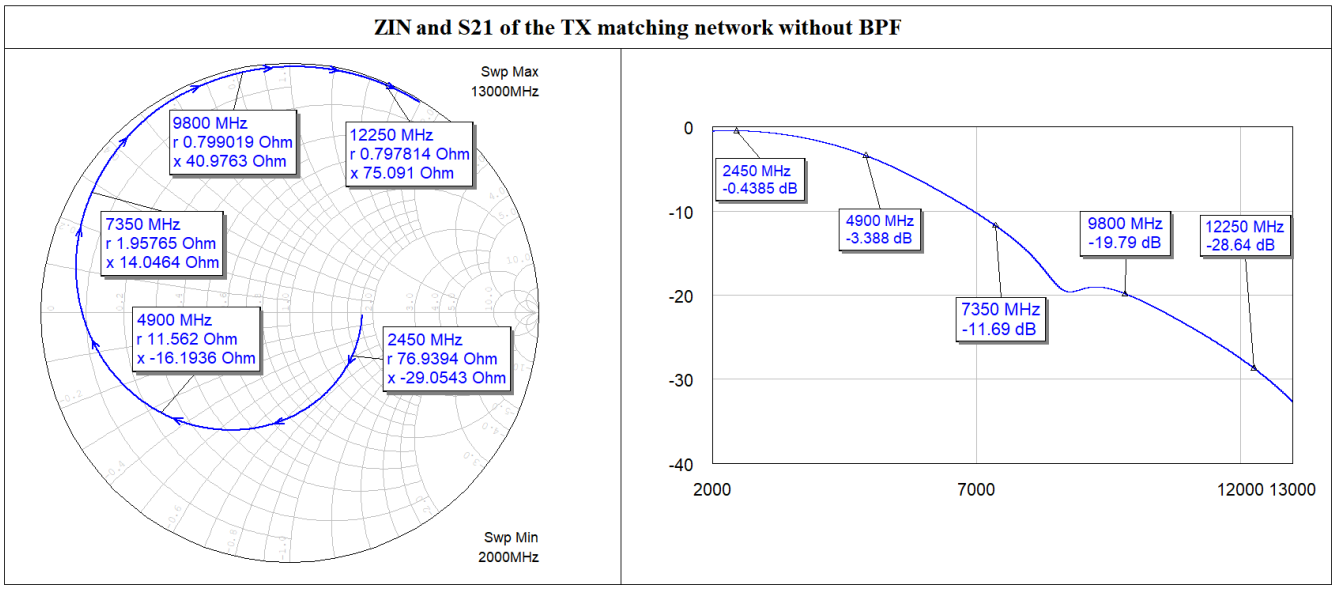

Figure 4.10. Direct Tie Matching Network ZIN Input Impedance and S21 Transfer Characteristics Simulations without BPF up to 13 GHz

As shown, the 2-element C-L TX matching network does not provide adequate harmonic suppression properties at the 2nd harmonic. Adding the BPF after the common filtering capacitor in the Direct Tie point and terminating the matching network at the swg RF coaxial connector with a 50 Ω load (similarly to termination nr.4 on Figure 3.7 Model for the EM Simulation of the SMD and PCB Layout Parasitics in CST Studio Suite on page 15), the results of Figure 4.5 modify to the following:

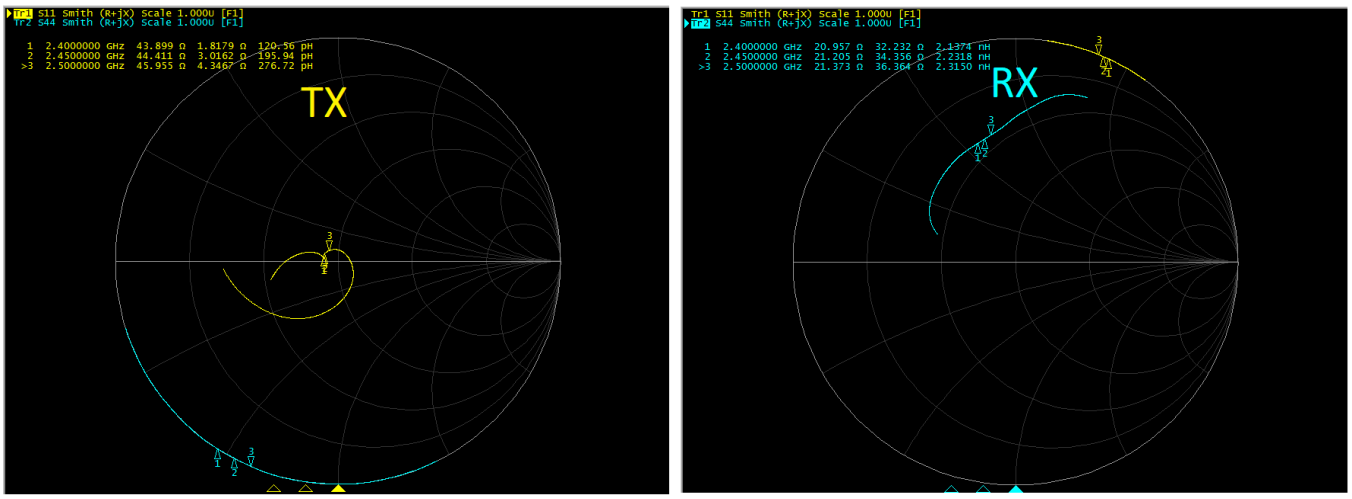

Figure 4.11. Direct Tie Matching Network ZIN Input Impedance Measurements with BPF (Recommended Values)

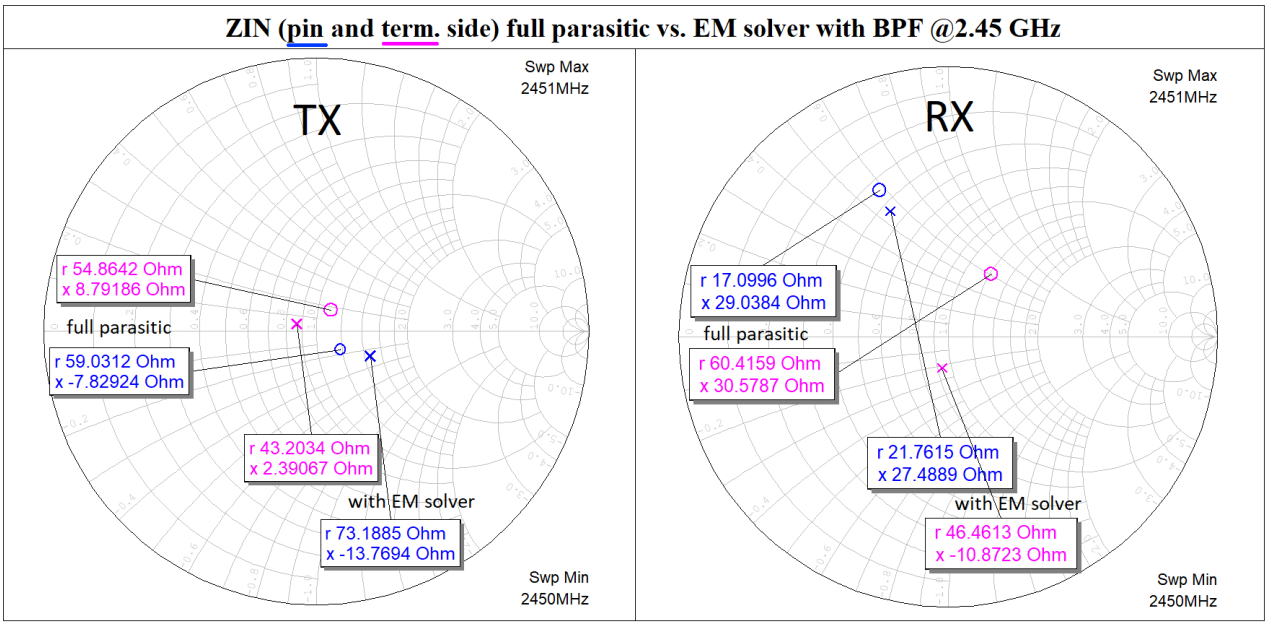

Figure 4.12. Direct Tie Matching Network ZIN Input Impedance Simulations with BPF (Recommended Values)

The results show that the TX matching network input and output side impedances are affected differently by the BPF in the measurements and simulations. The substitute transmission line models of the components can be seen in Figure 3.26 Transmission Line Model of the BPF in the a) Simulation with S-parameter File b) Measurements on page 25.

It can be shown in the EM simulations that the transmission line on the output of the BPF on the PCB layout is close to 50 Ω, which makes it clear that the BPF in the simulations have practically no impedance transforming effect, while in the measurements the BPF visibly does transform it.

Note: In the full parasitic model, the antenna termination is directly on the output of the BPF, which explains the magnitude of the impedance transformation (almost 180° due to “EL” = 72°). The reason why the EM solver method point shows a different shift around the center is because the antenna termination is not directly on the output of the BPF but at the swg RF connector. Thus, the 50 Ω transmission line between the two further rotates the point around the center, resulting in the final displayed value.

The harmonic filtering property of the TX path in the measurements and simulations is shown in the figures below:

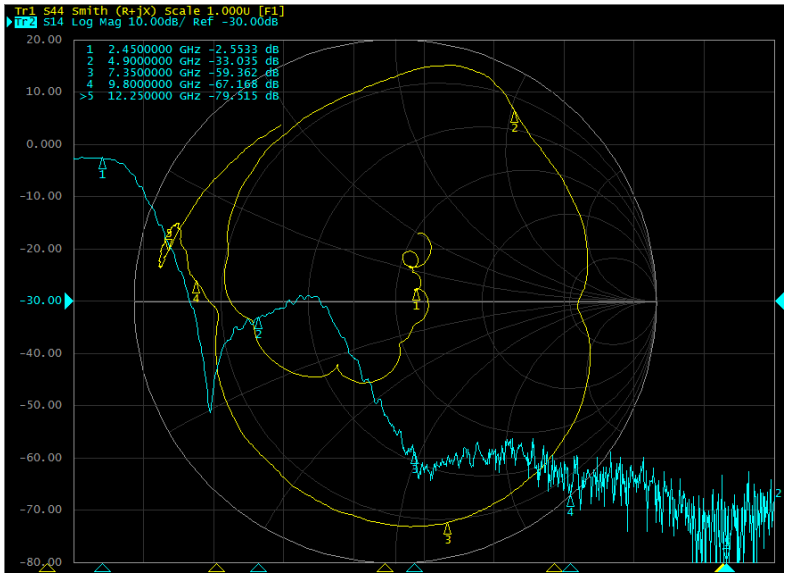

Figure 4.13. Direct Tie Matching Network ZIN Input Impedance and S21 Transfer Characteristics Measurement with BPF up to 13 GHz

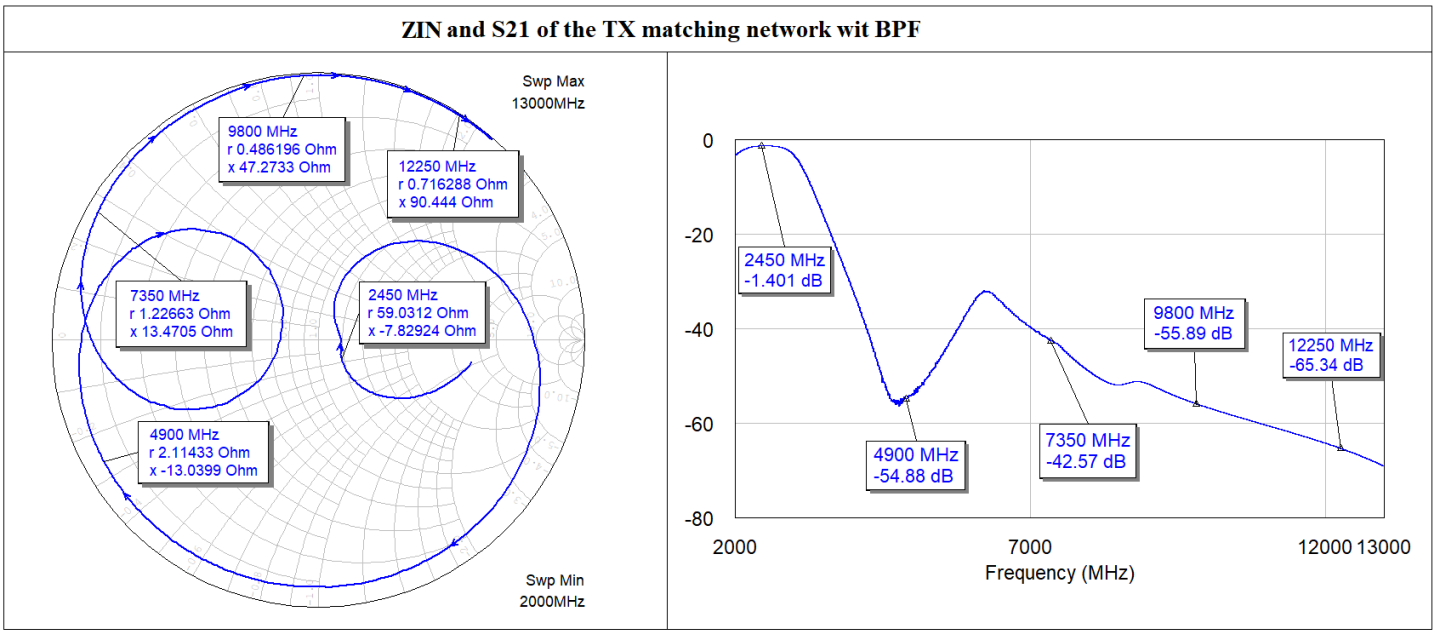

Figure 4.14. Direct Tie Matching Network ZIN Input Impedance and S21 Transfer Characteristics Simulations with BPF up to 13 GHz

5. Layout Design Guidelines

Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended that designers use the reference designs as-is since they minimize detuning effects caused by parasitics or generated by poor component placement and PCB routing. SiWx917 reference design files are available in Simplicity Studio under the Kit Documentation tab.

The compact RF part of the designs (excluding the 50 Ω single-ended antenna) is highlighted by a blue frame, and it is strongly recommended to use the same framed RF layout to avoid any possibility of detuning effects. The figure below shows the framed compact RF part of the designs.

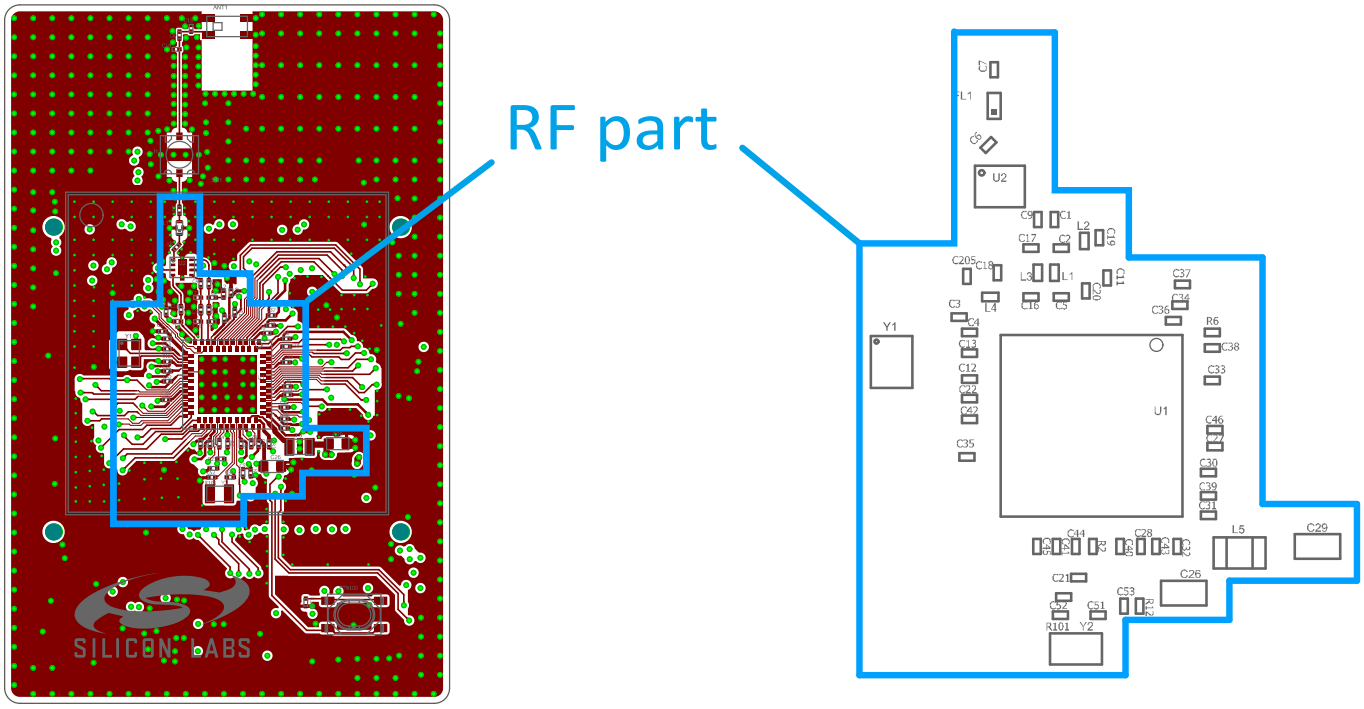

Figure 5.1. Top Layer of the BRD4338A Radio Board (Left Side) and Assembly Drawing of the RF Part (Right Side)

The layout of the MCU VDD filtering capacitors should also be copied from the reference design as much as possible. When layouts cannot be followed as shown by the reference designs (due to PCB size and shape limitations), the layout design rules described in the following sections are recommended.

5.1 General Layout Design Guidelines I.

- For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design, because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required.
- Avoid the separation of the ground plane metallization. It is recommended to create a unified ground plane on the PCB as much as possible which is not separated by traces. Also, the ground path between the matching network and the SiWx917 IC exposed pad ground should be clear and unhindered on at least one of the PCB layers. The only exceptions for ground plane separation are the matching network and HFXO areas, where the ground pins should NOT be connected to the Top layer ground. More details on these exceptions are provided in 5.2 Layout for the SiWx917 Wireless MCUs.
- Use as many grounding vias (especially near the GND pins) as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.
- Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges.
- For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers.
- Avoid using long and/or thin transmission lines to connect the RF related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.
- Use tapered line between transmission lines with different width (i.e., different impedance) to reduce internal reflections.
- Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.
- Always ensure good VDD filtering by using some bypass capacitors (especially at the range of the operating frequency). The series self-resonance of the capacitor should be close to the filtered frequency. The bypass capacitor which filters the highest frequency should be placed closest to the VDD pins of the SiWx917. In addition to the fundamental frequency, the crystal/clock frequency and its harmonics (up to the 3rd) should be filtered to avoid up-converted spurs.
- Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may be an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace.
- Place the RF-related parts (especially the antenna) far away from the dc-dc converter output and the related dc-dc components.
- Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.
- Use as short VDD traces as possible. The VDD trace can be a hidden, unwanted radiator so it is important to simplify the VDD routing as much as possible and use large, continuous GND pours with many stitching vias. To achieve the simplified VDD routing, try to avoid star topology of VDD traces (i.e., avoid connecting all VDD traces in one common point).
- Using silkscreen near the antenna could slightly affect the dielectric environment of the antenna. Although this effect is usually negligible, if possible, try to avoid using silkscreen on the antenna or on the antenna copper pour keep out areas.

5.2 Layout for the SiWx917 Wireless MCU

Examples shown in this section are based on the layout of the following designs.

- BRD4338A
- BRD4340B

The common layout design concepts are shown for both radio boards to demonstrate the basic principles. Later on, separate sections will provide additional layout design guidelines to the matching network and VDD filtering sections. The layout structures for the RF part of the previously listed designs are shown in the figures below.

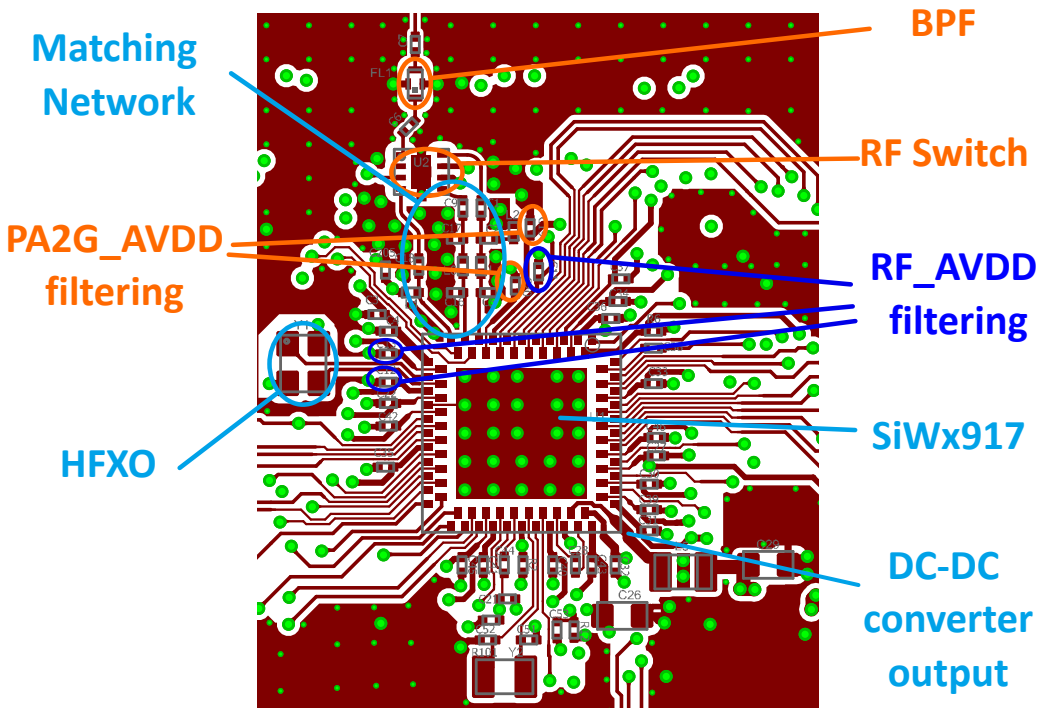

Figure 5.2. Layout of the RF Section for the BRD4338A Radio Board with RF Switch (Top Layer)

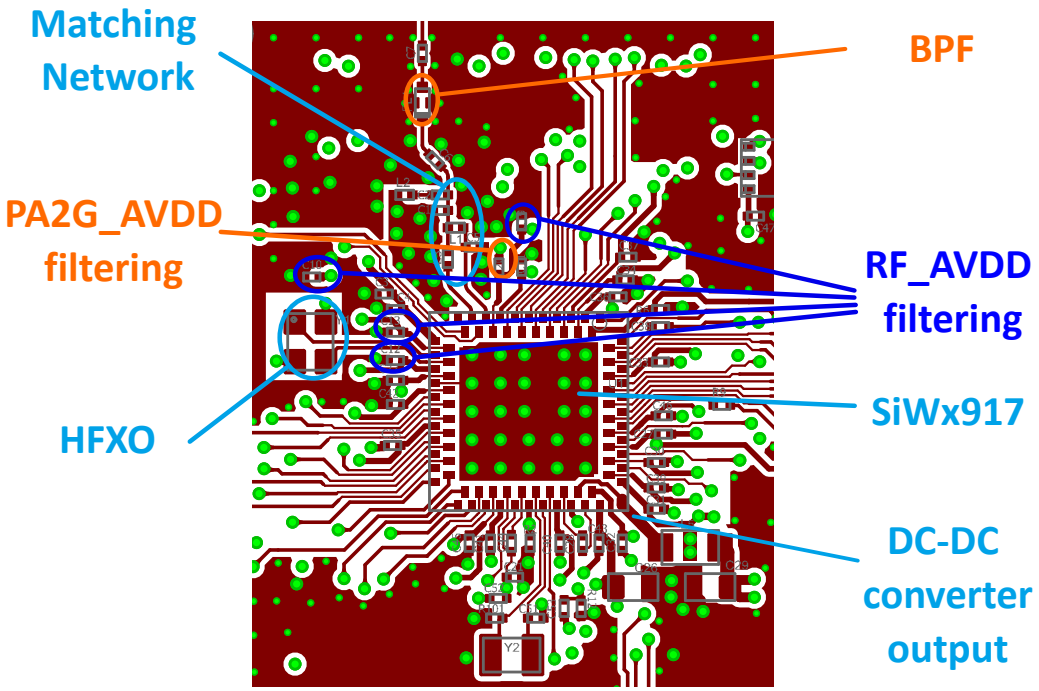

Figure 5.3. Layout of the RF Section for the BRD4340B Radio Board with Direct Tie connection (Top Layer)

5.3 General Layout Design Guidelines II.

- The lower-value VDD bypass capacitors (the ones with ~nF values) should be kept as close as possible to the VDD pin.
- To ensure good ground connection, all VDD filtering capacitors should use vias close to their ground pins. It is also recommended that the GND return path between the GND vias of the VDD filtering capacitors and the GND vias of the RFIC paddle should not be blocked in any way; return currents should have a clear and unhindered pathway through the GND plane to the back of the RFIC.
- The exposed pad footprint for the paddle of the SiWx917 should use as many vias as possible to ensure good grounding and heat sink capability. It is highly recommended to follow the thermal via pattern of the reference design.
- The RF crystal should be placed as close as possible to the XTAL_IN and XTAL_OUT pins to minimize wire parasitic capacitances and any frequency offsets.
- The ground pins of RF crystal should be connected directly to the first inner layer ground plane using ground vias. Connecting the ground pins to the common ground metal on the top layer should be avoided.
- The series matching/filtering inductors should be placed one after another or perpendicular to each other to reduce coupling between stages (the recommended matching networks have one inductor in every path however).
- Traces near the GND pins of the capacitors should be thickened to improve the grounding effect in the thermal straps. This minimizes series parasitic inductances between the ground pour and the GND pins.
- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering. Gaps should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to the restrictions of the actual radio board design. These restrictions include traces routed on other layers or components on the bottom side, which are not shown in the figure above.
- The area beneath the RF chip and the matching network (on the first inner layer) should be filled with continuous ground metal as it will show good ground reference for the matching network and will ensure a good, low impedance return path to the RF chip's ground as well. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX/RX matching network and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear, unhindered pathway through the GND plane to the back of the RFIC.

The figure below demonstrates the above listed layout design recommendations on the BRD4338A Radio Board.

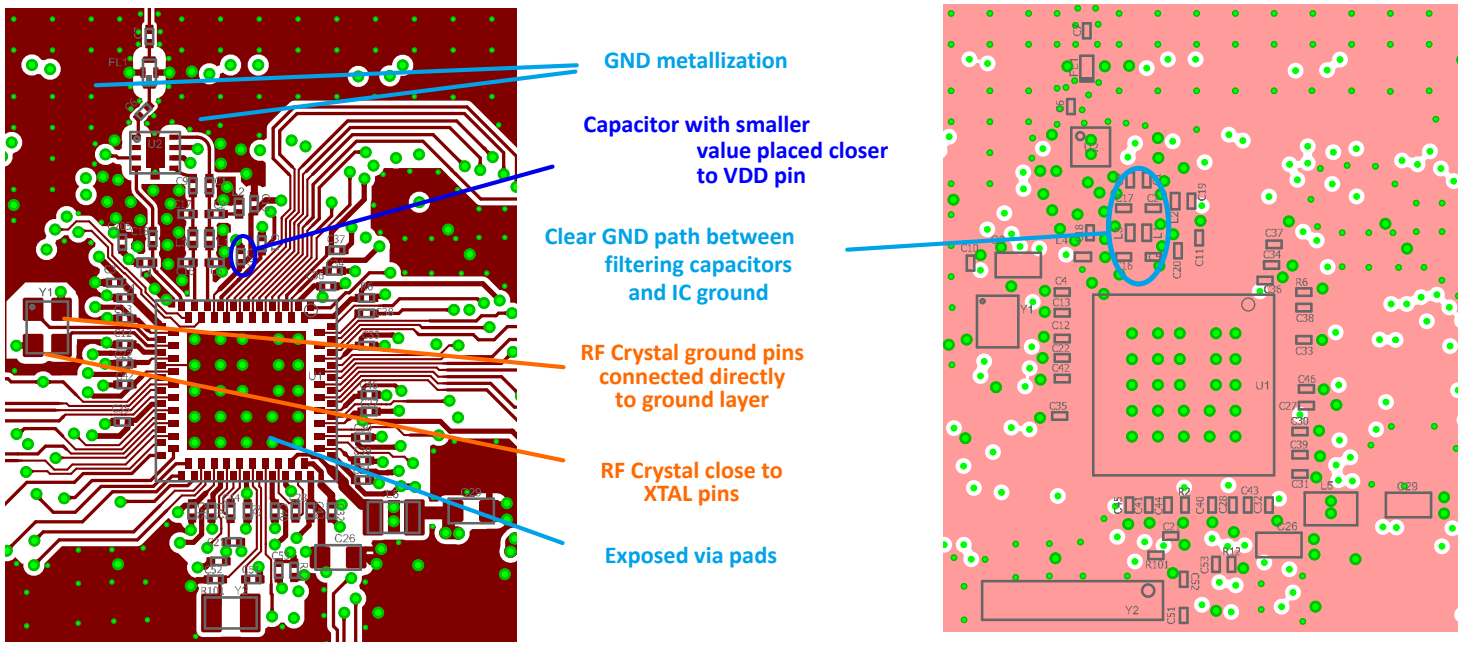

Figure 5.4. VDD Filtering, RF Crystal, and Exposed Pad Ground Layout Guidelines on BRD4338A (Top Layer, Inner Layer 1)

- Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VDD trace, to reduce their harmonic radiation caused by the fringing field.
- If the trace routing on the inner layers prevents placing plated thru hole vias, use micro-vias between the TOP and 1st inner GND layers.

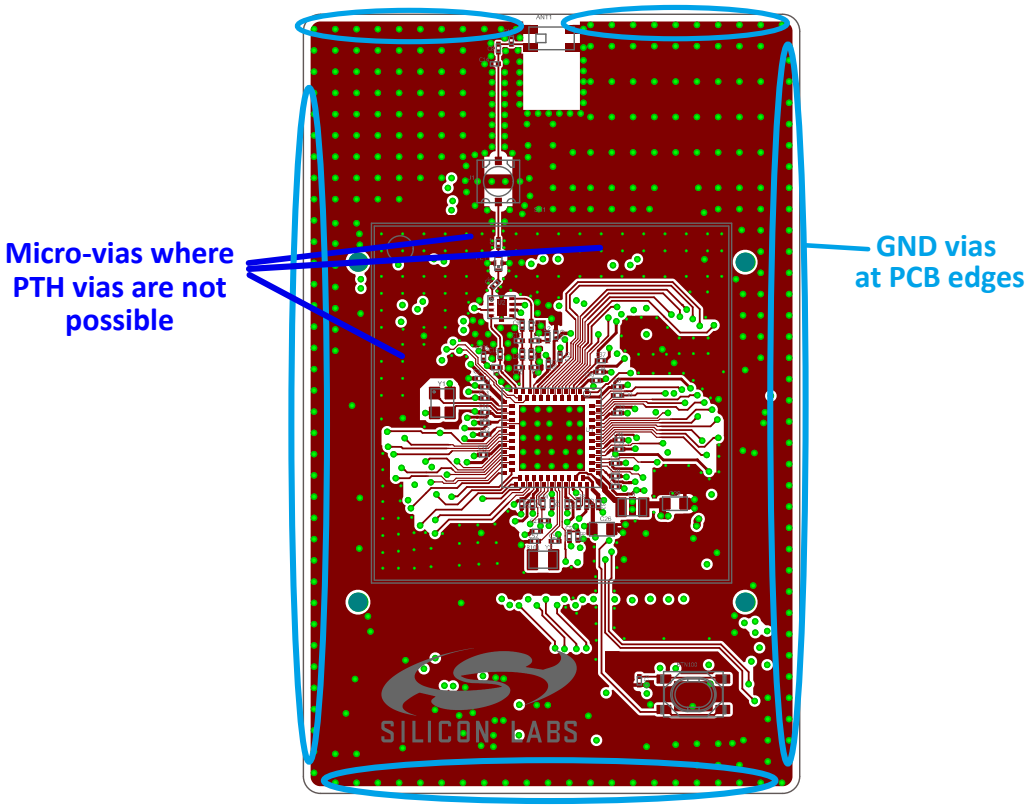

Figure 5.5. GND Vias at PCB Edges and Micro-vias where PTA Vias are not Placeable on BRD4338A Radio Board (Top Layer)

- If necessary, a shielding cap can be used to shield the harmonic radiations of the PCB; in that case, the shielding cap should cover all of the RF-related components (excluding the antenna).
- The ideal layer consistency for PCBs with more than two layers is as follows:
  - Top layer: Use as much continuous solid GND metallization as possible with many vias.
  - First inner layer: Use continuous, unified GND metallization beneath the RF part; wires can be routed beneath the non- RF parts if necessary.
  - All other inner layers: Route as many (supply and digital) traces on these layers as possible.
  - Bottom layer: This layer should be unified GND metal; route traces on this layer only if necessary.

The following figure illustrates the layer consistency on the layout of BRD4338A Radio Board.

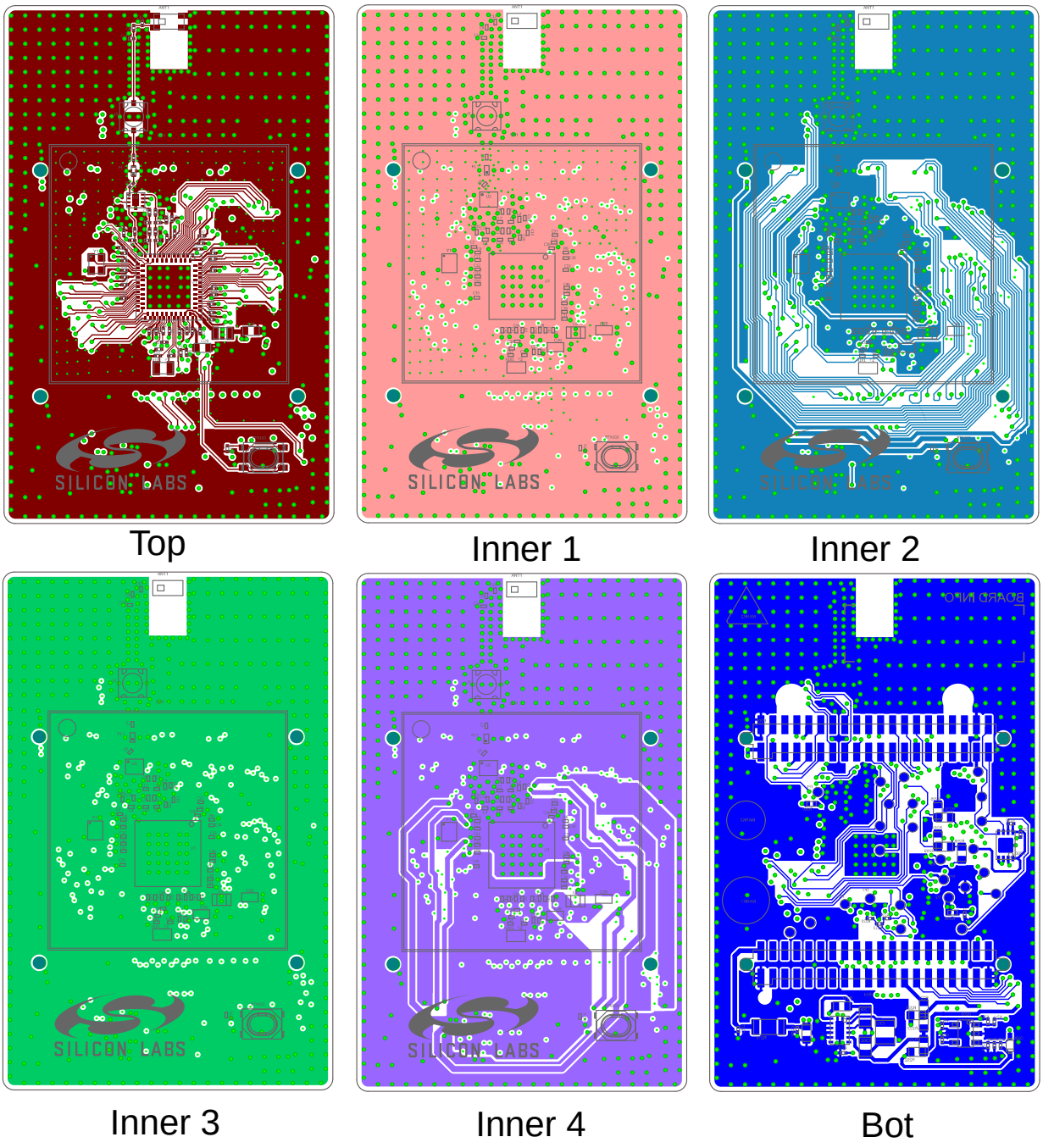

Figure 5.6. Layer Consistency on BRD4338A Radio Board

- Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.
- Avoid placing the supply lines close to the PCB edge.
- To reduce sensitivity to PCB thickness variations, use 50 Ω grounded coplanar lines where possible for connecting the antenna or the U.FL connector to the matching network. This also reduces radiation and coupling effects. A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency.
- The interconnections between elements are not considered transmission lines since their lengths are much shorter than the wavelength, and, thus, their impedances are not critical. However, we highly recommend using the same trace width as for the 50 Ω traces. This is particularly advised for the 1st trace that connects the RF pin to the 1st matching component.
- Use many vias near the coplanar lines to minimize radiation losses.

The following figure shows the BRD4338A and BRD4340B Radio Board stack-up.

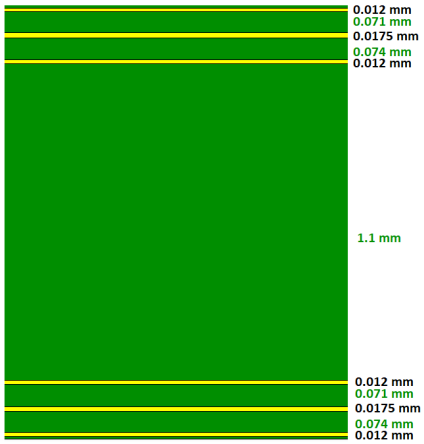

Figure 5.7. Typical 6-layer Stack-up of the Silicon Labs Radio Boards

The matching network component values are optimized for PCB stack-up configurations with a separation of 0.071 mm between the TOP and 1st inner layer.

The following table shows the trace parameters for 50 Ω characteristic impedance on the radio board stack-up:

Table 5.1. Parameters for 50 Ω Grounded Coplanar Lines

Lines	Parameters
f	2.45 GHz
T	0.012 mm
εr	4.2
H	0.071 mm
G	0.13 mm
W	0.13 mm

Note: The trace impedance is not particularly sensitive to the "G" gap value because the 1st inner GND layer is closer to the TOP layer transmission lines than the TOP layer GND pour itself on the sides (H = 0.07 mm vs G = 0.13 mm). This results in basically a microstrip rather than a coplanar line propagation mode, hence the 1st inner GND layer is acting as the main GND reference instead of the side GNDs. This means that the trace impedance can be calculated by microstrip line calculators, yielding a similar result as CPWG calculators. Note, however, that different impedance calculators may yield slightly different results.

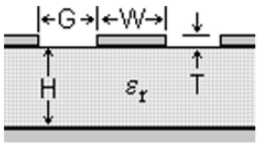

Figure 5.8. Grounded Coplanar Line (CPWG) Parameters

5.4 Matching Network Specific Layout Design Guidelines

- Keep ~1.3 mm distance between the RF pin and the 1st matching component of the matching network.
- Place the matching network components close to each other.
- Make sure that the GND pads of the matching network capacitors are connected directly to the inner GND layers without connecting it to the TOP layer GND pour (use copper cut-outs to create “GND islands” for the matching network capacitors GND pads).
- Ensure good ground connection of the RF Switch and BPF by placing vias close their GND pads.
- **Use a large copper cutout region under and around the BPF. Not doing so can cause significant degradation in the harmonic content of the signal.**

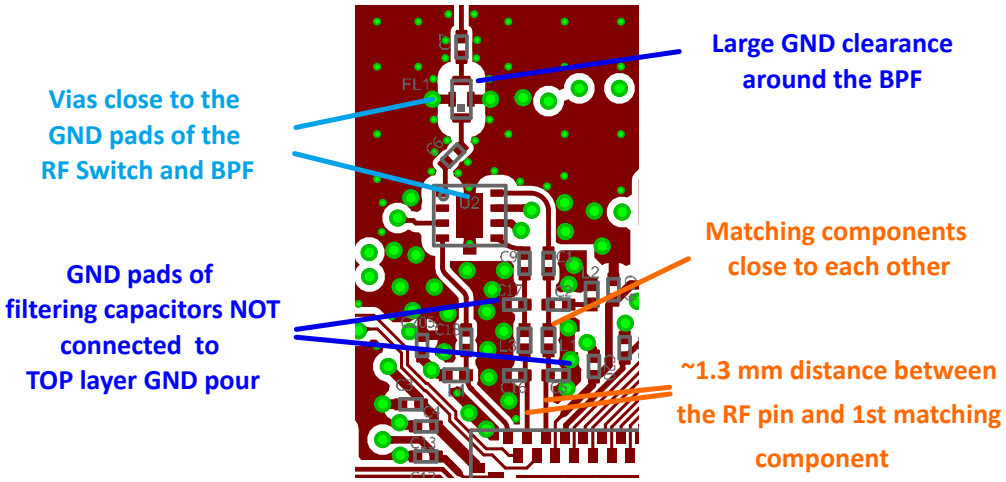

Figure 5.9. Layout of the Matching Network Section for the BRD4338A Radio Board with External RF Switch (Top Layer)

5.5 Power Supply Specific Layout Guidelines

- Place the VINBCKDCDC, VOUBCKDCDC, and VINLDOSOC external capacitors as close to the pins as possible. Use multiple GND vias close to their pads for proper ground connection.
- Form a GND “island” with multiple GND vias under the DCDC output inductor (L_DCDC) to isolate the two terminals of the inductor.
- Form power planes for good thermal management of the VDD traces. The separated power planes for the different VDD pins can be seen in the left figure below.
- Make sure that the trace from VOUBCKDCDC to VINLDOSOC is as short and as wide as possible (power plane is recommended).

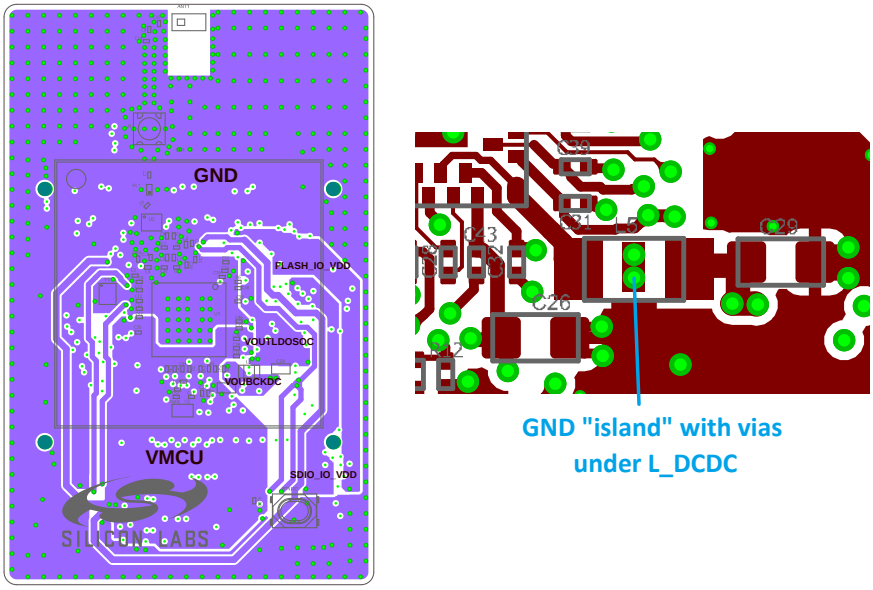

Figure 5.10. Layout of the Power Planes and DC-DC Converter Components on BRD4338A Radio Board with External RF Switch (Inner 4 and Top Layer)

6. Tested Alternative BPF and RF Switch Parts

The following tables and measurements show the alternative BPF and Switch parts that Silicon Labs has tested. The selection criteria were to choose three different parts each in three different price and expected performance ranges (low, medium, high). The components are not entirely footprint compatible with the Reference Parts.

The investigations included the following comparison measurements that were performed against the Reference Parts:

- Z_{IN} input impedance of the TX matching network with a 50 Ω termination on the output of the alternative part (the BPF measurements were done using the reference HWS520 RF Switch).
- S21 transfer characteristics (IL = insertion Loss). The measurements were done directly on the components.
- Insertion loss calculated from TX/RX measurements. The values are the average calculated from testing 18 different PHYs (lowest and highest data rate PHYs of 802.11b /g /n on channels 1, 7 and 11).
- 2nd harmonic emission measurements (conducted and radiated)

For visual understanding, the 50 Ω terminations for the VNA measurements can be seen in Figure 3.15 50 Ω Terminations for the Four Different Matching Network Input Impedance Measurements on page 20 (nr. 2 and 4).

Table 6.1. Performance of the Alternative Parts Compared to the Reference Parts

Reference Designator	Insertion Loss @2.45 GHZ (S21 VNA) [dB]	Insertion Loss @2.45 GHz (TX/RX) [dB]	2nd Harmonic [dB]		Part Number	Manufacturer
			Conducted	Radiated		
BPF	reference				LTB-1005-2G4H6-A2 (ref.)	Mag.Layers
	-0.2	-1.1	-0.9	-4	ADFC15-2450.00-A-T	Abracon
	-1.5	-1.6	-6	-10	DEA102450BT-1278A2	TDK
	0.8	0	-0.6	0.8	LFL1X2G45TU1E238	Murata (LPF)
RF Switch	reference		—	—	HWS520 (ref.)	Hexawave
	0.4	0.1			NJG1804K64-TE1	Nishinbo
	0.4	0.1			873-SKY13251-349LF	Skyworks
	0.3	0			PE42430MLAB-Z	Psemi

The conclusive measure for the performance of the alternative parts at the fundamental frequency is the insertion loss calculated from the TX/RX measurements. However, it is worth presenting the VNA measurements to understand the slight impedance transforming effects and transfer characteristics of the components. These metrics describe the passive components themselves, whereas the results from the TX/RX measurements are also influenced by how close the PA/LNA termination impedance is to optimal.

The BPF measurements on the VNA are shown in the figure below:

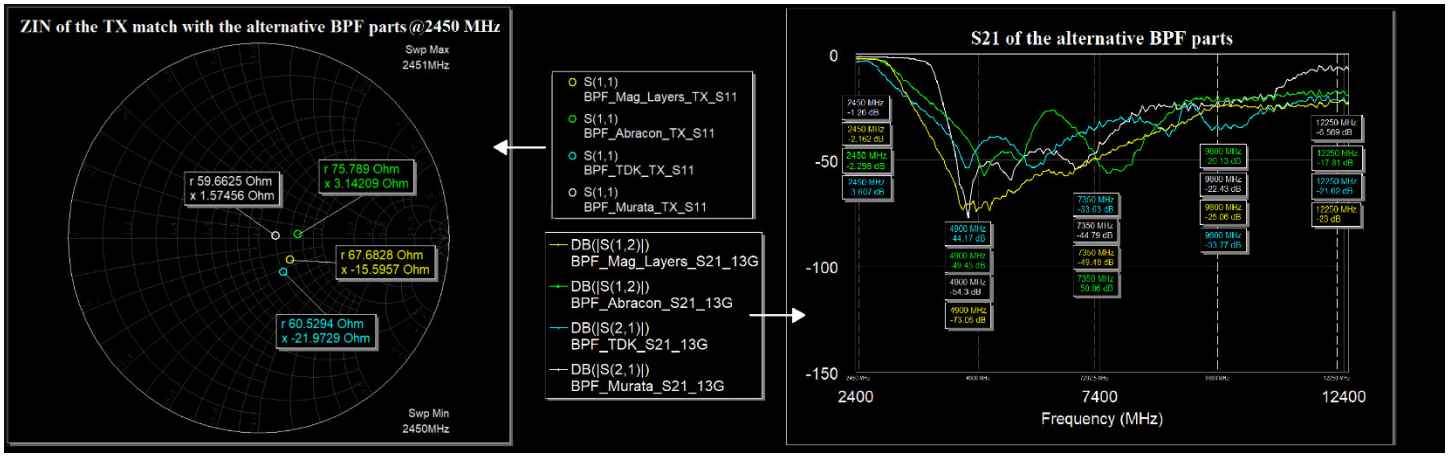

Figure 6.1. ZIN of the TX Match and S21 Transfer Measurements of the Alternative BPF Parts up to 13 GHz

The pass-band characteristics (-10 dB bandwidth) are displayed in the figure below:

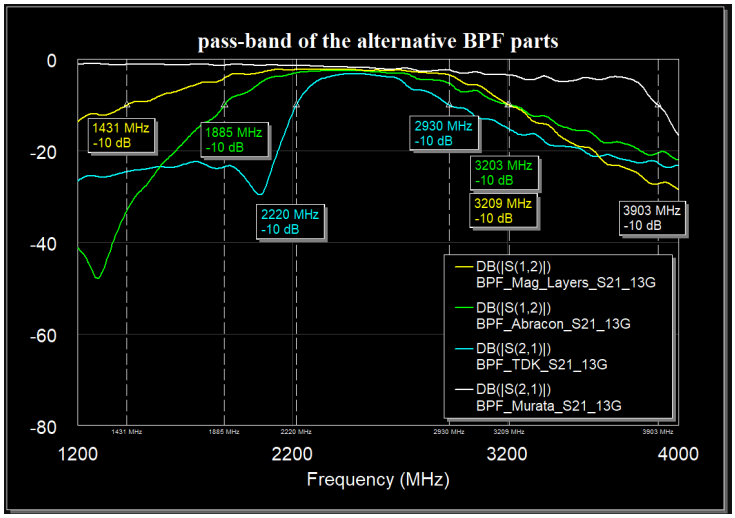

Figure 6.2. S21 Pass-Band Characteristics of the BPFs (-10 dB Bandwidths Marked)

The measurements suggest that:

- The different BPF parts introduce slightly different impedance transformations.
- The different BPF parts introduce different insertion losses at the fundamental 2.45 GHz and also different harmonic filtering.

The RF Switch measurements on the VNA are shown in the figure below:

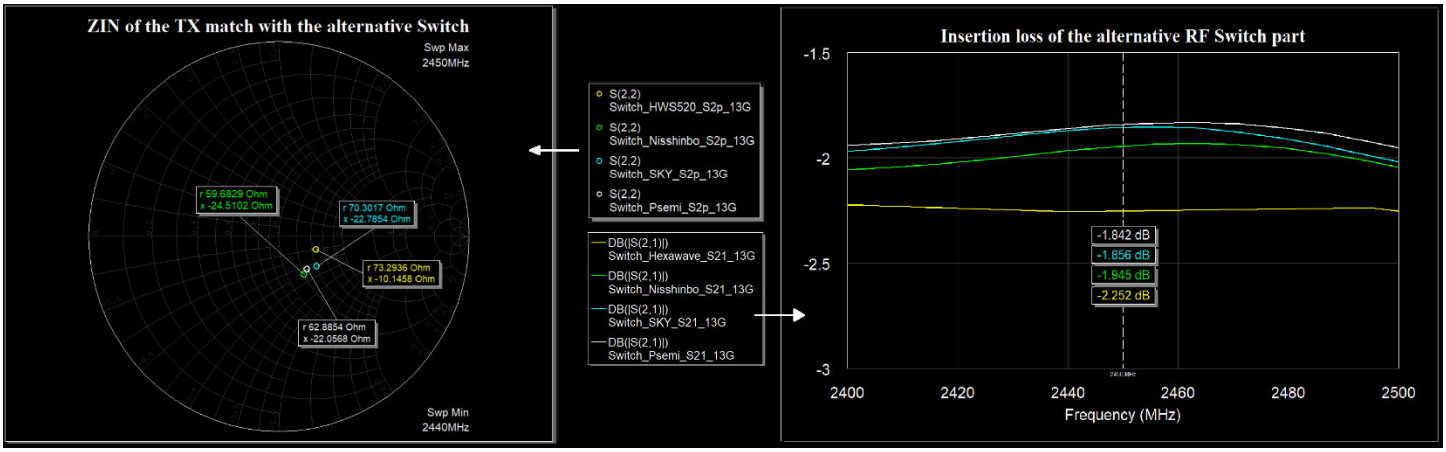

Figure 6.3. ZIN of the TX Match and S21 Insertion Loss (RF Switch) with the Alternative RF Switch Parts in the 2.4 GHz Band

The measurements suggest that:

- The alternative RF Switch parts introduce slightly different impedance transformations and HWS520 (yellow) is a relative outlier.
- The different RF Switch parts introduce very similar insertion losses at the fundamental 2.45 GHz.

Notice that the insertion loss of any element is made up of two main components:

1. Part of the signal is reflected back due to the mismatch at the input of the element placed into the system impedance (the loss is described by the transmission coefficient which is directly calculable from the reflection coefficient as S21 = S11 + 1).
2. Inherent attenuation inside the component due to dielectric and copper losses

As the insertion loss measurements were done with a VNA with 50 Ω ports, and the parts are also 50 Ω, the measured insertion loss is attributed mainly to the dielectric and copper losses inside the part.

7. Revision History

Revision 0.1

December 2023

- Initial version

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