AN1494: SiWx917 External Flash and PSRAM Application Note

This application note describes various Internal and External Flash/PSRAM configuration of SiWx917 IC and Module. It also describes recommended external flash and PSRAM parts and guidelines to select off-the-shelf flash/PSRAM parts.

Silicon Labs SiWx917 IC and Module includes a wireless subsystem and an integrated microcontroller application subsystem. The wireless subsystem consists of a Network Wireless processor (NWP) and the application subsystem consists of an ARM® Cortex® M4 processor (M4). This is a single-chip solution to simplify design, reduce cost, and speed up the time to market. It offers a variety of memory options to choose from, as described in the following sections.

KEY POINTS

- Package Options with Flash and PSRAM
- Flash Selection Criteria
- PSRAM Selection Criteria

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1. Introduction

SPI Flash Controllers

A serial flash device is a non-volatile memory that can be electrically erased and reprogrammed. It is used for storing executable code or data readily available for M4/NWP processor. After power-up, the executable code is read by the M4/NWP processor from the serial flash and then executed. The code in the serial flash is write-protected and cannot be altered.

Serial flash memories are controlled by many kinds of serial interface protocols (SPI, SSP, SSI, SMI, etc.). The SiWG917 supports SPI based flash. SPI flash memory is a secondary device.

To access it, dedicated QSPI flash controller is present which is Primary.

SiWG917 has a QSPI flash controller which has 2/4/8 - wired interface for serial access of data from flash. The QSPI controller can be used in either single, dual, quad or octal modes with support for SDR to read the processor's instructions and for data transfers to/from the flash. The controller supports inline decryption of encrypted instructions read from the flash before they are passed on to the M4/NWP processor's instruction cache. Instructions are read using the Direct Access mode while data transfers use the Indirect Access mode in case of the flash. The QSPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs. The Direct Access mode is used to read instructions and data directly from flash. It supports inline decryption using an AES engine for the instructions or data transfer with flash. The Indirect Access mode is used to read and write data/instructions from flash. The two modes - Direct Access and Indirect Access - can be used to access the same flash or two different flashes (using CSN0 and CSN1) at a time by enabling hardware-controlled mode. The QSPI controllers have independent AHB secondaries for these modes of access.

SiWG917 can use a single common SPI flash for executing instructions by both NWP and M4 processors. Each processor has a dedicated QSPI flash controller. Dynamic arbitration has taken place between two controllers without any processor intervention for executing instructions from common flash. Arbitration multiplexes the two SPI interfaces into a single SPI interface connected to the flash. The flash memory is partitioned into two parts dedicated to each processor respectively.

There are two flash configurations available, which are described further.

Common Flash Configuration

In the common flash configuration, flash is shared between both NWP and M4 processors. Flash Initialization, configuration, program and erase can be done only by NWP processor. M4 processor can do only instruction fetching in direct access mode. Flash memory is divided into two regions, one each for the processor. M4 can only read M4 assigned memory region. NWP has no restriction, and it can access complete flash memory.

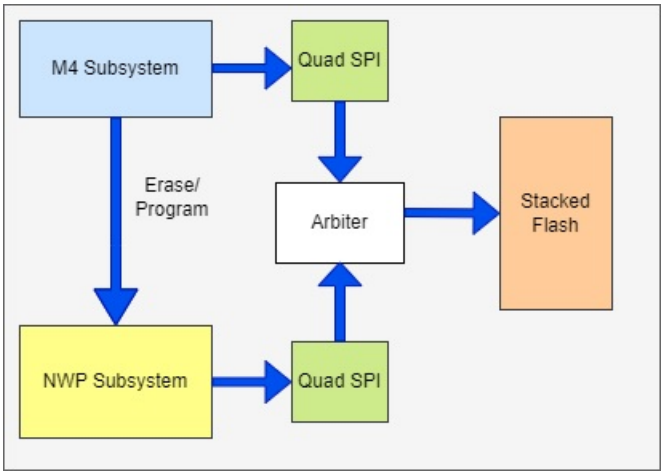

Figure 1.1. Common Flash Configuration

Dual Flash Configuration

In the dual flash configuration, each processor has its own dedicated flash memory. In this configuration, M4 can access complete flash memory. M4 can perform flash initialization, configuration, programming and erase.

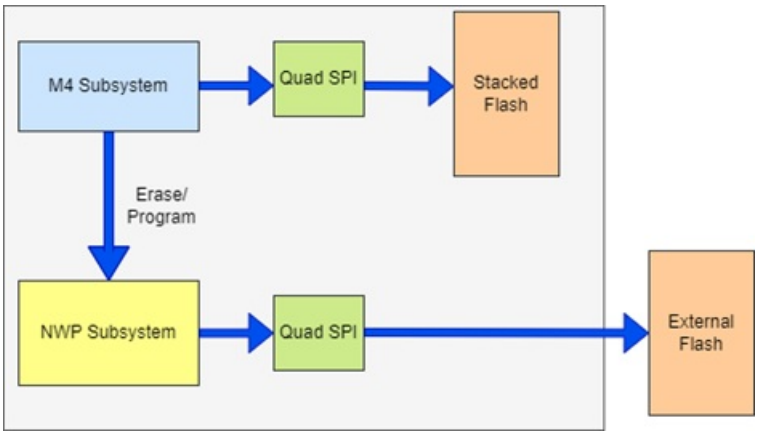

Figure 1.2. Dual Independent Flash Configuration

Flash/PSRAM SPI Features

Following are the features of the SPI Flash Primary Controller:

- Supports Single/Dual/Quad/Octal (S/D/Q/O) modes for reading M4/NWP processor instructions and data transfers to/from flash.
- Support for SPI Mode-0 and Mode-3
- Support for SDR mode flash
- Supports both 8 and 16-bit flash commands
- Support both 24 and 32-bit addressing modes
- Supports inline decryption (AES) in XTS/CTR mode with 128-bit and 256-bit key sizes while reading encrypted instructions from the flash
- Supports up to two flashes connected to CSN0 and CSN1
- **Direct Access Mode:**
  - Configuration of flash and reading/writing data from/to the flash uses the Indirect Access mode which requires the M4/NWP processor to program the SPI flash controller for each access.
  - Supports reading of upto 32 KB bytes of data from flash/PSRAM in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10, and 16-bit addressing in this mode.
- **Indirect Access Mode:**
  - Instructions are read from flash using the Direct Access mode which does not need any processor involvement after the initial configuration of the controller. The read command used for this mode is programmable depending on the flash used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from flash - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- **Common Flash Mode:** Flash can be accessed by both MCU and NWP simultaneously.
- **Clock Configuration:**
  - Support for selection of source clock between AHB bus clock and PLL clock
  - Support for even division factors upto 64 to generate the SPI clock from the source clock.
- Transmission of Extra-byte after the address phase is supported. The contents of this byte are programmable. There is also an option to only transmit the first nibble of the extra byte and maintain a Hi-z on the bus for the next nibble.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the flash requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports interrupt generation based on different events
- Supports **Dual Flash mode:** Reading of data from two flashes simultaneously
- Supports flash Write Protect

The SPI controller in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs from multiple vendors.

Note: The QSPI controller interface is available only for interface to serial flash devices. It cannot be used as a general SPI peripheral.

SPI PSRAM Controllers

For applications that require additional RAM, additional external RAM can be added in the form of pseudo static RAM (PSRAM). The PSRAM is an additional RAM of size that is selected e.g. 2/4/8/16 MB. PSRAM memory is a QSPI secondary device. M4 microcontroller communicates with the PSRAM through dedicated Quad SPI Primary controller.

SiWG917 has SPI PSRAM controller which has 2/4/8 - wired interface for serial access of data from PSRAM. Dedicated SPI controllers are present for PSRAM. It can be used in either Single, Dual or Quad modes with support for SDR to read the M4 processor's instructions and for data transfers to/from the PSRAM. The controller supports inline decryption of encrypted instructions read from the PSRAM before they are passed on to the M4 processor's Instruction Cache. The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs. The Direct Access mode is used to read instructions and read/write data directly to/from PSRAM. It supports inline decryption using an AES engine for the instructions or data transfer with PSRAM. The Indirect Access mode is used to read and write data/instructions from PSRAM. The two modes - Direct Access and Indirect Access - can be used to access the same PSRAM or two different PSRAM (using CSN0 and CSN1) at a time by enabling hardware-controlled mode. The SPI controllers have independent AHB secondaries for these modes of access.

SPI PSRAM Primary Controller Features

Following are the features of the SPI PSRAM Primary Controller:

- Supports Single/Dual/Quad (S/D/Q/O) modes for reading M4 processor instructions and data transfers to/from PSRAM
- Support for SPI Mode-0
- Supports full duplex mode in single-bit SPI mode. Support for HOST SPI secondary interface
- Support for SDR mode PSRAMs
- Supports both 8 and 16-bit PSRAM commands
- Support both 24 and 32-bit addressing modes
- Supports only AES CTR mode encryption and decryption of PSRAM data with 128, and 256-bit key sizes
- Supports up to two PSRAMs connected to CSN0 and CSN1
- Supports Direct mode write
- Supports semi direct mode read operation for PSRAM
- **Direct Access Mode:**
  - Data transfer from/to PSRAM using the Direct Access mode which does not need any M4 processor involvement after the initial configuration of the controller. The read/write command used for this mode is programmable depending on the PSRAM used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from PSRAM - this option makes the SPI controller post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- **Indirect Access Mode:**
  - Configuration of PSRAM and reading/writing data from/to the PSRAM uses the Indirect Access mode which requires the M4 processor to program the SPI controller for each access.
  - Supports reading of up to 32 KB bytes of data from PSRAM in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10 and 16-bit addressing in this mode.
- **Clock Configuration:**
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the PSRAM requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports configurable memory ranges on which we can save code in encrypted form and the execution will happen with inline decryption.
- Supports dual PSRAM mode - reading and writing from/to two PSRAM simultaneously
- Supports interrupt generation based on different events

The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs from multiple vendors.

2. Flash and PSRAM Package Option

There are four unique configuration options for flash and PSRAM connection to the SiWG917:

- In-package flash/PSRAM
- Only external Flash
- In-package PSRAM and external flash
- In-package Flash and external PSRAM

Table 2.1. Flash and PSRAM Package Options and Supply Connection Details

Mode	Configuration	GPIO pins	Suggested OPN	Supply connections
Mode 1	In-package Flash	0:5	SiWG917M100MGTBA	Flash_IO_VDD to be used
Mode 2	• In-package PSRAM • External Common Flash	• 0:5 (PSRAM) • 46:51 (M4 Flash)	• SiWG917M141XGTBA • SiWG917M121XGTBA	Option 1: In-package generated Flash LDO output 1.8V is connected to PSRAM; Implication on higher standby associated power **Recommended** Option 2: External LDO 1.8 V source from customer board to be connected Flash_IO_VDD and VOUTLDO1p8 to external Flash and IO_VDD_1
Mode 3	External Common Flash	46:51	SiWG917M111XGTBA	**Recommended** Option 1: VOUTLDO1p8 to be connected to External Flash and IO_VDD supply pin. Option 2: Alternative: Use wide range Flash (1.8-3.3 V) and connect wide range power so that there is no restriction on MCU Peripheral voltage choice.
Mode 4	External Dual-flash	• 46:51 (NWP Flash) and • 52:57 (M4 Flash)	SiWG917M111XGTBA	**Recommended** Option 1: VOUTLDO1p8 to be connected to External Flash and IO_VDD supply pin. Option 2: VOUTLDO_1P8 or 3.3V to flash and IO_VDD_1 depending on MCU Peripheral choice (1.8 V or 3.3 V).

Mode	Configuration	GPIO pins	Suggested OPN	Supply connections
Mode 5	• In-package Common Flash • External PSRAM	• 0:5 (Flash) • 46:51 (PSRAM) OR 52:57 (PSRAM)	SiWG917M111MGTBA Module OPN : • SiWG917Y110LGNBA • SiWG917Y111MGNBA • SiWG917Y110LGABA • SiWG917Y111MGABA	Option 1: VOUTLDO_1P8 to External PSRAM. So MCU Peripheral 1.8V **Recommended** Option 2: External LDO 1.8 V source from customer board to be connected for External PSRAM and IO_VDD_1, Flash_IO_VDD and VOUTLDO1p8 to In package Flash.
Mode 6	• In-package Flash • External Flash	• 0:5 (NWP Flash) • 46:51 (M4 Flash)	SiWG917M100MGTBA	**Recommended** Option 1: VOUTLDO1p8 need to be connected to both In-package Flash and external Flash and IO supplies (IO_VDD_1 and FLASH_IO_VDD) Option 2: External LDO 1.8 V to both In-package Flash and external Flash and IO supplies (IO_VDD_1 and FLASH_IO_VDD) Option 3: In-package Flash LDO 1.8 V to be connected to In-package Flash and FLASH_IO_VDD. External LDO 1.8V/3.3V is connected to external Flash and IO_VDD_1.

Example supply connections for different cases are shown in the figures below.

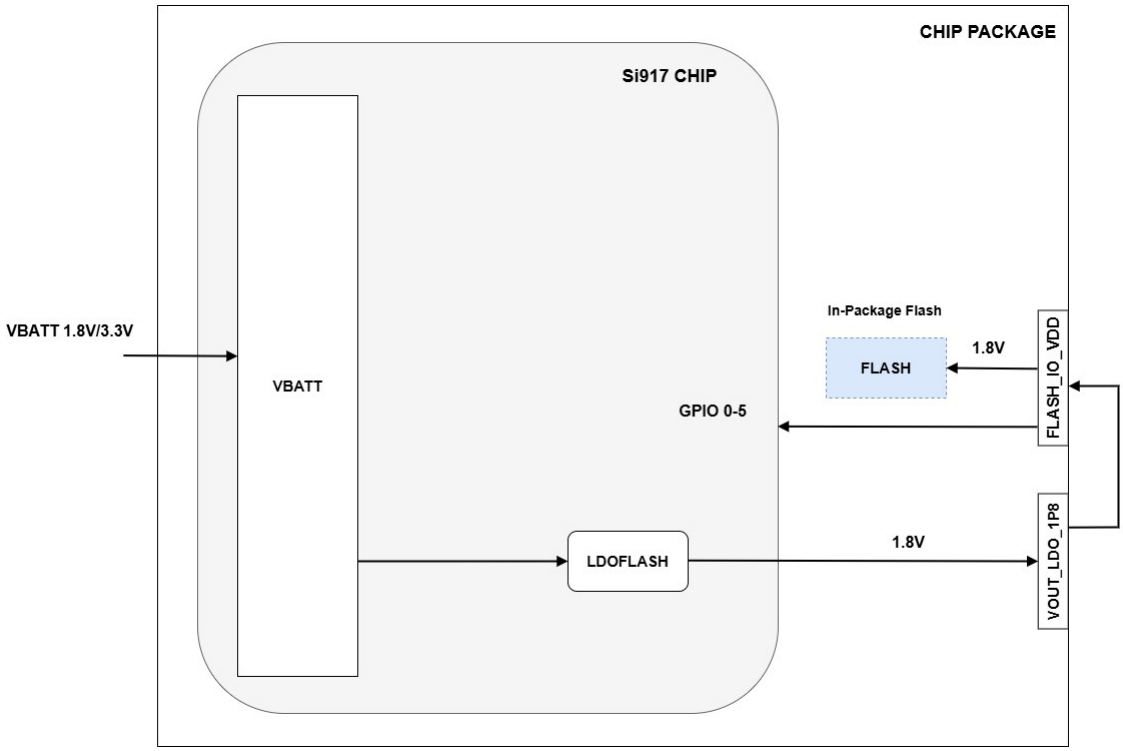

Figure 2.1. In-PackageFlash supply Connections (Mode1)

In Figure 2.1 In-PackageFlash supply Connections (Mode1) on page 9 in-package flash supply connections (Mode1) the on-chip 1.8 V flash LDO is connected to the VOUT_LDO_1P8 pad via PCB routing. VOUT_LDO_1P8 is connected to the FLASH_IO_VDD pad which is the input supply for the in- packageflash and respective GPIOs. In this case, IO_VDD_1 gets the supply from VBATT which can operate at either 1.8 V or 3.3 V depending upon the peripherals connected on these GPIOs.

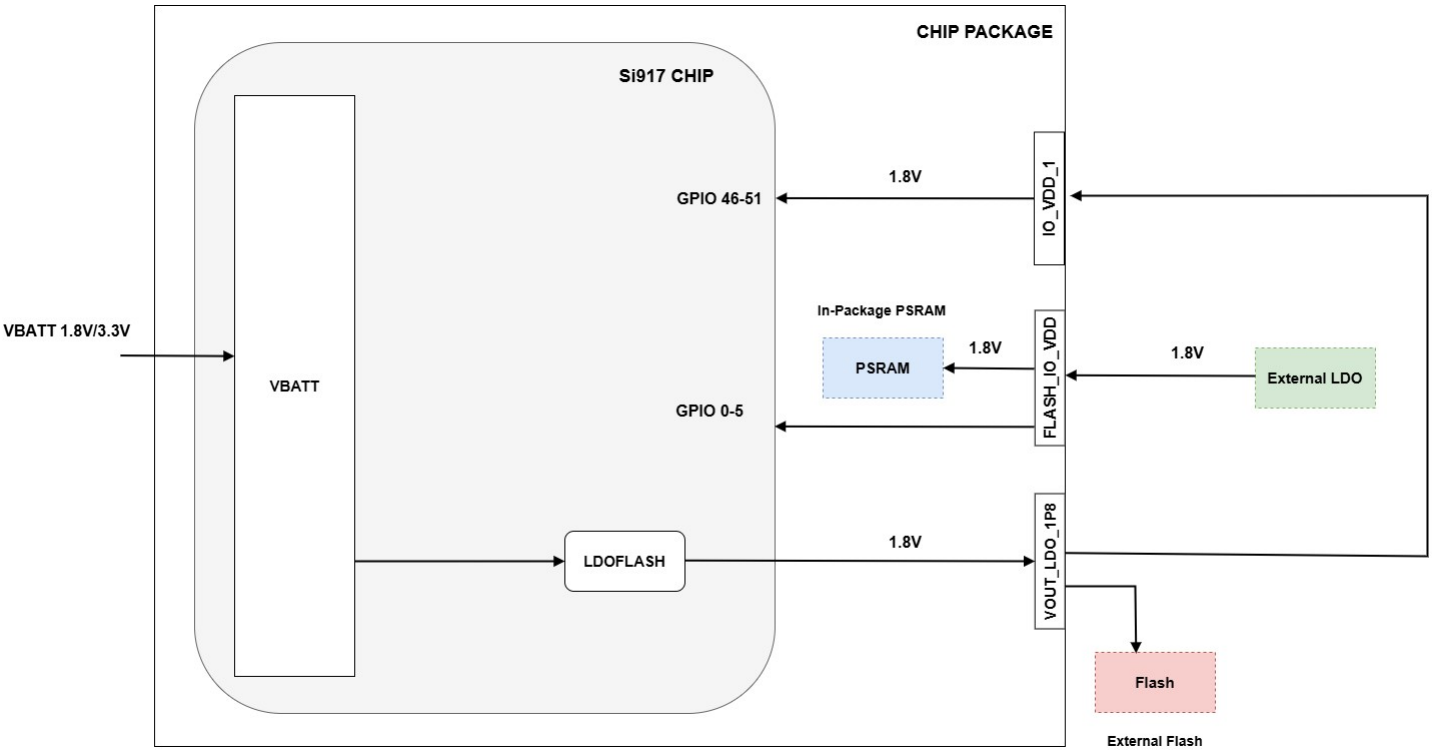

Figure 2.2. In-Package PSRAM, External Common Flash(Mode 2, Option 2)

In Figure 2.2 In-Package PSRAM, External Common Flash(Mode 2, Option 2) on page 9 External LDO is used to power up Inpackage PSRAM and Internal Flash LDO to power up External Flash and dedicated GPIOs for lower stand by currents.

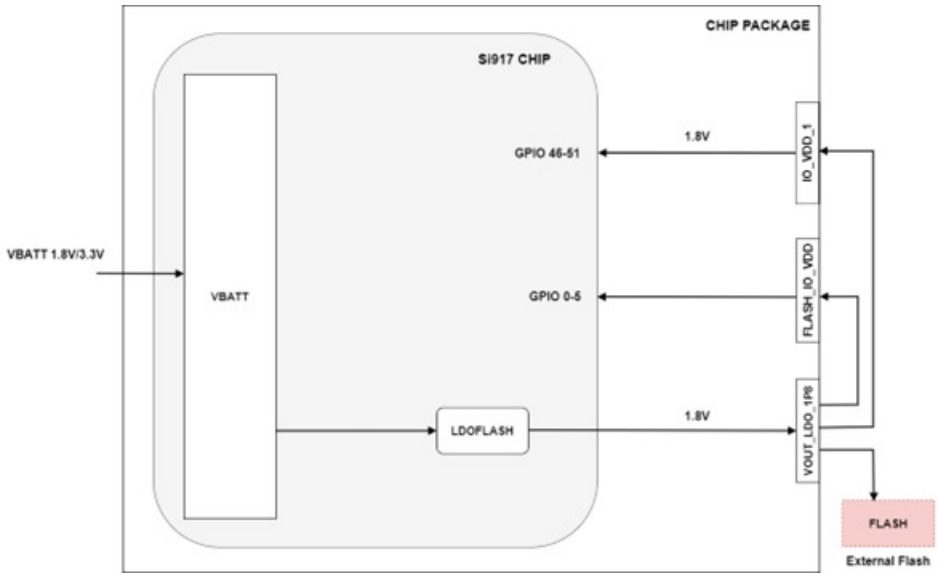

Figure 2.3. External Common Flash(Mode 3, Option 1)

In Figure 2.3 External Common Flash(Mode 3, Option 1) on page 10 External flash is powered through Internal Flash LDO supply VOUTLDO1P8 which is also connected tothe FLASH_IO_VDD pad (connects to GPIO 46-51).

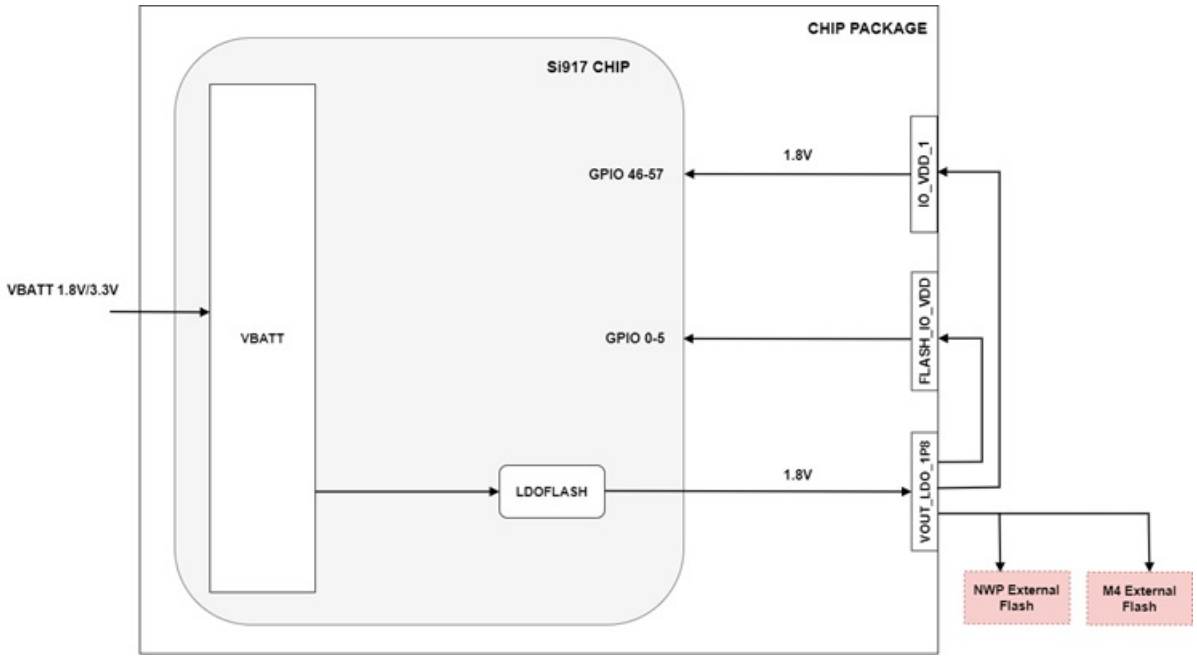

Figure 2.4. External Dual Flash (Mode4, Option 1)

In Figure 2.4 External Dual Flash (Mode4, Option 1) on page 10 External Dual Flash configuration, on-chip LDO supply the on-chip 1.8 V flash LDO is connected to VOUT_LDO_1P8 pad via PCB routing. VOUT_LDO_1P8 is connected to the FLASH_IO_VDD pad. The VOUT_LDO_1P8 supply is also connected to the external Flash and IO_VDD_1 which powers GPIOs 46-57 for NWP and M4 dedicated GPIOs.

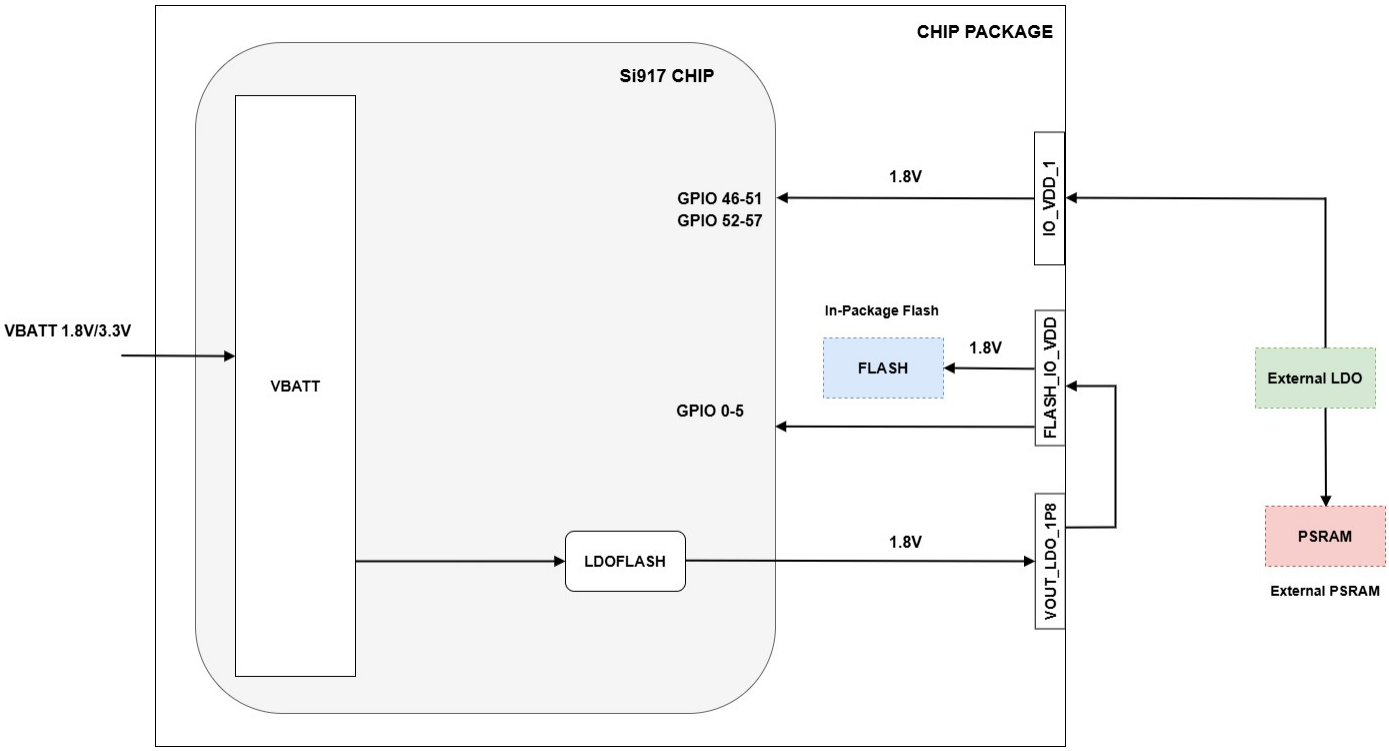

Figure 2.5. In PackageFlash and External PSRAM (Mode 5, Option 2)

In Figure 2.5 In PackageFlash and External PSRAM (Mode 5, Option 2) on page 11 In-package flash and external PSRAM, an external 1.8 V supply is connected to the External PSRAM and IO_VDD_1 (connects to GPIO 6-12 and GPIO 46-57). The VOUT_LDO_1P8 supply pin is connected to FLASH_IO_VDD for In package flash.

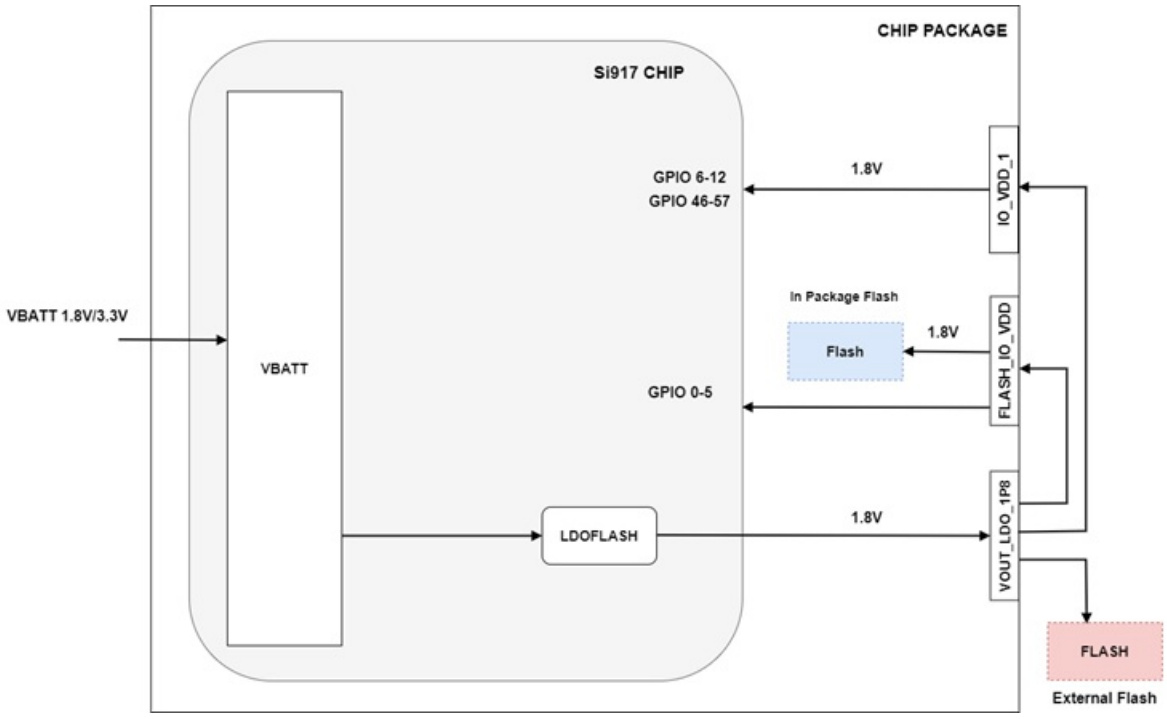

Figure 2.6. In-PackageFlash and External Flash Powered from On-Chip LDO Supply (Mode 6, Option 1)

In Figure 2.6 In-PackageFlash and External Flash Powered from On-Chip LDO Supply (Mode 6, Option 1) on page 11 in-package Flash and external flash powered from on-chip LDO supply (Mode 6, Option 1) the on-chip 1.8V flash LDO is connected to VOUT_LDO_1P8

pad via PCB routing. VOUT_LDO_1P8 is connected to the FLASH_IO_VDD pad which supplies the in-package Flash and GPIOs 0-5. The VOUT_LDO_1P8 supply is also connected to the external flash and IO_VDD_1 which powers GPIOs 6-12 and 46-57.

3. Recommended External Flash and PSRAM

The SPI controllers in the MCU have been designed with programmable options for most of the single- and multi-bit operations so that it can interface with flash ICs and PSRAM ICs from multiple vendors. The list of supported flash/PSRAMs and vendors is given below:

Table 3.1. Flash

S.No.	Vendor	Part #	Flash Density (in Mbit)	V_{cc} (in V)	Bus Width (in bits)
1	GigaDevice	GD25LE32E	32	1.65-2.0	1/2/4
2	GigaDevice	GD25LE64E	64	1.65-2.0	1/2/4
3	Macronix	MX25R3235F	32	1.65-3.6	1/2/4
4	Macronix	MX25U3235F	32	1.65-2.0	1/2/4
5	XMC	XM25QU32CK	32	1.65-1.95	1/2/4

Table 3.2. PSRAM

S.No.	Vendor	Part #	Memory Density (in Mbit)	Vcc (in V)	Bus Width (in bits)
1	AP memory	APS1604M-SQR	16	1.65-1.95	1/2/4
2	AP memory	APS6404L-SQRH	64	1.65-1.95	1/2/4
3	AP memory	APS6404L-3SQR-ZR	64	2.7-3.6	1/2/4
4	AP memory	APS1604M-3SQR-ZR	16	2.7-3.6	1/2/4

Note: [**APS6404L-SQRH**] does not support Half-Sleep mode. You might not achieve the actual deep-sleep current numbers.

4. Flash Selection Criteria

- Should support SPI mode 0
- Should support single, dual and quad modes
- DDR mode is not supported
- Octa mode is not supported
- Max size is 16 MB. (16 MB flash planned for future support)
- Minimum 8 MB flash for standard wireless FW option, 4 MB flash for Lite-Wireless FW option (For Common flash)
- For Dual-Flash depends on customer requirements. (Range from 1 to 16 MB for external M4 Image)
- Supply voltage can be 1.8 V or 3.3 V. 1.8 V is preferred and can be supplied through flash LDO. 3.3 V must be externally supplied
- Frequency > 80 MHz for all commands excepts 03 or 0B
- Clock low to output valid delay ≤ 8ns
- V_{cc} min to flash accessibility should be around 1 msec. Recommended < 1.2 msec
- Power ratings (active, standby currents) to be decided by customers

5. PSRAM Selection Criteria

- PSRAM should support SPI mode 0
- Should support single-, dual-, and quad-modes
- DDR mode is not supported
- Octa mode is not supported
- Should support linear bursting (row boundary crossing)
- Maximum size is 16 MB but only planned for future support
- Supply voltage can be 1.8 V or 3.3 V. 1.8 V is preferred and can be supplied through flash LDO. 3.3 V must be externally supplied
- Frequency > 80 MHz for all commands excepts 03 or 0B
- Clock low to output valid delay ≤ 8ns
- CSN low time should be as high as possible
- Power ratings (active, standby currents) to be decided by Customers

Note: The above Selection Criteria for Flash and PSRAM confirms support from Hardware perspective. App Note related to External Memory support from SW perspective will be released soon.

6. Revision History

Revision 0.1

December, 2024

Initial release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com