AN1511: SiMG301 Single-layer Hardware Design Example

Manufacturing a product with multiple multilayer circuit boards is expensive. We offer a cost effective solution for a single-PCB, single-layer smart light bulb design, powered by the Series 3 SiMG301 Wireless SoC, integrating a high-performance radio with up to +10 dBm output power and LED pre-driver peripheral.

The design example demonstrates the possibility of putting the mains power supply, the radio interface and the LED power section on a single-layer metal core PCB with a diameter of 40 mm, enabling lower cost of manufacturing and better thermal performance, while not compromising on RF performance.

Note: This release of the Application Note focuses on the RF performance aspects of such a design. The power supply and the LED driver will be documented in more detail in subsequent releases.

KEY POINTS

- Mains power supply, radio interface, and LEDs all on a metal core single copper layer PCB
- Integrated LED driver to reduce external component count
- Aluminum core to enhance heat spreading
- Nominal LED power of 8 W
- 2.4 GHz +10 dBm with external monopole antenna

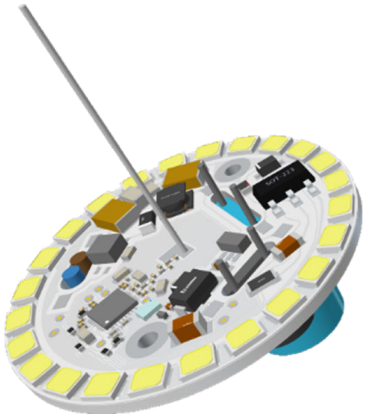


Table of Contents

1. Introduction

1.1 What Problems Does the Design Solve?

This Application Note aims to help with the design of a smart light bulb with lower manufacturing costs. General guidelines are explored through the specific circuit board designed for this application, featuring a single-layer metal core PCB. The aluminum core enhances its thermal performance required by LED bulbs, while also serving as a ground plane for the antenna. The SiMG301 Wireless SoC integrates an LED pre-driver peripheral, optimizing board real estate and BOM costs.

1.2 Simplified System Block Diagram

This diagram shows the simplified architecture of the electronic part of the design. This does not include the recommended external current limiting resistor, nor the mechanical or thermal interfaces.

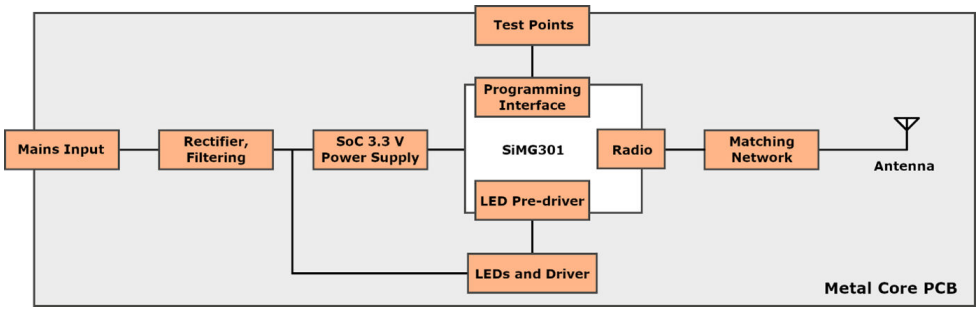


Figure 1.1. A system-level overview of the design

1.3 SiMG301 LED Pre-Driver Peripheral and the Power Supply

This version of the Application Note does not describe the pre-driver peripheral in detail. A subsequent release will include the system-level design requirements, considerations and measurement results regarding the power electronics sections.

2. Layout Design Guidelines

2.1 Single-Layer Metal Core PCB

To comfortably fit in a small light bulb, the design was constrained to a circular shape with a diameter of 40 mm. On the board edge, the LEDs can be found with their pads extended by copper pours to enhance thermal coupling to the metal core, improving diode cooling capabilities.

Two mounting holes are located on opposite sides of the board and are fitted with M2 screws from the top, placing them on the side opposite the antenna. These can be used to secure the PCB to an enclosure, tying it to the circuit ground (not Protective Ground). Since the circuit is entirely drawn on a single layer, with the added difficulty of having to keep high-voltage clearances, adequate ground connections could not be achieved. Thus, the screws are required to be populated even if they are not mechanically necessary.

The design files can be found according to 4.1 Reference Design Schematics and PCB design in the 4. Appendix.

2.1.1 Stackup

An aluminum core, single copper layer PCB was designed with the following layer structure, for a total thickness of 1.6 mm.

Table 2.1. PCB stack-up

Layer	Height	Material
Solder Mask	0.01 mm	Dk = 3.5
Signal Layer	0.035 mm (1 oz/ft^2)	Copper
Dielectric Layer	0.12 mm	Dk = 4.8
Metal Core	1.445 mm	Aluminum

The circuit was manufactured on the AL-01-B10 Aluminum-based Copper-Clad Laminate. For more information about the materials, refer to its documentation. To be able to use the same matching network element values, both the layer stackup and the matching network layout must be followed closely.

2.1.2 Metal Core as Ground Reference

Designing a radio frequency circuit on a single layer that complies with regulatory requirements is a challenge. The closest thing to a ground reference plane is the aluminum core itself, which is connected to the circuit ground both directly with two M2 screws, and through capacitive coupling. Although this is not ideal compared to multilayer circuits, measurements supported the viability of this construction.

2.2 High Voltage Clearances

As the LED driver uses a voltage-increasing topology, the peak voltage difference between the high and low voltage parts of the circuit is given by adding the voltage of the LED chain to the rectified AC peak voltage. Supplied from 230 V mains, this results in a maximum difference of around 350 V, requiring attention from the designer.

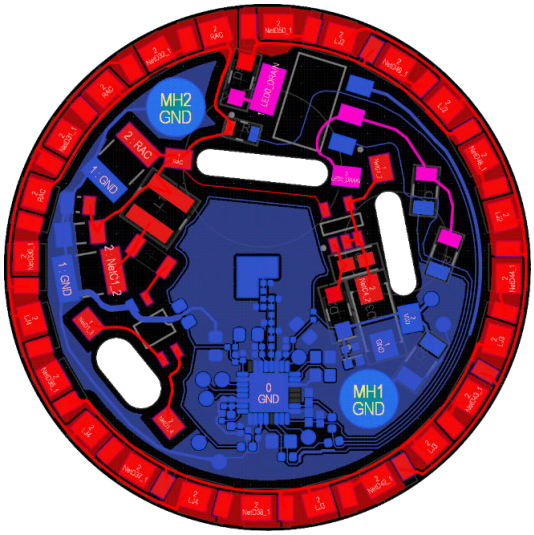


Figure 2.1. High and low voltage sections (marked red and blue, respectively) illustrating class separation. Both include the FET drain (magenta)

2.2.1 Conformal Coating

Such a design must comply with the effective safety standards regarding minimum clearance and creepage for given potential differences. Although an off-board fuse can lower the necessary distances according to some regulations, minimizing the probability of dielectric breakdown is recommended to enhance product lifespan.

Since the board has circular outline with a diameter of only 40 mm, conformal coating is applied, reducing the required clearance distances, enabling the compact design with a lower probability of breakdown. Although this works on most of the board, only the outer surface is being protected, traces under components are not. As a rule, a clearance of 0.7 mm was used between high and low voltage sections, with manual care for keeping more separation in areas not coated.

2.2.2 Component Pin Clearances

Although smaller packages may be available that otherwise meet electrical requirements, for some of the components, larger packages must be selected just to meet the clearance requirements between their pins belonging to high voltage difference nets.

2.3 Through-Hole Component Mounting Options

Since an aluminum core was used, through hole components must be mounted differently from typical designs. Every hole is drilled all the way through the metal core, leaving the bare aluminum shaft, which is tied to ground. Fitting a TH part would short its leads to GND.

This design utilizes a Bent Lead solution, which, along with an alternative mounting style, can be seen in figures Figure 2.2 Through-Hole component mounting options: Bent Lead on page 6, and Figure 2.3 Through-Hole component mounting options: Bottom Entry Connector on page 6.

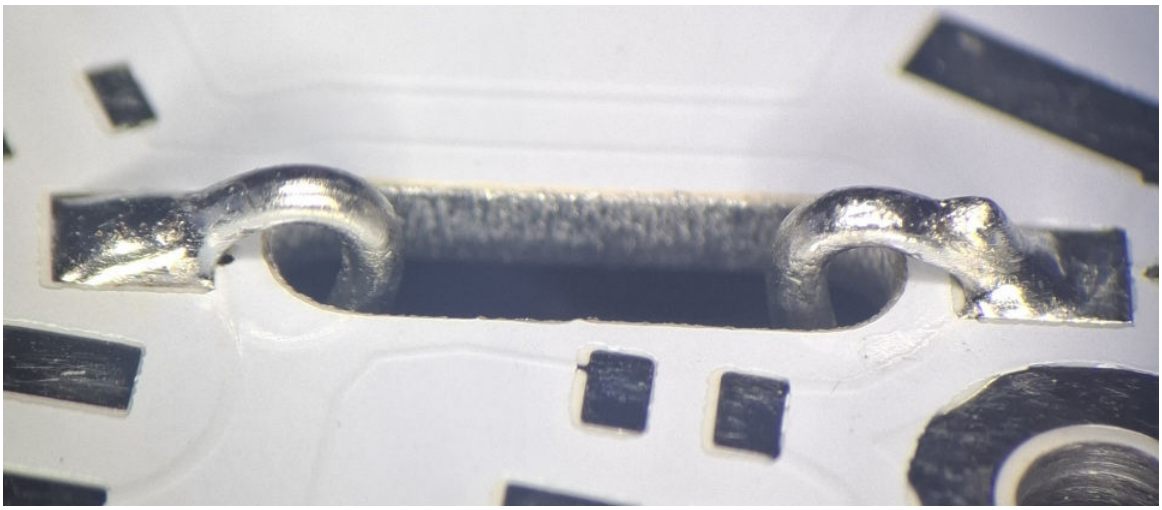


Figure 2.2. Through-Hole component mounting options: Bent Lead

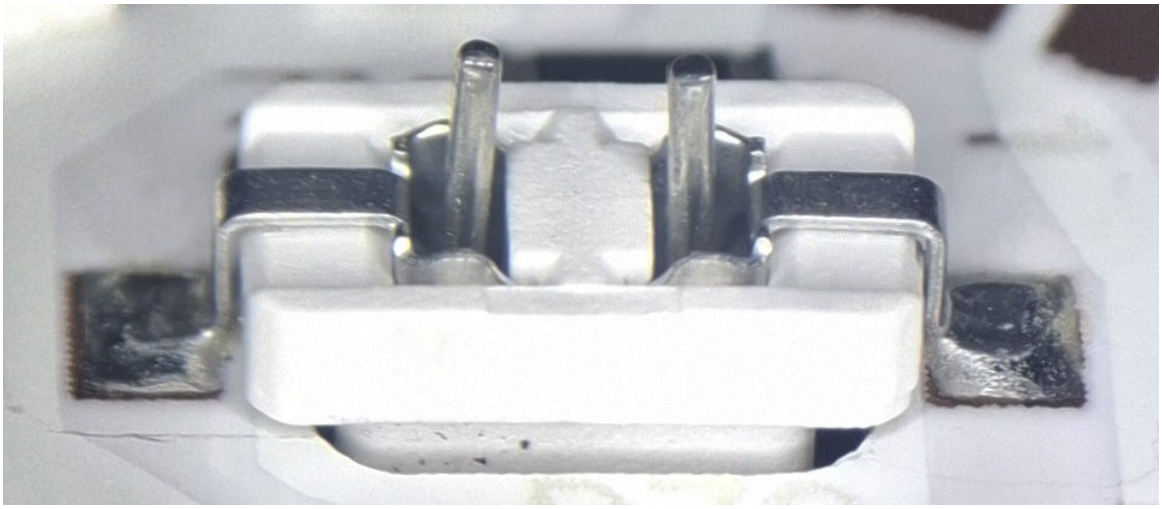


Figure 2.3. Through-Hole component mounting options: Bottom Entry Connector

2.4 RF Considerations

Vias cannot be used to stitch the top-layer ground to a ground plane below, nor can they be used to route signals beneath it. To create a sufficient ground plane for the antenna, multiple patches of ground pours are connected with jumpers, as seen in the following sections.

To further improve the grounding, some of the unused GPIO pins are disabled and shorted to ground to provide a clear path for the ground return currents.

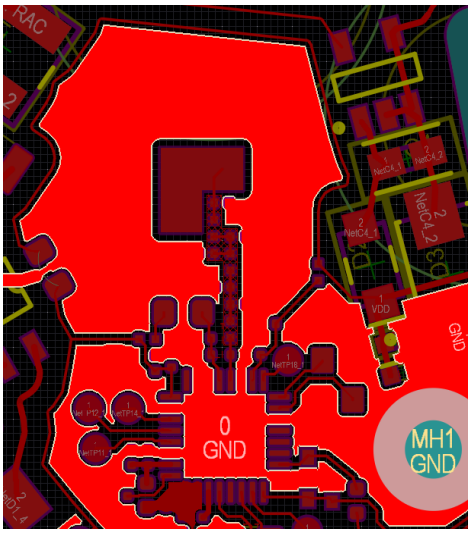


Figure 2.4. Extra ground connections through unused GPIO pins

2.4.1 Matching Network Layout

A matching network layout was designed with simulation tuned elements. If more filtering is necessary, extra tuning element slots are available in parallel.

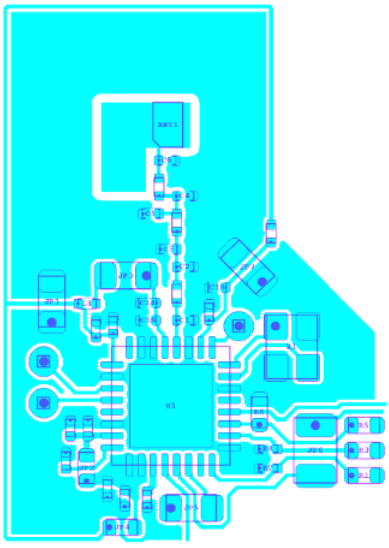


Figure 2.5. Simulated matching network layout

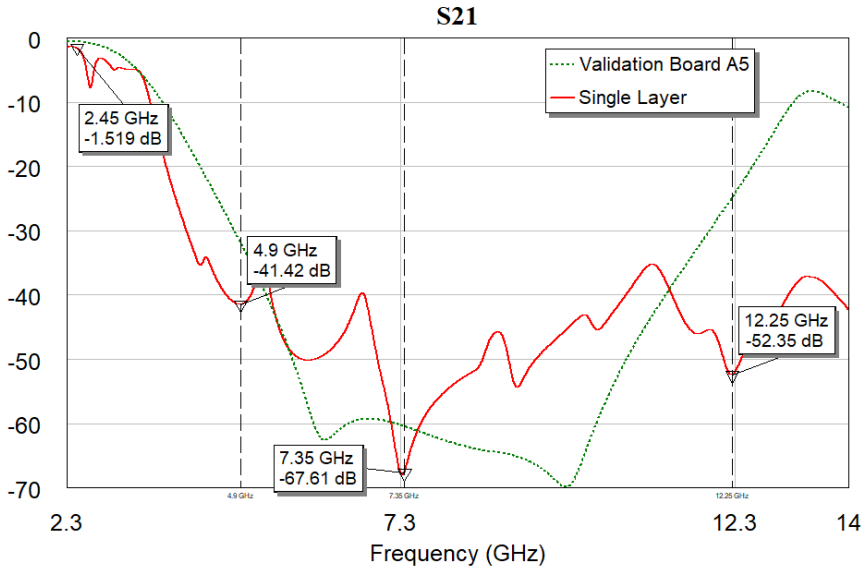


Figure 2.6. Simulated harmonic suppression

The designed layout was evaluated and tuned using EM simulation, with emphasis on third and fifth harmonic suppression. Figure 2.6 Simulated harmonic suppression on page 8 shows that the expected result performs adequately when compared to the BRD4407A 4-layer reference design.

During the final PCB design process, slight modifications have been made to this layout. The ground plane was extended outwards as much as possible to improve antenna efficiency. Non-RF critical components have been added, replaced or moved. Overall, no changes were made that would negatively impact RF performance.

2.4.2 Antenna

A simple monopole antenna is soldered to the antenna pad found on the center of the PCB. Its length is nominally 31.25 mm, which is quarter wavelength at the 2.4 GHz band. This size can fit inside a typical light bulb.

The area surrounding the antenna pad should be dedicated as a ground plane. Board real estate is limited, so a tradeoff must be made between RF performance and occupied area. The LED pre-driver enables the designer to use fewer external components, saving space, resulting in better potential radio performance.

3. Testing and Results

3.1 Safety Precautions

To reduce risk of injury and damage, whenever reasonable, the device was powered externally from a 3.3 V source (typically the WSTK/WPK main board) during measurements, to leave the high-voltage section unused. However, if the setup required the HV power supply, other safety measures had to be in place.

When planning to test the device on mains voltage, always ensure proper safety precautions are in place before powering the setup.

- Utilize an isolation transformer. Have an easily accessible safety switch on the secondary.
- Limit DUT current with a series power resistor of around 5-10 ohms, which also functions as a fuse.
- When connecting the device to any equipment galvanically, ensure the wires, probes and the equipment are rated for voltages up to at least 400 V. Note that connecting any equipment this way may affect isolation. Pay special attention to non-isolated probes, for example a single-ended oscilloscope probe ground being connected to protective earth.
- If possible, all communication interfaces between the DUT and a host should be galvanically isolated.

An isolation transformer and a Ground-Fault Current Interrupter (GFCI) cannot be used simultaneously when protective earth is galvanically connected to the device (for example through a single-ended probe referenced to GND). Leakage currents may make the GFCI trip, rendering the setup unreliable, and at the same time, referencing to earth after isolation undermines the protective effect of the circuit interrupter.

3.2 RF Measurements

3.2.1 Matching Networks

The final matching network element values can be seen in Table 3.1 Bench tuned matching network element values on page 10, with Figure 3.1 Complete matching network on page 10 showing their arrangement. Note that these values are tuned for the particular matching network layout and board stackup used in this design. Both the layout and the stackup must be followed in order to obtain the same results without retuning.

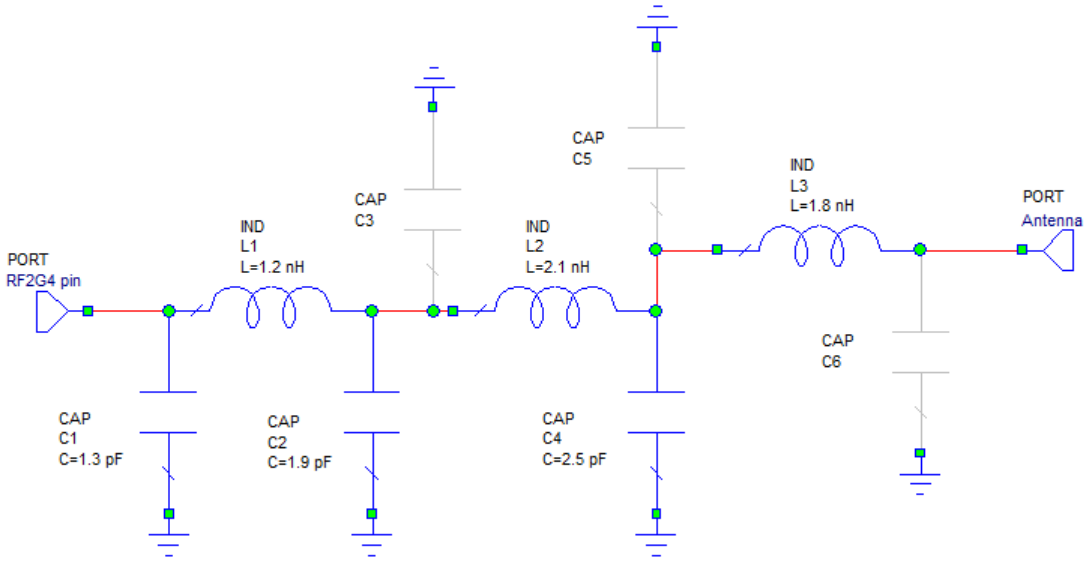


Figure 3.1. Complete matching network

Table 3.1. Bench tuned matching network element values

Designator	Value	OPN
C1	1.3 pF	GRM0335C1H1R3BA01
L1	1.2 nH	LQP03HQ1N2W02D
C2	1.9 pF	GRM0335C1H1R9BA01
C3	NP	—
L2	2.1 nH	LQP03HQ2N1W02D
C4	2.5 pF	GRM0335C1H2R5WA01D
C5	NP	—
L3	1.8 nH	LQP03HQ1N8W02D
C6	NP	—

The PA matching network was assembled using simulation tuned elements, terminated by a 50-ohm resistor. An RF “pigtail” probe was soldered to the RF output pad, setting the reference plane to the output of the IC, where the optimal PA termination impedance is known for a range of metrics.

The BRD4407A Radio Board was used for reference, measured port parameters are plotted over the 10 dBm PA output power load pull measurement of the SiMG301. Since the simulation tuned elements resulted in an acceptable impedance at the fundamental, no change was made at this stage.

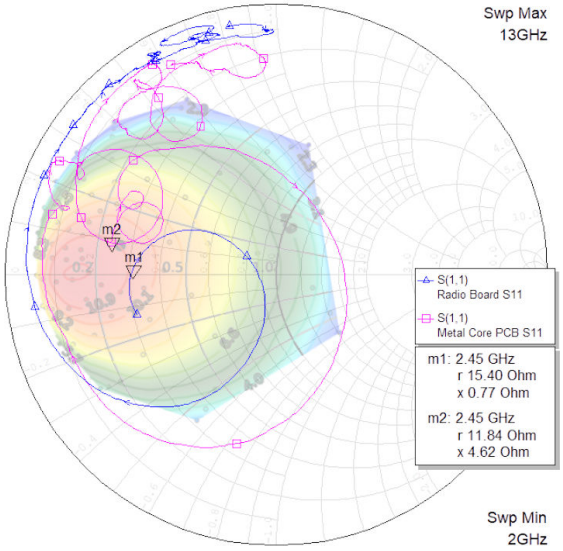


Figure 3.2. BRD4407A vs Metal Core PA match comparison

In a different setup, a quarter wave monopole antenna was soldered to the center pad. Since the PA matching network is designed for optimal RF performance considering a 50-ohm termination, the antenna impedance was tuned to 50 ohms, as seen on Figure 3.3 Antenna match impedance curve on page 11.

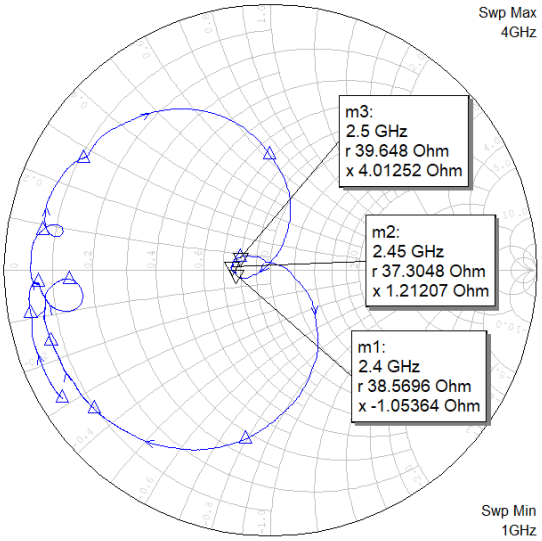


Figure 3.3. Antenna match impedance curve

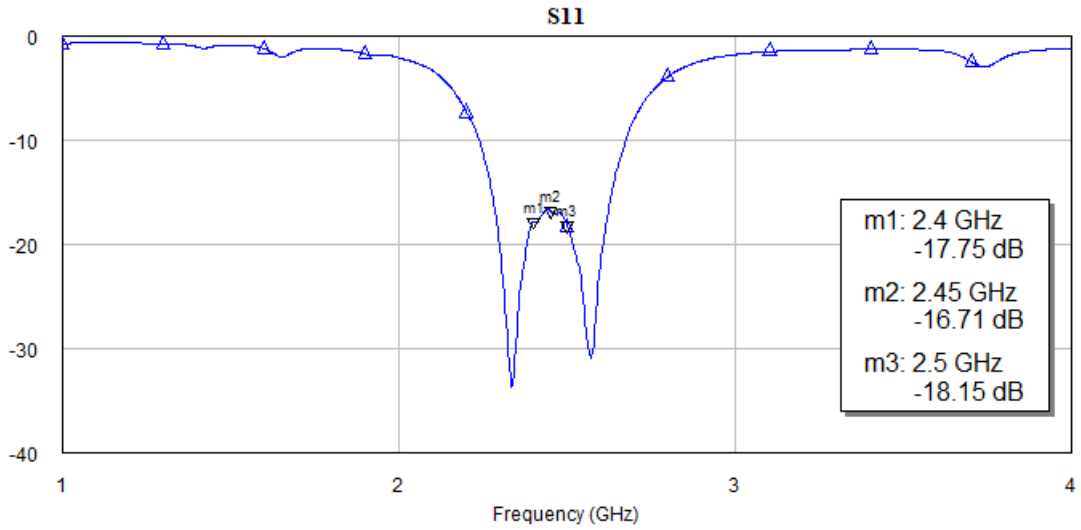


Figure 3.4. Antenna match return loss [dB]

Figure 3.4 Antenna match return loss [dB] on page 12 shows that the return loss of the ANT match is at least 16.6 dB over the 2.4 GHz band.

3.2.2 Radiated TX Power

An anechoic chamber was used to determine EIRP at the fundamental and harmonic frequencies. Following are two sets of tables, containing data from two power settings at the band edges and center frequency.

Table 3.2. Worst Case Radiated Harmonic Emissions at Maximum Power (CW tone)

Frequency	Measured maximums in EIRP [dBm]	Orientation and frequency of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP at max. [dBm]
Fund.	16.5	XY/V, 2450 MHz	13.5	30.0
2nd harm.	-46.3	XY/H, 2480 MHz	5.1	-41.2
3rd harm.	-25.2	YZ/H, 2480 MHz	-16.0	-41.2
4th harm.	-56.4	XY/V, 2480 MHz	52.6	-3.8
5th harm.	-42.2	YZ/H, 2480 MHz	1.0	-41.2
6th harm.	-47.6	YZ/H, 2480 MHz	43.8	-3.8

It is apparent that the third harmonic fails the regulatory margin, but this is somewhat expected as the fundamental output power is over the 10 dBm the SiMG301 is rated for. Due to the antenna gain in the maximum direction of radiation, 16.5 dBm is observed at the fundamental – actual output power without the effects of an antenna can be found in the Table 3.3 Worst Case Radiated Harmonic Emissions at Raw Power Level 21 (CW tone) on page 13. Lowering the raw power level until all requirements are met yields level 21, as seen in the following table.

Table 3.3. Worst Case Radiated Harmonic Emissions at Raw Power Level 21 (CW tone)

Frequency	Measured maximums in EIRP [dBm]	Orientation and frequency of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP at max. [dBm]
Fund.	11.6	XY/V, 2402 MHz	18.4	30.0
2nd harm.	-48.7	XY/V, 2450 MHz	7.5	-41.2
3rd harm.	-41.7	XZ/V, 2480 MHz	0.4	-41.2
4th harm.	-57.5	YZ/H, 2480 MHz	48.2	-9.3
5th harm.	-51.4	XZ/H, 2480 MHz	10.2	-41.2
6th harm.	-48.2	XY/V, 2480 MHz	38.9	-9.3

If more output power is required, tuning the matching network elements could raise the possible maximum power level still meeting requirements. As Table 3.3 Worst Case Radiated Harmonic Emissions at Raw Power Level 21 (CW tone) on page 13 shows, the third harmonic is high, however, since the measurements were performed with a CW tone, an extra margin can be added to the limiting harmonics, depending on the used modulation. See the modulation relaxation values determined for EFR32MG24 in the BRD4188B Reference Manual. The values for SiMG301 can be considered similar.

These tables contain the measured levels among the three frequencies (2402, 2450, and 2480 MHz), compiling the lowest margin for every harmonic. More detailed results are available in the Appendix under 4.2 Complete TX Measurement Results for Maximum Power Level and 4.3 Complete TX Measurement Results for Raw Power Level 21, where each of these frequencies have their own table, for power levels 95 and 21, respectively.

3.2.3 Conducted TX Power

To measure the output power, the antenna pad was replaced with a u.FL connector.

Different raw power levels were used to evaluate the design. These were the following:

1. **95** – maximum possible output power
2. **21** – level at which the design passed radiated harmonic measurements (with the initial matching network)
3. **37** – where the nominal output power of 10 dBm is observed at the center frequency

Table 3.4. Conducted Harmonic Emissions at Given Power Levels (CW tone)

Raw Power Level	Fundamental	Measured Power at Nth Harmonic [dBm]						
		1st	2nd	3rd	4th	5th	6th	7th
95 (max)	2402 MHz	11.8	-37.9	-39.2	-69.0	-43.8	-68.3	-61.7
	2450 MHz	11.8	-38.0	-39.6	-69.5	-47.6	-71.0	-70.5
	2480 MHz	11.8	-38.0	-38.2	-69.0	-44.8	-70.5	-81.0
21	2402 MHz	8.2	-35.3	-56.9	-67.5	-53.0	-68.0	-80.0
	2450 MHz	8.2	-36.0	-57.3	-68.5	-57.3	-71.0	<-85*
	2480 MHz	8.1	-36.3	-56.2	-68.7	-54.8	-72.0	<-90*
37	2450 MHz	10.1	-40.5	-48.3	-68.1	-56.7	-72.0	-82.0

Note: *: Following noise of the spectrum analyzer.

The power level of 21 (raw) is the limit at which the filtering of the matching network still suppresses the radiated harmonics below regulatory limits. At this setting, the measured conducted output power on the fundamental is 8.2 dBm at the band center. This falls short of the value rating of the +10 dBm PA, however, due to the high gain antenna, the maximum direction EIRP reaches that value (as seen in Table 3.3 Worst Case Radiated Harmonic Emissions at Raw Power Level 21 (CW tone) on page 13). Further tuning is required if achieving maximum conducted output power is critical.

3.2.4 Conducted RX measurements and RX regulatory compliance (ETSI)

Measurement conditions:

- Powered by WSTK main board, not the onboard HV power supply
- Radio control via RAIL, maximum power setting
- M2 screws inserted to connect aluminum plane to GND
- Instrument settings: 100 kHz RBW
- Measured frequencies:
  - 2450 MHz: no amplification
  - 4900 MHz and 7350 MHz: through an amplifier chain

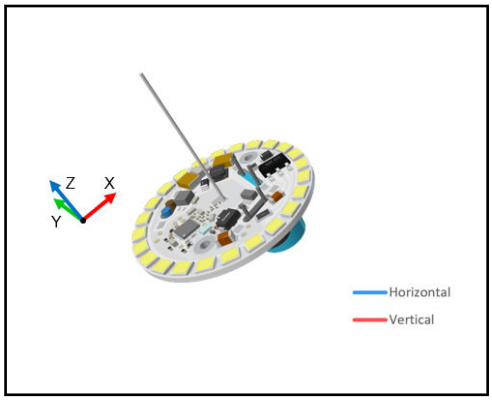
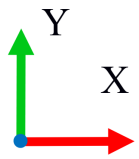
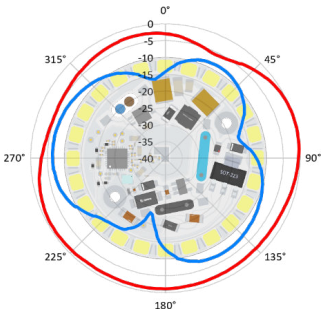
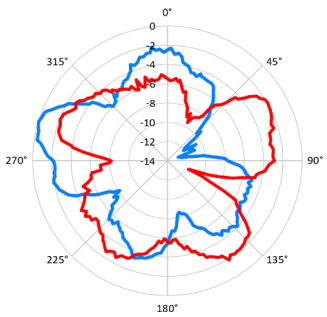
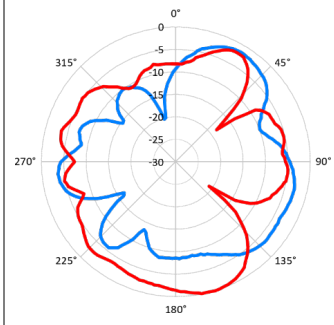
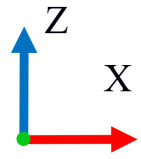
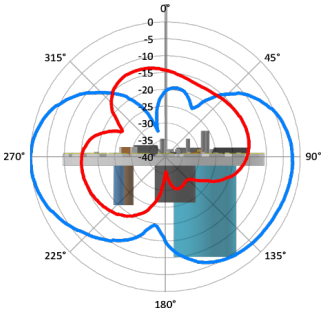
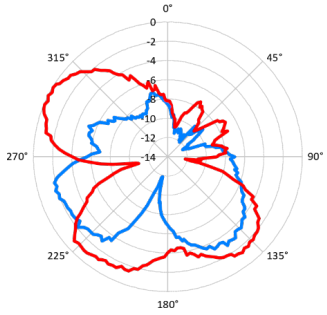
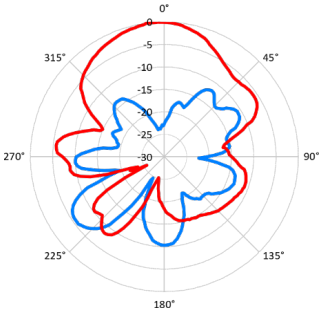
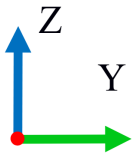
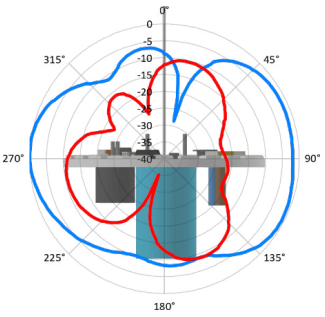
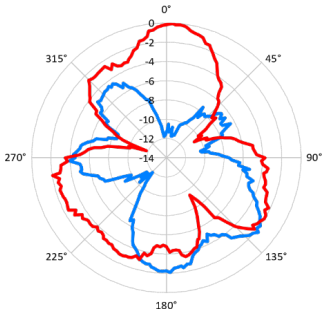
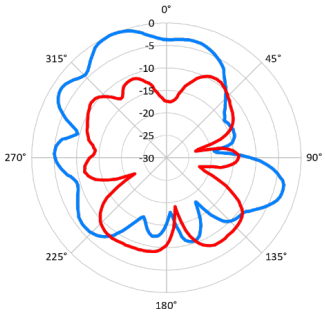


Table 3.5. Radiation pattern at given cuts and frequencies

Cut	2450 MHz	4900 MHz	7350 MHz
			
			
			

For easier visualization, each of the cuts have their respective orientation of the 3D model attached. All the traces are normalized to their local plot maximum. To get an absolute radiated pattern, use the EIRP results from 3.2.2 Radiated TX Power to denormalize them.

These radiation patterns can be used as a guide to measure the device only in the maximum direction to avoid having to do a full sweep for quick adjustments in the matching network for example. Tuning for better suppression, especially at the third harmonic can be done more effectively this way.

3.2.5 Conducted RX Sensitivity

Measurement conditions:

- RF shielded box
- 10 dB attenuator (to reduce noise figure)
- 2FSK, BLE (1 Mbps)
- u.FL connector instead of antenna pad

The datasheet sensitivity value for 1 Mbps GFSK is -98.6 dBm. Since the values below were measured using binary FSK modulation, slight differences might have occurred. Hence, the BRD4407 Radio Board was also measured in the same setup for reference.

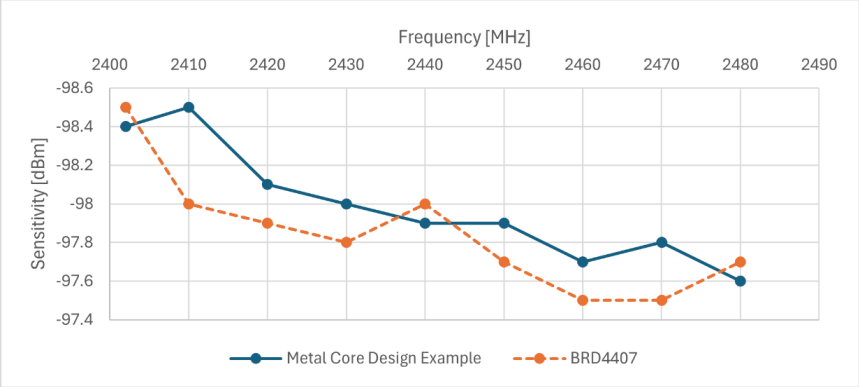


Figure 3.5. Receiver sensitivity results

Overall, as shown in the Figure 3.5 Receiver sensitivity results on page 16, the metal core design performed comparably, even slightly better than the Radio Board.

4. Appendix

4.1 Reference Design Schematics and PCB design

All design files will be included in the BRD4407A design package.

4.2 Complete TX Measurement Results for Maximum Power Level

Table 4.1. Radiated Harmonic Emissions at Raw Power Level 95 (Max) at 2402 MHz

2402 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	15.2	XY/V	14.8	30.0
2nd harm.	-46.5	YZ/V	5.2	-41.2
3rd harm.	-27.9	YZ/H	23.1	-4.8
4th harm.	-59.1	YZ/H	54.3	-4.8
5th harm.	-46.4	YZ/H	5.1	-41.2
6th harm.	-54.1	YZ/V	49.3	-4.8

Table 4.2. Radiated Harmonic Emissions at Raw Power Level 95 (Max) at 2450 MHz

2450 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	16.5	XY/V	13.5	30.0
2nd harm.	-46.5	XY/H	5.3	-41.2
3rd harm.	-26.8	YZ/H	-14.5	-41.2
4th harm.	-57.6	XY/V	54.1	-3.5
5th harm.	-43.0	YZ/H	1.7	-41.2
6th harm.	-49.4	YZ/H	45.9	-3.5

Table 4.3. Radiated Harmonic Emissions at Raw Power Level 95 (Max) at 2480 MHz

2480 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	16.2	XY/V	13.8	30.0
2nd harm.	-46.3	XY/H	5.1	-41.2
3rd harm.	-25.2	YZ/H	-16.0	-41.2
4th harm.	-56.4	XY/V	52.6	-3.8
5th harm.	-42.2	YZ/H	1.0	-41.2
6th harm.	-47.6	YZ/H	43.8	-3.8

4.3 Complete TX Measurement Results for Raw Power Level 21

Table 4.4. Radiated Harmonic Emissions at Raw Power Level 21 at 2402 MHz

2402 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	11.6	XY/V	18.4	30.0
2nd harm.	-49.4	XY/V	8.1	-41.2
3rd harm.	-45.2	XZ/V	36.8	-8.4
4th harm.	-60.0	YZ/H	51.6	-8.4
5th harm.	-52.7	XZ/V	11.5	-41.2
6th harm.	-53.7	YZ/V	45.3	-8.4

Table 4.5. Radiated Harmonic Emissions at Raw Power Level 21 at 2450 MHz

2450 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	10.4	XY/V	19.6	30.0
2nd harm.	-48.7	XY/V	7.5	-41.2
3rd harm.	-43.0	YZ/H	1.8	-41.2
4th harm.	-58.5	XY/V	49.0	-9.6
5th harm.	-51.6	XZ/H	10.3	-41.2
6th harm.	-50.1	YZ/V	40.6	-9.6

Table 4.6. Radiated Harmonic Emissions at Raw Power Level 21 at 2480 MHz

2450 MHz	Measured maximums in EIRP [dBm]	Orientation of the maximum	Margin [dB]	FCC_15.247_ limit in EIRP [dBm]
Fund.	10.7	XY/V	19.3	30.0
2nd harm.	-49.8	XY/V	8.6	-41.2
3rd harm.	-41.7	XZ/V	0.4	-41.2
4th harm.	-57.5	YZ/H	48.2	-9.3
5th harm.	-51.4	XZ/H	10.2	-41.2
6th harm.	-48.2	XY/V	38.9	-9.3

5. Revision History

Revision 0.1

September, 2025

Initial release.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support & Community
www.silabs.com/community

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com