AN1520: SiXG30x Hardware Design Considerations

This application note details hardware design considerations for SiXG30x devices. For Series 2 EFM32 and EFR32 Wireless Gecko devices, refer to AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations.

Topics specifically covered are supported power supply configurations, supply filtering considerations, debug interface connections, and external clock sources.

For more information on hardware design considerations for the radio portion of SiXG30x devices, see AN930.3: Series 3 2.4 GHz Matching Guide, AN933.3: Series 3 Minimal BOM, and AN928.3: Series 3 Layout Design Guide.

KEY POINTS

- Decoupling capacitors are crucial to ensuring the integrity of the device's power supplies.
- Different connectors can be used for the Serial Wire Debug (SWD) interface depending on board and tool requirements.
- External clock sources must be connected to the device correctly for proper operation.

1. Device Compatibility

This application note supports multiple device families. Some functionality is different depending on the device.

SiXG30x family members include:

- SiBG301
- SiMG301

2. Power Supply Overview

2.1 Introduction

Although the SiXG30x devices have very low average current consumption, proper decoupling is crucial. As for all digital circuits, current is drawn in short pulses corresponding to the clock edges. Particularly when several I/O lines are switching simultaneously, transient current pulses on the power supply can be on the order of several hundred mA for a few nanoseconds, even though the average current consumption is quite small.

These transient currents cannot be properly delivered over high-impedance power supply lines without introducing considerable noise in the supply voltage. To reduce this noise, decoupling capacitors are employed to supplement the current during these short transients.

2.2 Decoupling Capacitors

Decoupling capacitors make the current loop between supply, MCU, and ground as short as possible for high-frequency transients. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pins, ground pins, and PCB (Printed Circuit Board) ground planes.

All external decoupling capacitors should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 to +85 °C (standard temperature range devices) or -55 to +125 °C (extended temperature range devices).

For any capacitor connected to a regulator output (DECOUPLE is a primary example), the system designer must pay careful attention to the characteristics of the capacitor over temperature and bias voltage. Some capacitors — particularly those in smaller packages or that may use cheaper dielectrics — can experience a dramatic reduction in capacitance across temperature or as the DC bias voltage increases. Violation of data sheet specified capacitance limits can cause supply instability.

2.3 Power Supply Requirements

An important consideration for all devices is understanding their voltage requirements and the dependencies between power-supply pins. System designers must ensure that these power supply requirements are met, regardless of power configuration or topology. The relationships between the voltages applied to the various SiXG30x supply pins are defined below. Failure to observe these constraints can result in damage to the device and/or increased current draw. Refer to the device data sheet for absolute maximum ratings and additional parameters governing voltage supplies.

- AVDD — No dependency on any other supply pin.
- IOVDD — No dependency on any other supply pin.
- DVDD ≥ DECOUPLE

For devices with in-package or external flash, the following restrictions apply to DVDD (MCU logic supply) and FVDD (flash regulator output/supply):

- DVDD ≥ FVDD
  - DVDD must adhere to the input supply requirements of the flash regulator when used to power FVDD.
  - When an external supply powers FVDD, it must be tied to DVDD.

Supply inputs for the low-power wireless (LPW) subsystem are handled as follows:

- PAVDD ≥ RFVDD

  Note: When using a SiXG30x device in an applications where the radio is never used, connect its supply and I/O pins as follows:
  - PAVDD = RFVDD = DVDD
  - RF2G4_IO = NC

Energy use and the functionality of certain peripherals can be impacted by power supply configuration. For example, inputs to mixed-signal peripherals, such as the Analog-to-Digital Converter (ADC) cannot exceed the minimum of the AVDD and IOVDD supply voltages. Similarly, increased leakage can occur if DVDD is not within its valid operating range while AVDD and IOVDD are fully powered.

Power Supply Pin Overview

The table below provides an overview of available power supply pins. Some pins may not be present on certain devices depending on the feature set.

Table 2.1. Power Supply Pin Overview

Pin Name	Description
AVDD	Supply to analog peripherals
DECOUPLE	Output of the internal digital LDO
DVDD	Input to the internal digital LDO
IOVDD	GPIO supply
FVDD	Flash LDO output and interface supply
PAVDD	Radio power amplifier supply
RFVDD	Supply to radio analog (and HFXO on LPW-enabled devices)

2.4 DVDD and DECOUPLE

All SiXG30x devices include an internal linear regulator that powers the core digital logic. The DECOUPLE pin is the output of the digital LDO and requires a 1 µF capacitor. For better high-frequency noise suppression, a 0.1 µF capacitor can be placed in parallel with the 1 µF capacitor on the DECOUPLE pin.

As mentioned in 2.2 Decoupling Capacitors, care should be taken in the selection of regulator output decoupling capacitors, such as for DECOUPLE, to ensure that changes in system temperature and bias voltage do not cause capacitance changes that fall outside of the data sheet specified limits and which could destabilize the regulator output.

On SiXG30x devices, the input supply to the digital LDO is the DVDD pin and the DECOUPLE pin is the output of the LDO. Decoupling of DVDD should include a bulk capacitor of C_{DVDD} and this bulk capacitor should be at least 10 µF. For better high-frequency noise suppression, a 0.1 µF capacitor (C_{DVDD1}) can be placed in parallel with the C_{DVDD} capacitor on the DVDD pin.

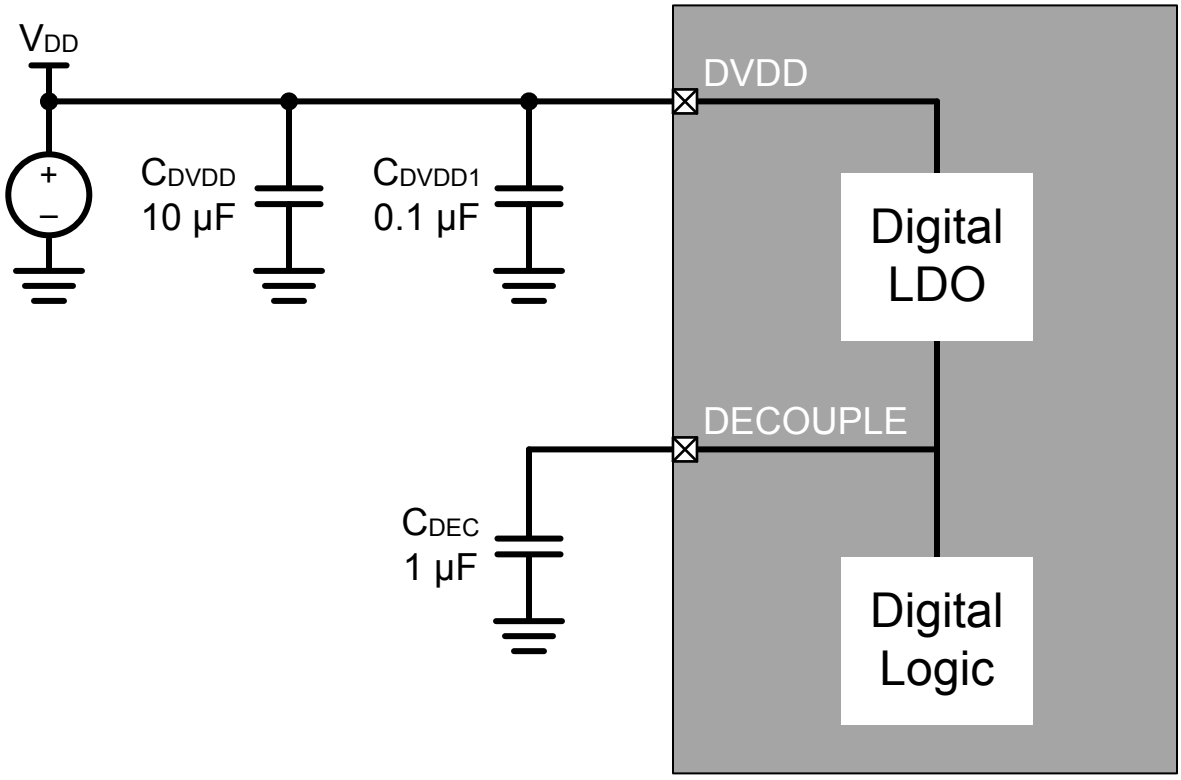

Figure 2.1. DVDD and DECOUPLE

Note: The DECOUPLE pin cannot be used to power any external circuitry. Although DECOUPLE is connected to the output of the internal digital LDO, it is provided solely for the purpose of decoupling this supply and is not intended to power anything other than the internal digital logic of the device.

2.5 AVDD

The analog peripheral performance of the device is impacted by the quality of the AVDD power supply. For applications with less demanding analog performance, a simpler decoupling scheme for AVDD may be acceptable. For applications requiring the highest quality analog performance, more robust decoupling and filtering is required.

Note: The number of AVDD analog power pins may vary by device and package.

2.5.1 AVDD Standard Decoupling

The figure below illustrates a standard approach for decoupling the AVDD pin(s). In general, one 1 µF bulk capacitor (C_{AVDD}), as well as one 0.1 µF capacitor for each AVDD pin (C_{AVDD_0} through C_{AVDD_n}), must be provided.

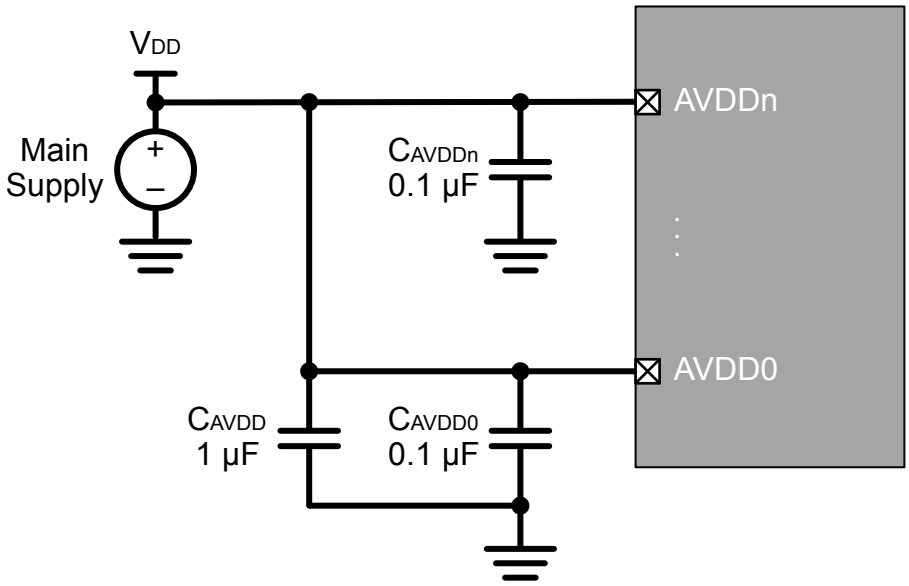

Figure 2.2. AVDD Standard Decoupling

2.5.2 AVDD Improved Decoupling

The figure below illustrates an improved approach for decoupling and filtering the AVDD pin(s). In general, one 1 µF bulk capacitor (C_{AVDD}), as well as one 0.1 µF capacitor for each AVDD pin (C_{AVDD_0} through C_{AVDD_n}), must be provided. In addition, a ferrite bead and series 1 Ω resistor provide additional power supply filtering and isolation and are preferred when higher ADC accuracy is required.

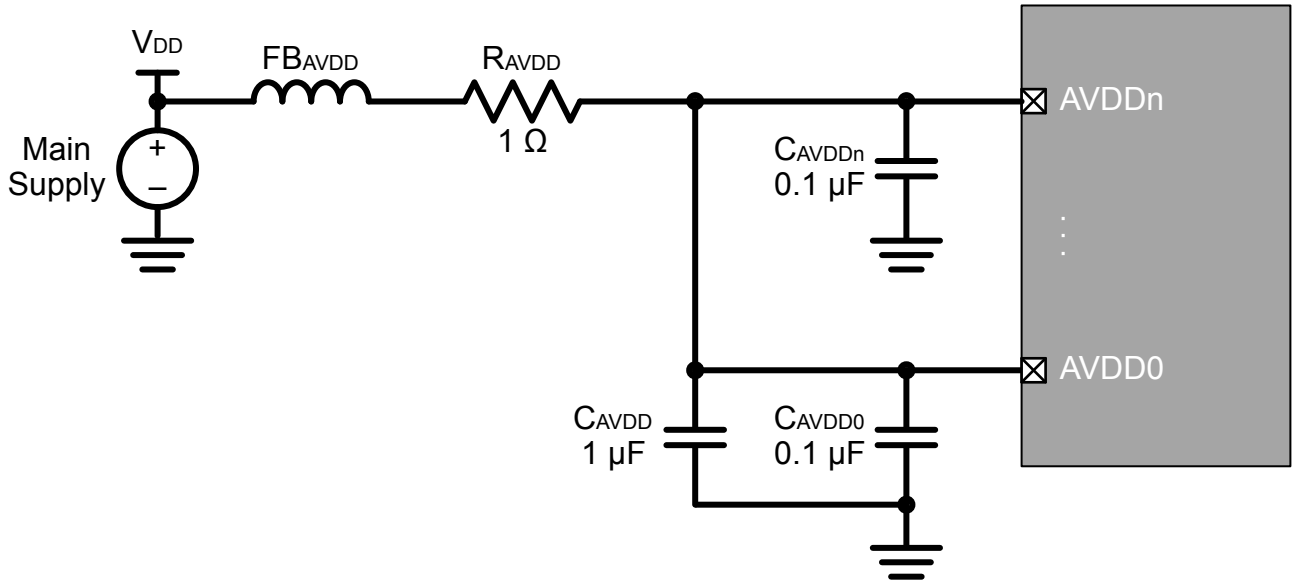

Figure 2.3. AVDD Improved Decoupling

The following table lists some recommended ferrite bead part numbers suitable for AVDD filtering.

Table 2.2. Recommended Ferrite Beads

Manufacturer	Part Number	Impedance	I_{MAX} (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Würth Electronics	74279266	1 kΩ @ 100 MHz	200	0.600	-55 to +125	0603/1608
Würth Electronics	742692004	240 Ω @ 100 MHz	200	0.750	-55 to +125	0201/0603
Murata	BLM21BD102SN1D	1 kΩ @ 100 MHz	200	0.400	-55 to +125	0805/2012

2.6 IOVDD

The IOVDD pin(s) provide decoupling for all of the GPIO pins on the device. For proper decoupling when powering IOVDD from the main supply, include a 0.1 µF capacitor per IOVDD pin, along with a 1 µF bulk capacitor. Increase the bulk capacitor value in applications using GPIO to drive heavy and dynamic loads.

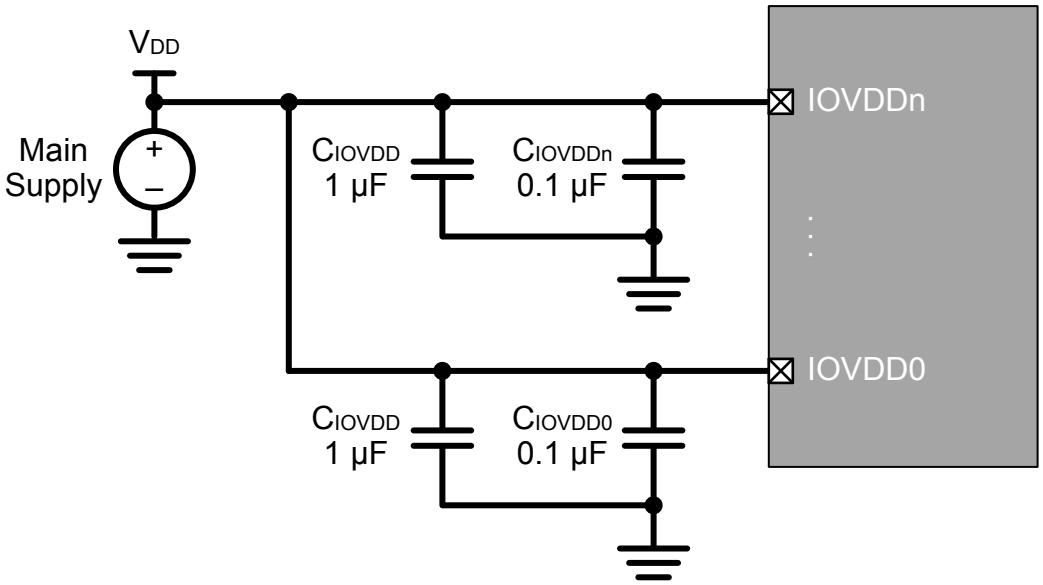

Figure 2.4. IOVDD Decoupling

2.7 FVDD Decoupling

FVDD is the 1.8 V supply for devices with co-packaged or external flash memory and the dedicated I/O interface to this memory. When a system-wide supply of at least 1.9 V is available, FVDD is typically provided by the flash regulator (FLREG), an on-chip LDO powered by DVDD. When a 1.8 V supply is available, such as in systems running from a single 1.8 V supply, FVDD can be powered from this supply and the FLREG can be disabled.

Regardless of whether or not the FLREG is used, FVDD must be decoupled with 1 µF and 0.1 µF capacitors, such as those used for the primary AVDD supply pin. In systems where DVDD is nominally 1.8 V, FVDD must be tied to DVDD, the FLREG must be disabled, and DVDD and FVDD each must be decoupled as specified.

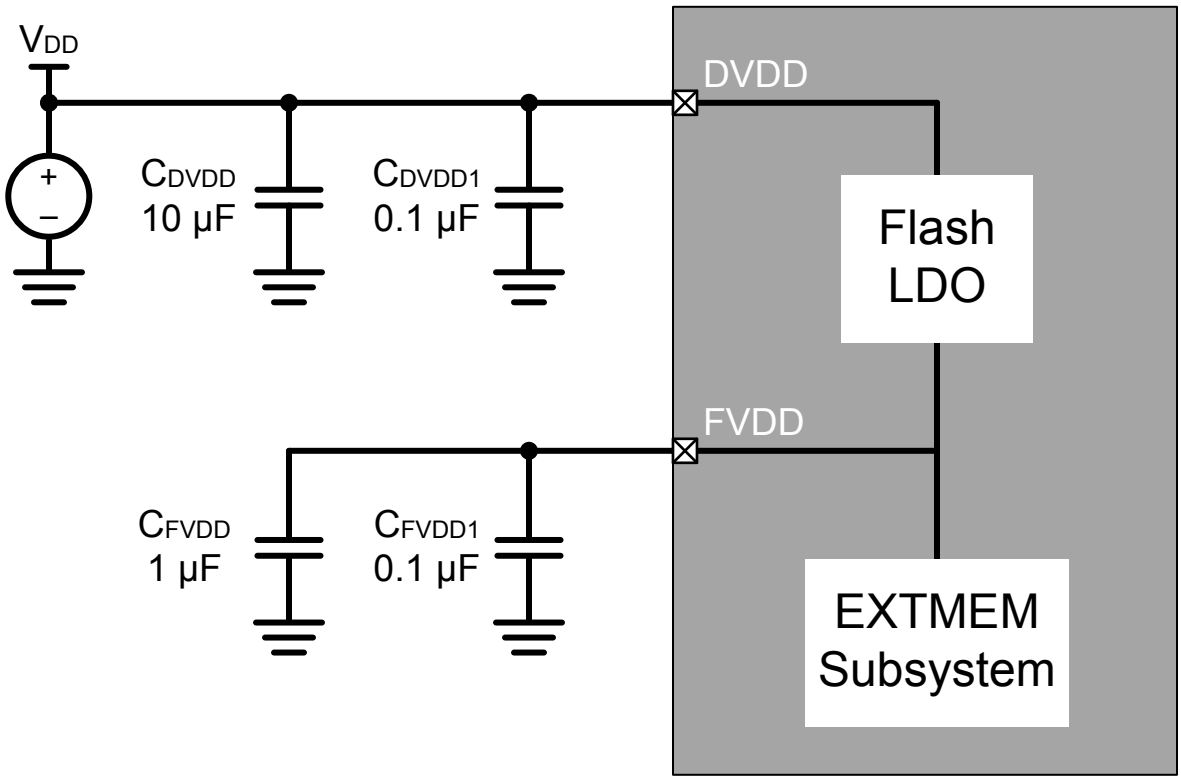

Figure 2.5. FVDD Decoupling

2.8 Radio (RFVDD & PAVDD)

On all SiXG30x devices, the PAVDD ≥ RFVDD relationship listed in 2.3 Power Supply Requirements is necessary for proper operation. Lower current is possible when RFVDD can be run at a lower voltage than PAVDD. For example, if DVDD is powered from a 1.8 V supply, RFVDD can also be powered from this supply with no loss of functionality.

2.8.1 RFVDD and PAVDD — Powered from Main Supply

PAVDD and RFVDD can be powered directly from the main supply on SiXG30x devices. The component values for each device can be found in 2.8.2 RFVDD and PAVDD — Decoupling Component Values.

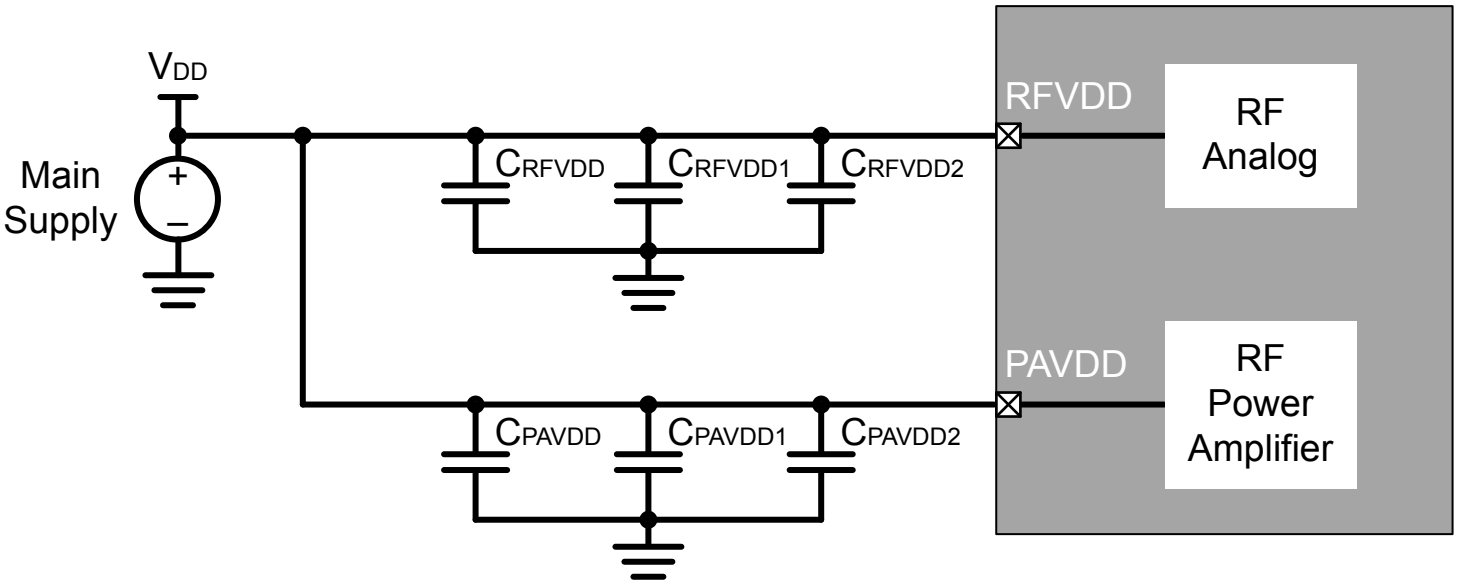

Figure 2.6. RFVDD and PAVDD Decoupling (2.4 GHz Application, Both Powered from Main Supply)

2.8.2 RFVDD and PAVDD — Decoupling Component Values

The component values used to decouple the PAVDD and RFVDD supplies on SiXG30x devices vary depending on the transmit power level and the frequency band in which the radio is intended to operate. The component values listed in Table 2.3 RFVDD and PAVDD Decoupling Values on page 9 are those used during characterization and correspond to the data sheet specifications for a given device.

Table 2.3. RFVDD and PAVDD Decoupling Values

Device	Application	C_{RFVDD}	C_{RFVDD1}	C_{RFVDD2}	C_{PAVDD}	C_{PAVDD1}	C_{PAVDD2}
SiXG301	2.4 GHz	1 µF	120 pF	0.3 pF	1 µF	120 pF	0.3 pF

3. Example Power Supply Configurations

3.1 Standard Decoupling Example

The following figure illustrates a standard decoupling approach for a SiXG30x device that includes co-packaged flash and that is intended for 2.4 GHz radio operation. RFVDD and PAVDD component values for a given device can be found in 2.8.2 RFVDD and PAVDD — Decoupling Component Values.

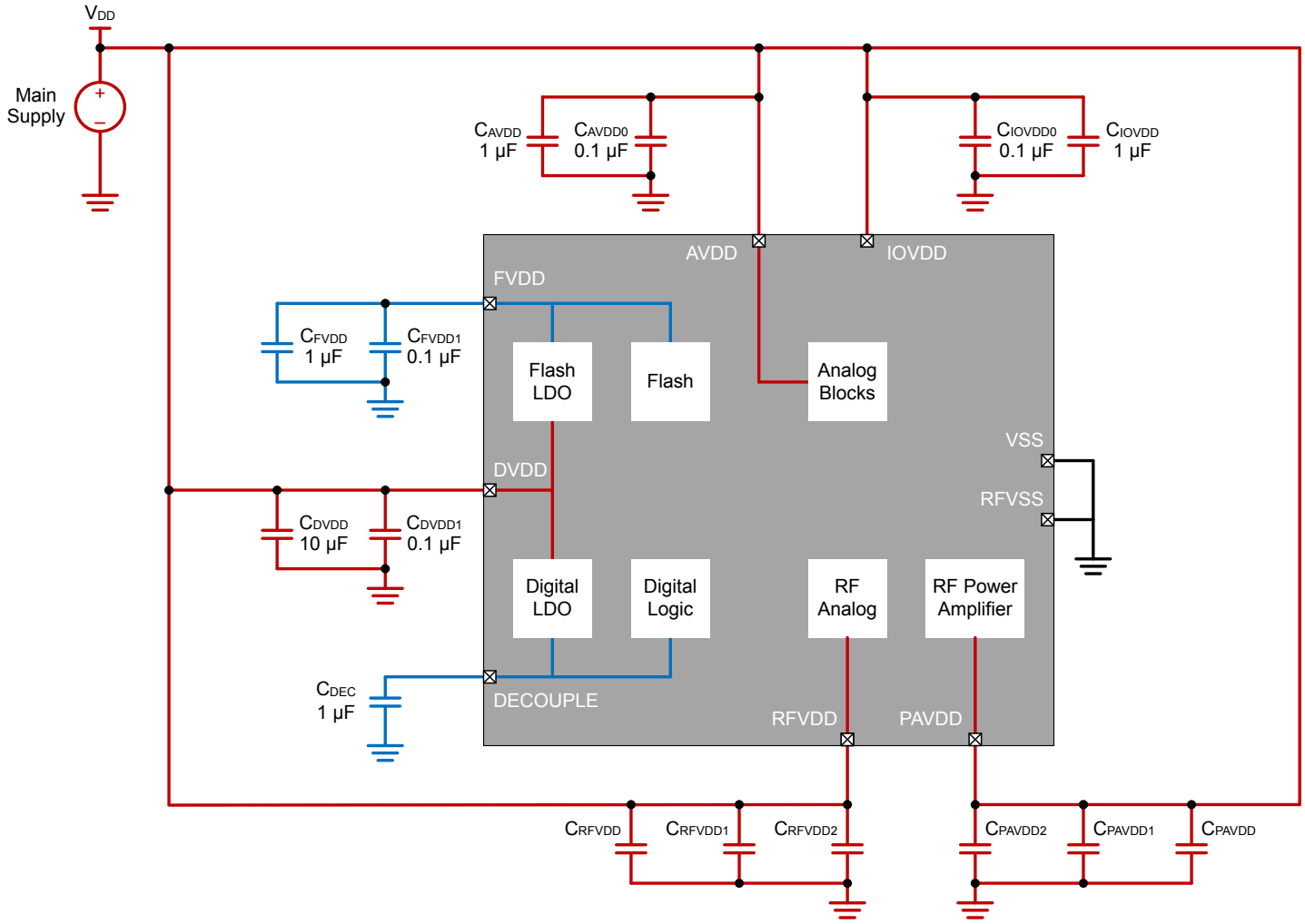

Figure 3.1. 2.4 GHz Standard Decoupling Example

3.2 Improved Decoupling Example

The following figure illustrates an improved decoupling approach that provides better noise suppression and isolation between the digital and analog power pins using a ferrite bead and a resistor. This configuration is preferred when higher ADC accuracy is required. Suitable ferrite bead options are listed in Table 2.2 Recommended Ferrite Beads on page 7. RFVDD and PAVDD component values for a given device can be found in 2.8.2 RFVDD and PAVDD — Decoupling Component Values.

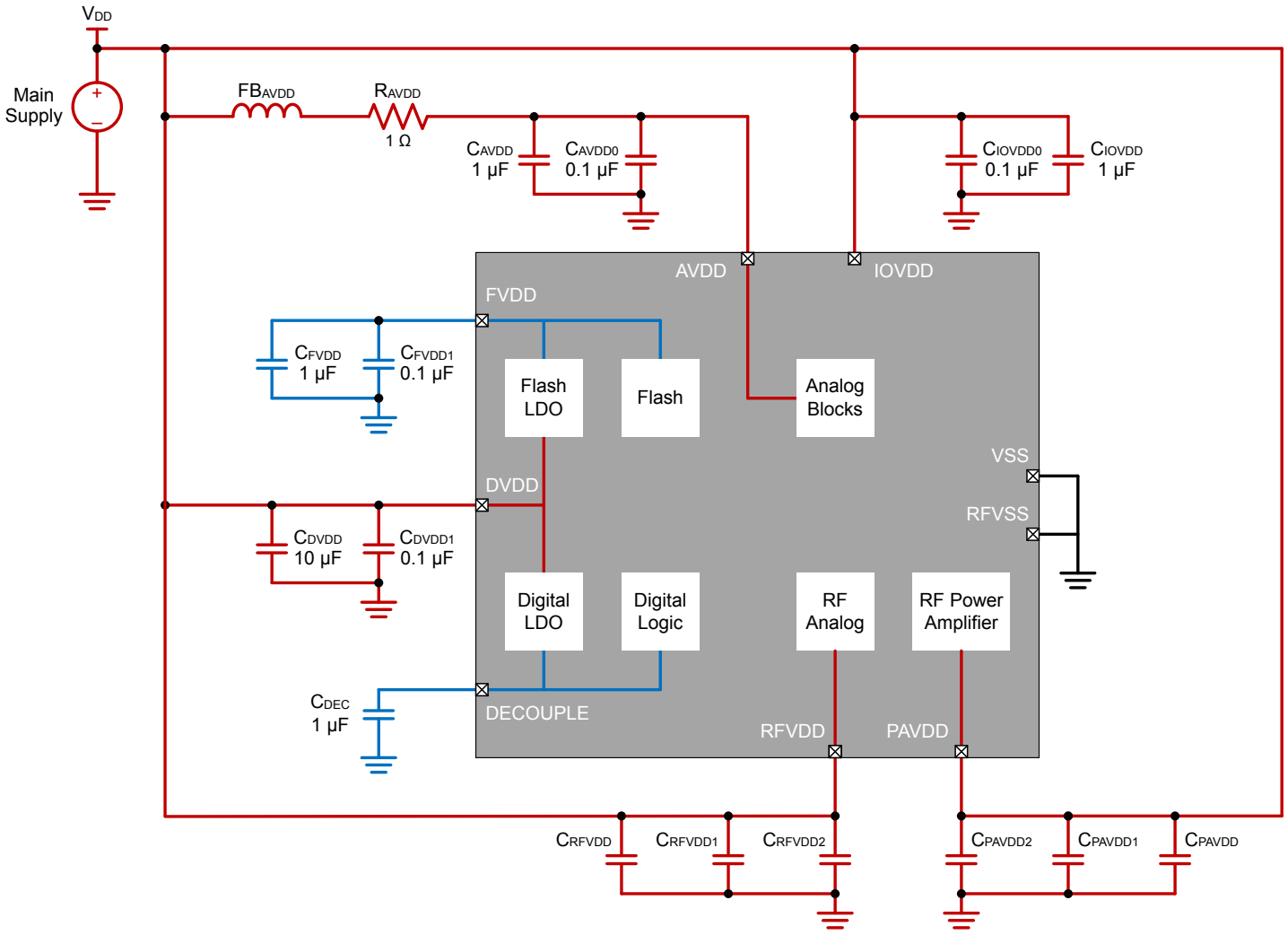

Figure 3.2. 2.4 GHz Improved Decoupling Example

4. Debug Interface and External Reset Pin

4.1 Serial Wire Debug

The Serial Wire Debug (SWD) interface is supported by all SiXG30x devices and requires the SWCLK (clock input) and SWDIO (data in/out) pins. The optional SWV (serial wire viewer) line is used for instrumentation trace and program counter sampling, and is not needed for flash programming and normal debugging. However, it can be valuable in advanced debugging scenarios, and designers are strongly encouraged to include it along with the other SWD signals.

Arm® defines two standard debug connectors depending on the level of functionality required. The 10-pin Cortex® Debug Connector has the smaller footprint of the two. In addition to standard functionality, such as execution control and memory read/write access, software tools can provide data from console debug prints and program counter sampling. Simplicity Studio's Energy Profiler uses this data when the processor SWV pin is connected.

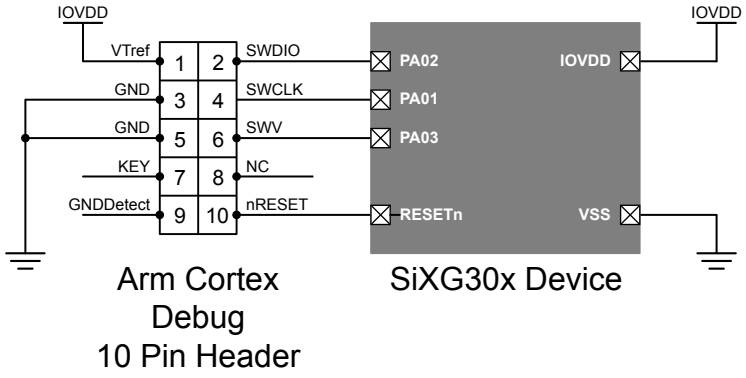

Figure 4.1. Arm Cortex Debug Connector

Note:

- VTref does not supply power. It is used as a reference voltage for debug level translators and must be connected to IOVDD.
- KEY is used to ensure proper connector alignment and is typically not present on the board debug connector and blocked on the receiving pin of the matching ribbon cable. It otherwise has no connection in the system.
- GNDDetect is grounded by the debug probe and allows a target system to detect connection of the debugger. On a development board, for example, this can be used to isolate or otherwise multiplex signals that may be shared for debug purposes. Unless this functionality is needed in a system, GNDDetect can be left disconnected.

In systems where at-speed trace is required, the 20-pin Cortex Debug+ETM Connector can be used. It simply adds pins 11 - 20 for TRACECLK, TRACEDATA[3:0], and additional grounds to the 10-pin Cortex Debug connector.

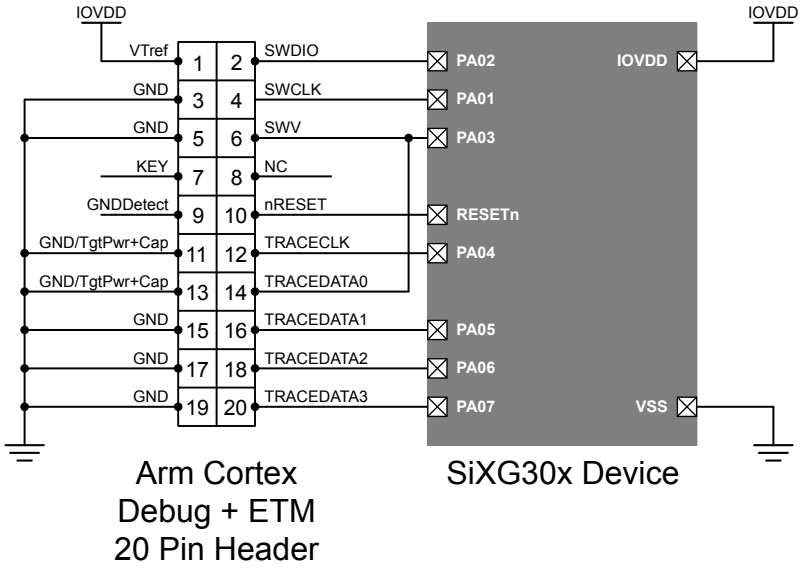

Figure 4.2. Arm Cortex Debug+ETM Connector

Note: Along with VTref, KEY, and GNDDetect, the following considerations apply when using the 20-pin trace connector:

- SWV and TRACEDATA0 are both multiplexed on pin PA03 and thus cannot be used simultaneously.
- Arm permits user-defined functionality on pins 6 and 8 of the 20-pin connector, discussion of which is beyond the scope of this document and generally not supported by Silicon Labs and third-party tools.
- Pins 11 and 13 should be grounded in most systems. Arm has defined optional functionality whereby these pins can deliver power to an appropriatelty designed target, typically a development tool. Not all debug tools support this, but, in cases where it can be used, each pin must be decoupled with a 10 nF capacitor at the connector.

Tool infrastructure and availability has a sizable influence on which debug connector to place in a design. Simply because it is still used by many debug probes, consideration may also need to be given to Arm's legacy JTAG connector.

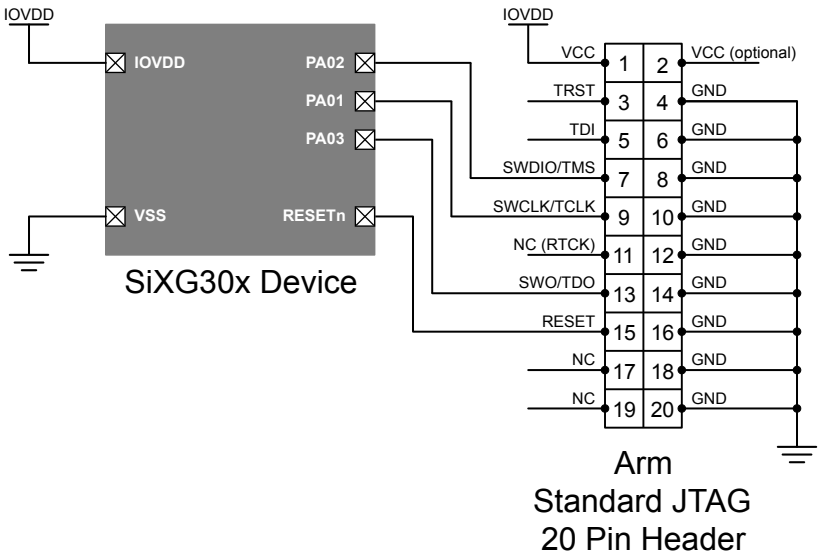

Figure 4.3. Arm Standard JTAG Connector with SWD

Note: VCC does not supply power. It is used as a reference voltage for debug level translators and must be connected to IOVDD.

For further discussion of debug and programming interfaces, see Application Note AN958: Debugging and Programming Interfaces for Custom Designs.

4.2 JTAG Debug

SiXG30x devices optionally support JTAG for debug using the TCK (clock), TDI (data input), TDO (data output), and TMS (test mode select) lines.

- TCK is the JTAG interface clock.
- TDI carries input data and is sampled on the rising edge of TCK.
- TDO carries output data and is shifted out on the falling edge of TCK.
- TMS is the test mode select signal and is used to navigate through the Test Access Port (TAP) state machine.

Note: The JTAG implementation on SiXG30x devices does not support boundary scan. It can operate in pass-through mode and participate in a chain with other devices that do implement JTAG for firmware programming or boundary scan purposes.

The connection to Arm's legacy JTAG 20-pin debug connector is shown below. Pins with no connection should be left unconnected.

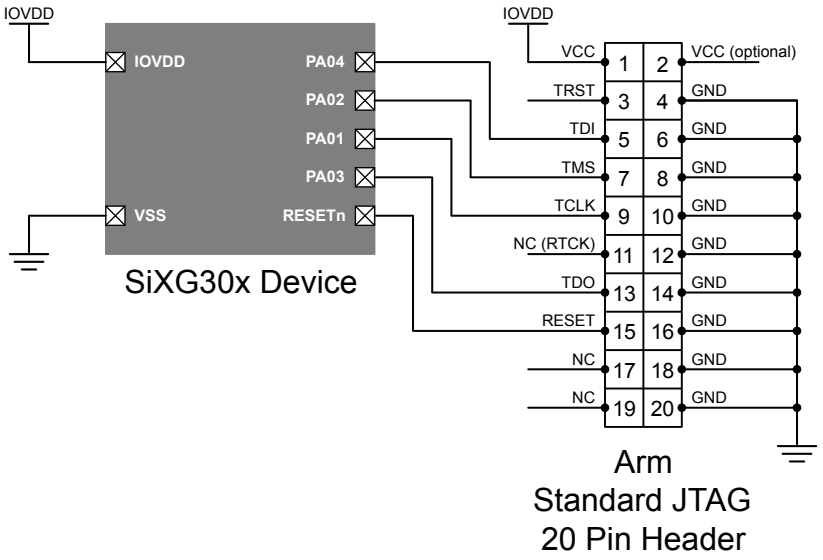

Figure 4.4. Arm Standard JTAG Connector

Note: VCC does not supply power. It is used as a reference voltage for debug level translators and must be connected to IOVDD.

For further discussion of debug and programming interfaces, see Application Note AN958: Debugging and Programming Interfaces for Custom Designs.

4.3 External Reset Pin (RESETn)

SiXG30x processors are reset by driving the RESETn pin low. A weak internal pull-up device holds the RESETn pin high, allowing it to be left unconnected if no external reset source is required. A low-pass filter connected to RESETn helps suppress noise glitches that can cause unintended resets. The characteristics of the pull-up device and input filter are identical to those present on any GPIO pin and are specified in the device data sheet.

Note:

1. The internal pull-up ensures the proper release of reset. When the device is not powered, RESETn must not be connected through an external pull-up to an active supply or otherwise driven high as this could damage the device.
2. RESETn is internally pulled to DVDD. In cases where RESETn is connected to an external signal that can drive the pin at a voltage that differs from DVDD, the internal pull up provides a path for possible current draw. Examples of this include supply voltage monitors, reset supervisors, debug probes, or other processors in system. In such cases, connect RESETn only to open drain outputs to avoid unintended current draw when not driven low.

5. External Clock Sources

5.1 Introduction

In addition to its internal high- and low-frequency RC oscillators, SiXG30x devices support different external sources for high- and low-frequency clocks. Supported clock sources include crystals and off-chip oscillators with output waveforms that meet relevant data sheet specifications. This section describes how external clock sources are connected.

For additional information on the external oscillators, refer to application note AN0016.3: Oscillator Design Considerations .

5.2 Low-Frequency Crystals

A crystal is connected as shown in the figure below across the LFXTAL_I (input) and LFXTAL_O (output) pins on SiXG30x devices.

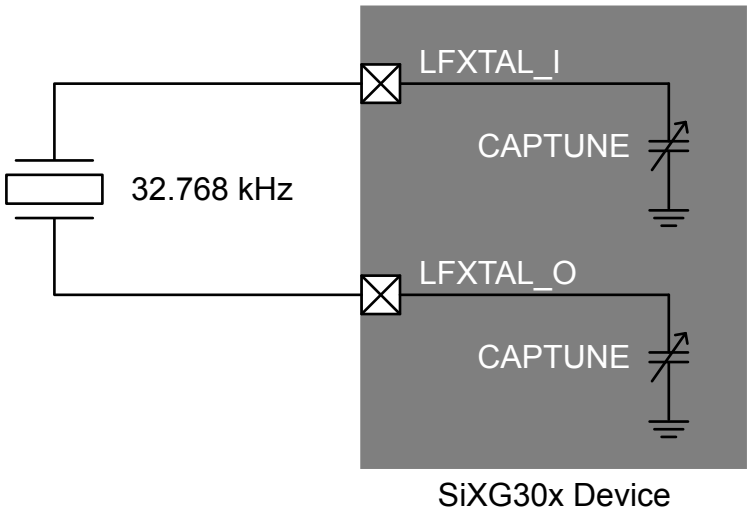

Figure 5.1. Connecting a Crystal to the LFXO

Low frequency crystals do not require external load capacitors as these are integrated on-chip and can be tuned by register bit fields under software control, thus reducing BOM cost and saving space in the PCB footprint. The Low-Frequency Crystal Oscillator (LFXO) supports 32.768 kHz crystals. Check device-specific data sheets for supported crystal load capacitance and ESR values and refer to device-specific reference manuals for on-chip load capacitor tuning instructions.

5.3 Low-Frequency External Clocks

SiXG30x devices can source a low-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal can be either a square wave or a sine wave with a frequency of 32.768 kHz. The external clock source must be connected as shown in Figure 5.2 Connecting an External Clock Source to the LFXO on page 16.

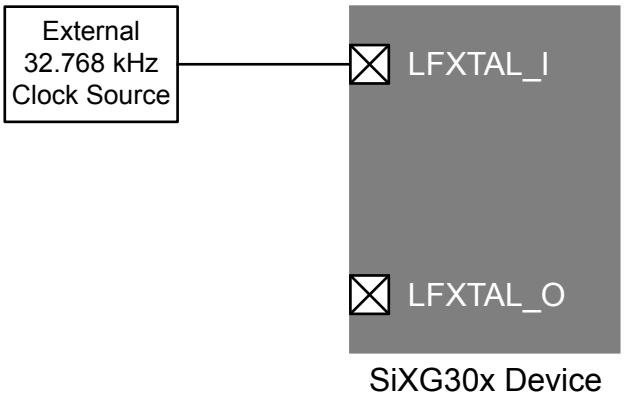

Figure 5.2. Connecting an External Clock Source to the LFXO

Bypass and buffered input modes are supported for external clock sources. A CMOS square wave that toggles between ground and the IOVDD supply voltage with a duty cycle of 50% can be used when LFXO_CFG_MODE = DIGEXTCLK, which bypasses the LFXO.

An external sine wave source (LFXO_CFG_MODE = BUFEXTCLK) having minimum and maximum amplitudes of 100 and 500 mV (0.2 and 1 V peak-to-peak), respectively, can be connected in series with the LFXTAL_I pin and is internally AC-coupled. The sine wave minimum voltage must be higher than ground and the maximum voltage less than the DVDD supply voltage.

When using either DIGEXTCLK or BUFEXTCLK mode, the LFXTAL_O pin is free to be used as a general purpose GPIO.

5.4 High-Frequency Crystals

A crystal is connected as shown in the figure below across the HFXTAL_I (input) and HFXTAL_O (output) pins on SiXG30x devices.

External load capacitors are not required and must not be used. These capacitors are integrated on-chip and can be tuned independently for the input and output pins using register bit fields under software control. This improves RF performance, saves PCB space, and reduces BOM cost. Check device-specific data sheets for the supported range of crystal frequencies, load capacitance tuning, and ESR values. In particular, specific crystal frequencies are mandatory when using on-chip radios and their associated protocol stacks; use of other values is expressly **not** supported.

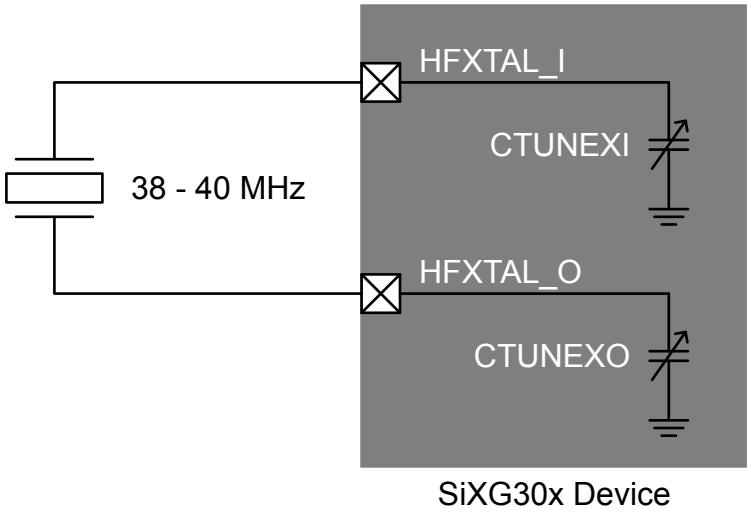

Figure 5.3. Connecting a Crystal to the HFXO

5.5 High-Frequency External Clocks

SiXG30x devices can source a high-frequency clock from an external source such as a TCXO or VCXO. To select a proper external oscillator, consider specifications such as frequency, aging, stability, voltage sensitivity, rise and fall time, duty cycle, and signal levels. The external clock signal must be a sine wave (clipped sine supported) with a frequency in accordance with the device data sheet. The external clock source must be connected as shown in Figure 5.4 High-Frequency External Clock on page 18.

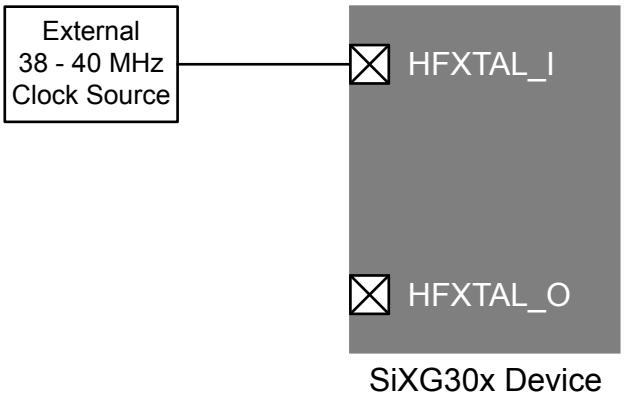

Figure 5.4. High-Frequency External Clock

Unlike the LFXO, which has specific modes for a buffered or digital external clock, the HFXO has more limited external clock input flexibility. When a crystal is not used, the external clock signal must be a sine wave (HFXO_CFG_MODE = EXTCLK) having minimum and maximum amplitudes of 275 and 525 mV (0.55 and 1.05 V peak-to-peak), respectively.

Excursions of the sine wave must not cross below ground or exceed a maximum input level of 1.05 V. The external clock must be connected in series with the HFXTAL_I pin and can be either AC- or DC-coupled. When AC coupling is used, the HFXO_CFG_ENXIDCBIASANA bit must be set. This enables a fixed internal DC bias of 410 mV on the HFXTAL_I pin so that the amplitude of the input sine wave can be managed with the series coupling capacitor.

6. Revision History

Revision 0.1

December, 2025

- Initial revision.

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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