AN781: Alternative Output Termination for Si5211x, Si5213x, Si5214x, Si5216x, Si522xx, Si5310x, Si5311x, and Si5315x PCIe Clock Generator and Buffer Families

This application note is intended to provide optional, alternative output terminations for converting a low-power HCSL output clock from a Silicon Labs PCIe clock generator or buffer device into a LVPECL, LVDS, or CML formatted clock. These optional terminations are particularly useful in applications that require both 100 MHz PCIe output clocks, as well as 100 MHz LVDS, LVPECL, or CML output clocks for FPGAs, SGMII, or other chipsets. Rather than using separate clock generators or oscillators to satisfy these system requirements, one can utilize a single-clock generator or buffer IC from Silicon Labs and employ different terminations on each output to achieve the desired results. It is relevant to note all Silicon Labs devices that provide HCSL PCIe outputs utilize low-power, push-pull buffers as opposed to constant current mode buffers. There are many advantages to using low-power, push-pull output buffers, including lower power consumption, elimination of external termination resistors, and overall reduction in total PCB area.

KEY FEATURES OR KEY POINTS

- Translate HCSL to LVPECL, LVDS or CML levels
- Reduce Power Consumption
- Simplify BOM AVL

1. Conversion of HCSL Signals to LVPECL Signals

A low-power, push-pull HCSL output clock can be converted to either 2.5 V or 3.3 V LVPECL standards by using an output termination as shown in Figure 1.1 Termination Scheme for HCSL to LVPECL Conversion on page 2. Figure 1.2 Oscilloscope Measurement of LVPECL Conversion on page 2 shows the output clock at the measurement point indicated in Figure 1.1 Termination Scheme for HCSL to LVPECL Conversion on page 2. VCC supply is required to set the common mode voltage at the receiver end. Table 1.1 Resistor Selection for Different VCC Standards (LVPECL Signal Conversion) on page 3 lists the resistor selection based on VCC.

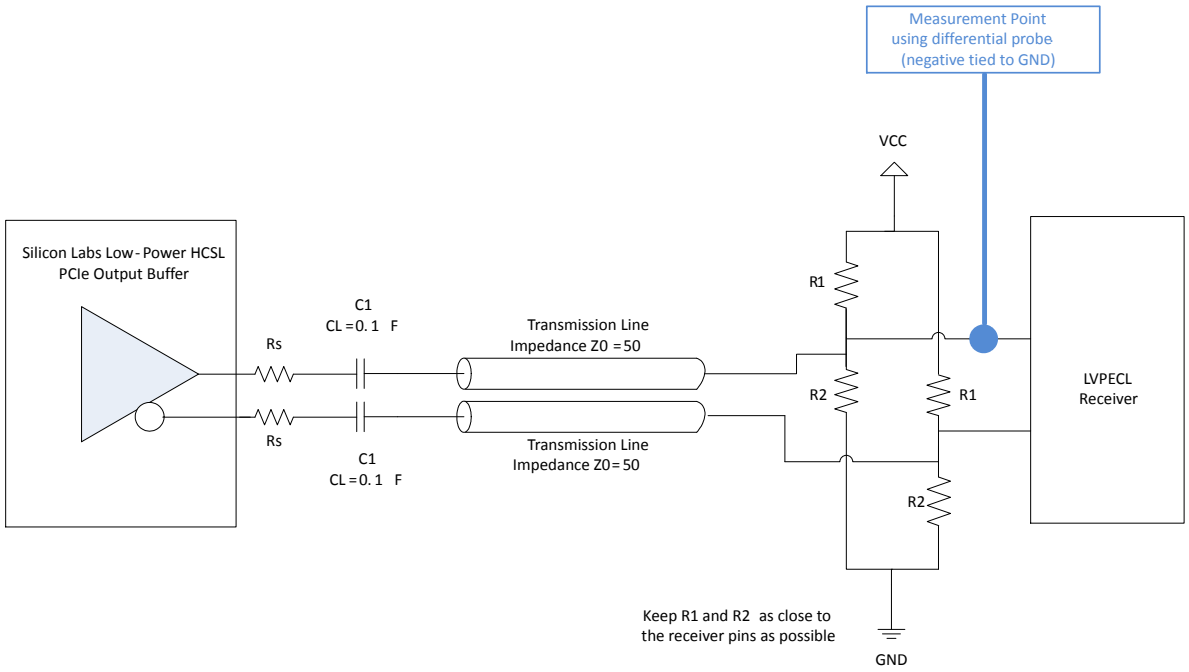

Figure 1.1. Termination Scheme for HCSL to LVPECL Conversion

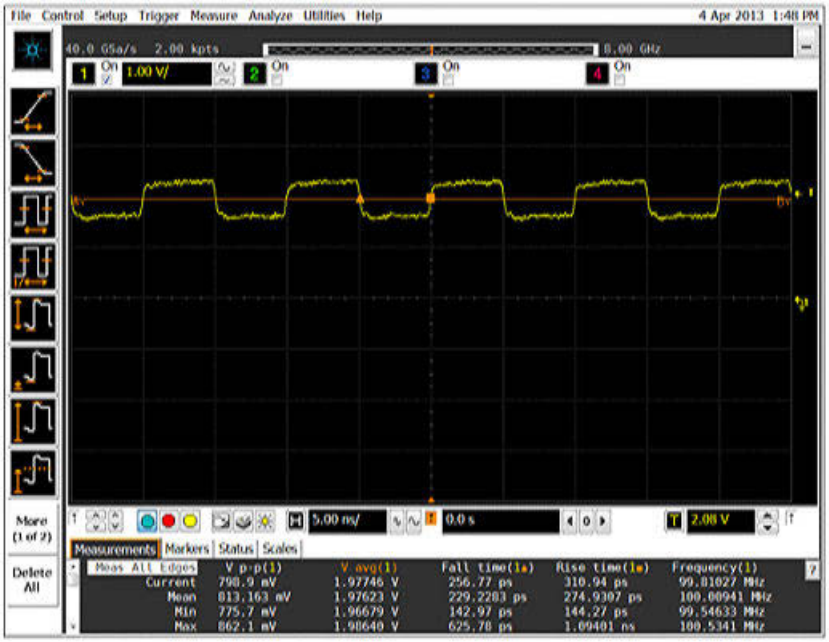

Figure 1.2. Oscilloscope Measurement of LVPECL Conversion

Table 1.1. Resistor Selection for Different VCC Standards (LVPECL Signal Conversion)

VCC	Expected Common Mode Voltage (V)	R1 (kΩ)	R2 (kΩ)
3.3	2	3	5
2.5	1.1	5	4

Table 1.2. Series Resistor Selection for PCIe Clock Generators and Buffers

Device	Zdiff (Ω)	Rs (Ω)
Si5310x, Si5311x	100	33
Si5211x, Si5213x, Si5214x, Si5216x, Si5315x	100	0
Si52202/04/08/12	100	0

2. Conversion of HCSL Signals to LVDS Signals

One can also convert a low-power, push-pull HCSL clock output to a 1.8 V, 2.5 V, or 3.3 V LVDS clock output. The recommended termination scheme is shown in Figure 2.1 Termination Scheme for Low-Power HCSL to LVDS Conversion (When Receiver has no Termination or Internal 100 Ω Termination) on page 4, with the corresponding oscilloscope measurement shown in Figure 2.2 Oscilloscope Measurement of LVDS Conversion (When Receiver has no Internal Termination) on page 4 (at the measurement point indicated in Figure 2.1 Termination Scheme for Low-Power HCSL to LVDS Conversion (When Receiver has no Termination or Internal 100 Ω Termination) on page 4).

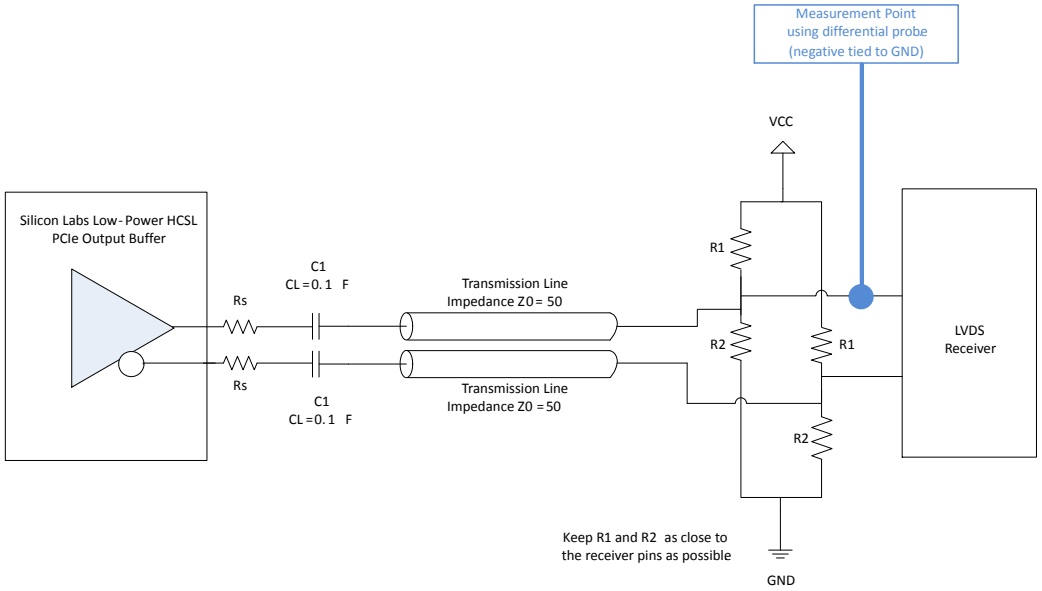

Figure 2.1. Termination Scheme for Low-Power HCSL to LVDS Conversion (When Receiver has no Termination or Internal 100 Ω Termination)

Figure 2.2. Oscilloscope Measurement of LVDS Conversion (When Receiver has no Internal Termination)

The swing will be reduced by 50% by an internal or external termination (the signal will be similar to the signal seen in Figure 2.4 Oscilloscope Measurement of LVDS Conversion (When Receiver has Internal or External 100 Ω Termination) on page 5). If the receiver does not have an internal 100 Ω termination, an external 100 Ω termination may be added, as shown in Figure 2.3 Termination Scheme for Low-Power HCSL to LVDS Conversion (When Receiver has no Internal 100 Ω Termination) on page 5.

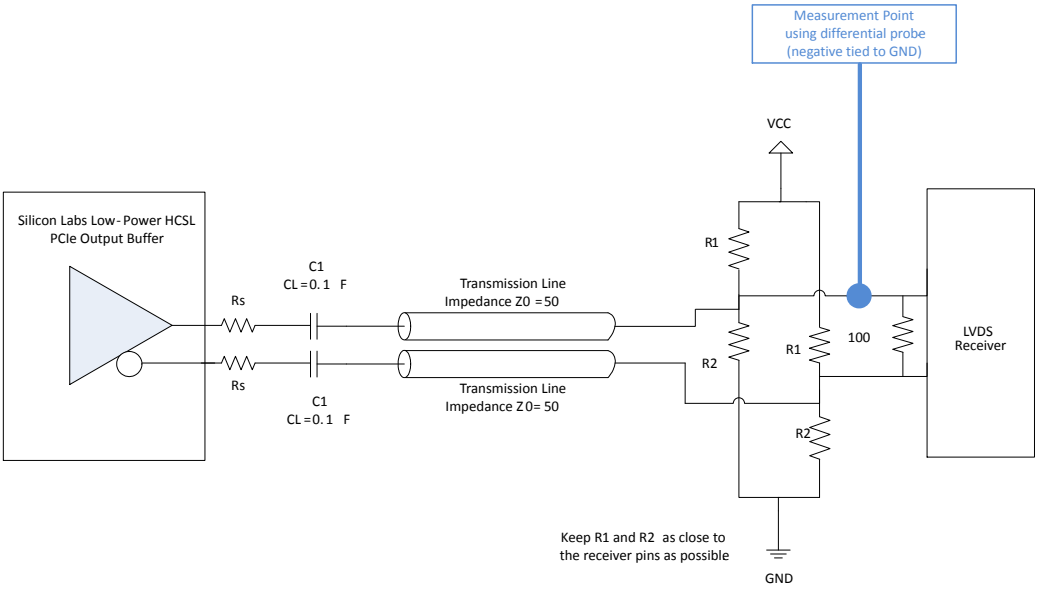

Figure 2.3. Termination Scheme for Low-Power HCSL to LVDS Conversion (When Receiver has no Internal 100 Ω Termination)

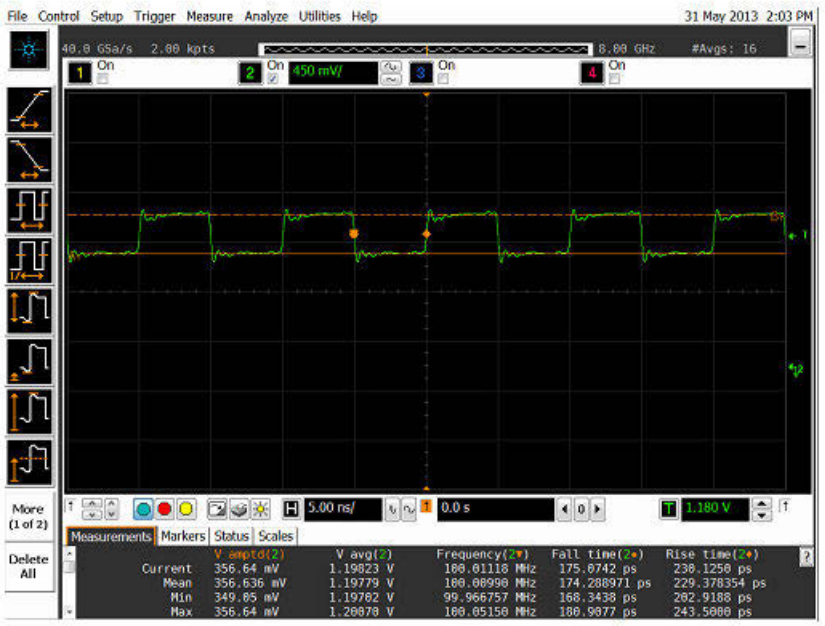

Figure 2.4. Oscilloscope Measurement of LVDS Conversion (When Receiver has Internal or External 100 Ω Termination)

The resistor selection guide for different VCC values at the receiver end is given in Table 2.1 Resistor Selection on page 5.

Table 2.1. Resistor Selection

Voltage Standard (V)	Expected Common Mode Voltage (V)	R1 (kΩ)	R2 (kΩ)
3.3	1.2	5	2.85
2.5	1.2	6	5.5
1.8	1.2	3	6

For series resistor selection of PCIe clock generators and buffers, see Table 1.2 Series Resistor Selection for PCIe Clock Generators and Buffers on page 3.

3. Conversion of HCSL Signals to CML Signals (AC Coupled to Receivers)

AC coupling is the recommended method for converting low-power HCSL signals to CML. The receiver should be able to generate the references needed to generate the common mode for CML signals. The recommended schematic is shown in Figure 3.1 Termination Scheme for HCSL to CML AC Coupling on page 6. It is also important to note that many CML receivers come with internal 50 Ω terminations to VCC, as shown in Figure 3.2 Typical CML Receiver Circuit Structure on page 6. Such internal terminations can reduce the signal swing by 50%.

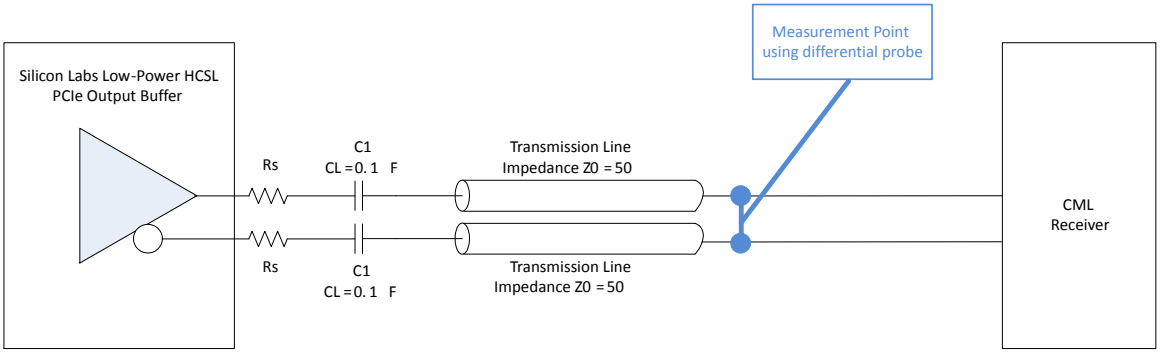

Figure 3.1. Termination Scheme for HCSL to CML AC Coupling

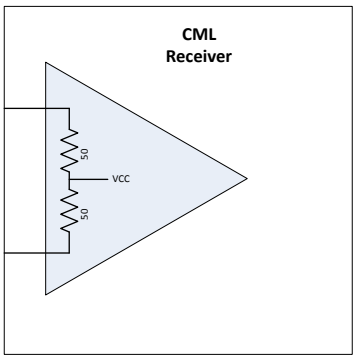

Figure 3.2. Typical CML Receiver Circuit Structure

4. Conclusion

This application note details methods in which low-power HCSL output clocks from the Si5211x, Si5213x, Si5214x, Si5216x, Si5310x, Si5311x, Si5315x, and Si522xx device families can be used to drive receivers that use other differential formats, specifically LVPECL, LVDS, and CML standards.

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