AN871: Driving Long PCIe Clock Lines

This Application Note makes recommendations for driving long PCIe® clock lines based on maintaining the PCIe clock signal integrity and performance required by industry specifications for PCIe clocks. It provides detailed analysis of both push-pull and constant current PCIe drivers to ensure systems maintain the high performance clock signals provided by Silicon Labs PCIe clock products.

KEY FEATURES OR KEY POINTS

- Constant Current vs Push-Pull Output Driver Comparison
- Output Amplitude and Rise/Fall Time Performance vs Trace Length Measurement Graph
- Trade-offs between Microstrip vs Stripline

1. PCIe Clock Signal Specifications

The Peripheral Component Interconnect Express (PCIe) standards were developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG). The first generation of specifications, known as 'Gen1', supports a bit rate of 2.5 Giga-Transfers per second (GT/s) and has been modified to support the higher bit rates of 5 GT/s, 8GT/s and now 16GT/s for Gen 2, Gen 3 and Gen 4 respectively. At the time this application note was written, the Gen4 specifications are in draft form and expected to be finalized by 2015.

PCIe Generation	Data Rate (GT/s)
Gen1	2.5
Gen2	5.0
Gen3	8.0
Gen4	16.0

Throughout these speed updates, the PCIe reference clock has continued to use HCSL signaling levels. Similarly, the signal integrity specifications have remain unchanged even though the jitter specifications have been revised. The key signal integrity specifications for the reference clock, referred to as "Refclk", are found in the PCI Express Base Specification Rev 4.0..

The signal integrity parameters that are effected by transmission line length include those shown in Figures 1 and 2 below. Although the PCI-SIG specifications allow an edge rate as slow as 0.6 V/ns differential, major silicon manufacturers require 1.0 V/ns minimum.

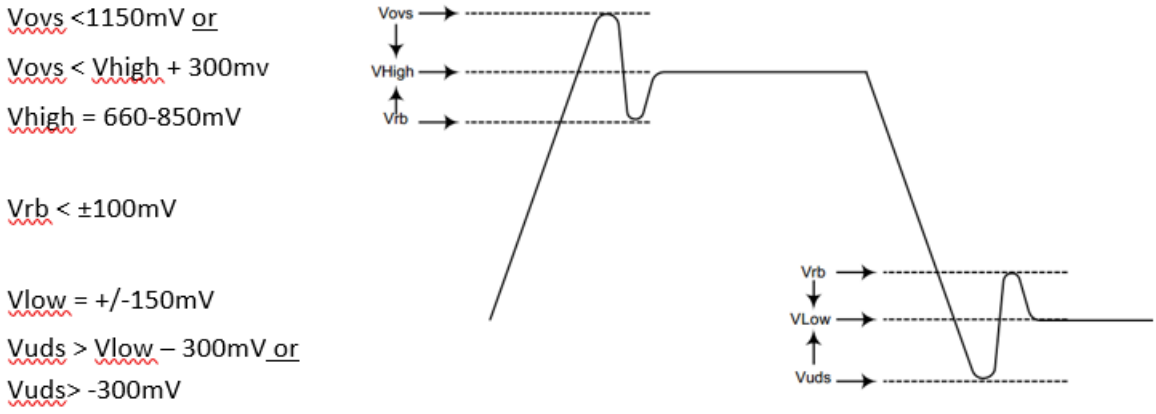

Figure 1.1. PCIe Single-Ended Signal Integrity Limits

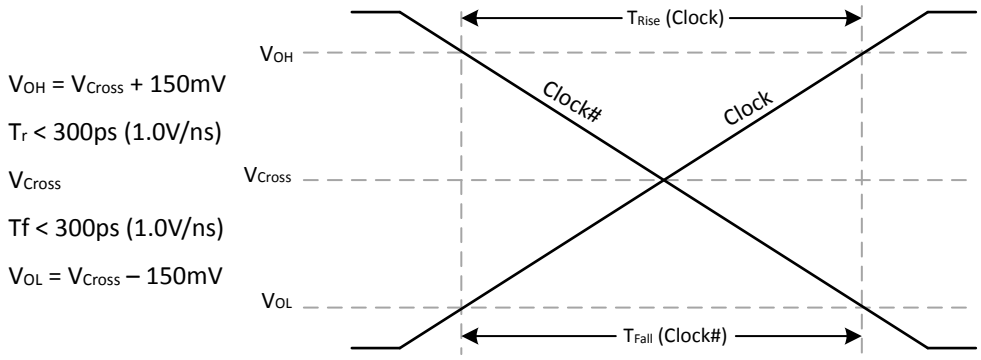

Figure 1.2. PCIe Differential Signal Integrity Limits

2. Types of PCIe Clock Drivers

There are two types of PCIe output buffers for clock drivers, constant current and “push-pull”. Figure 2.1 PCIe Clock Driver Types on page 3 shows the architecture of both types. The constant current output switches a constant current, Iout, between the Clock and Clock# output pins. With Rt set to 50 Ω to match the characteristic trace impedance, Zo, Iout needs to be 15 mA to produce a 750 mV single ended signal swing. The push-pull output is similar to a rail-to-rail LVCMOS1 output where the top voltage rail is regulated to the HCSL output high voltage, Vhcsl, typically 750 mV. Setting Ron + Rs to 50 Ω minimizes reflected signals. The push-pull architecture requires fewer external components, with Rs either being external or internal to the clock generator/buffer device. Another advantage of push-pull architecture is reduced power consumption. In addition, push-pull outputs can drive a longer PCB trace length.

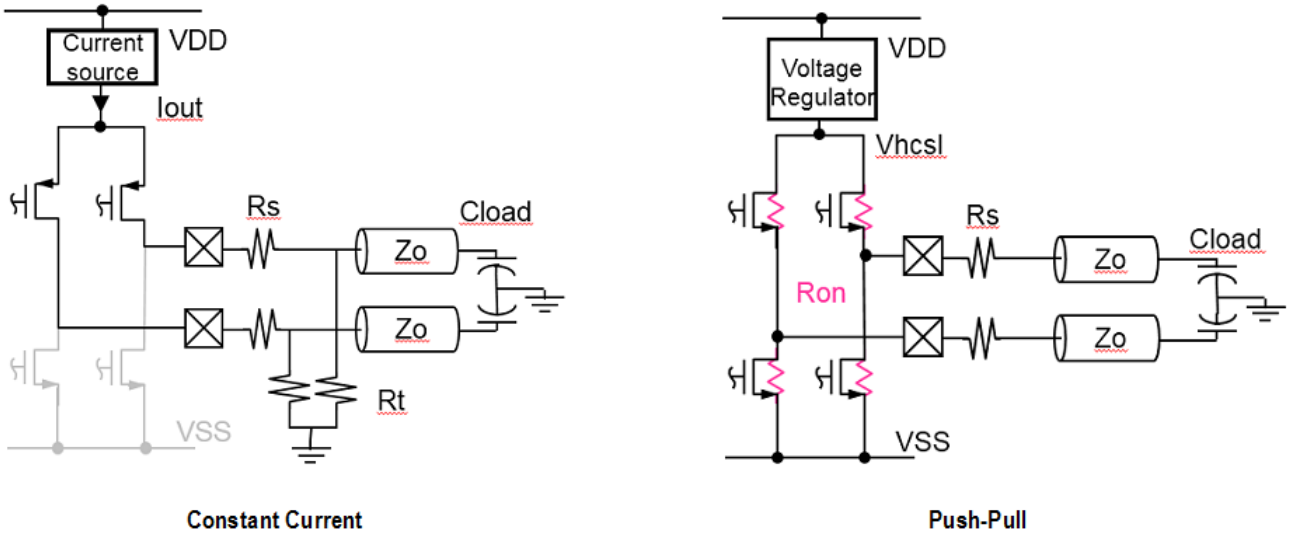

Figure 2.1. PCIe Clock Driver Types

3. Long Trace Lengths

Maximum trace length is not defined by the PCIe specifications. Due to variations in PCB technology and performance, a test length creating a 15 dB loss at 4 GHz is now recommended in GEN 4.0. Previously a test length of 12 inches was used in Rev 3.0 for measuring RFLFCLK jitter as shown in the figure below. Figure 3.1 PCIe Standards Refclk Test Setup on page 4 assumes the trace termination components are included in the Refclk generator block even though they may be external to the clock generator or buffer. Major component manufacturers often specify 10” trace lengths for measuring signal integrity.

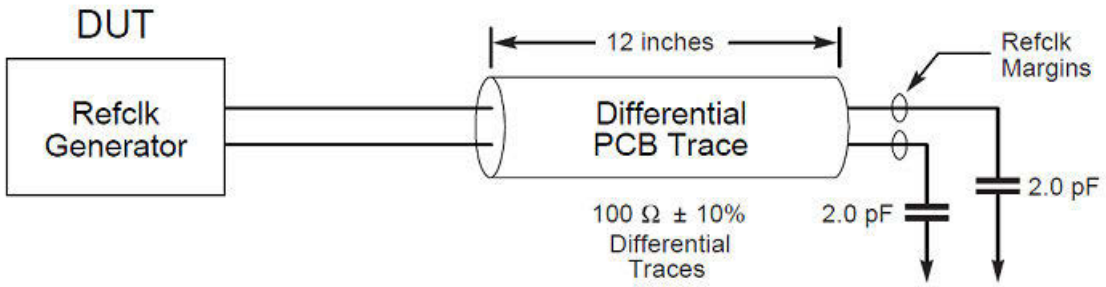

Figure 3.1. PCIe Standards Refclk Test Setup

There are applications where trace lengths greater than 12” are preferred, such as in servers and storage. Provided the Refclk jitter and signal integrity specifications are met at the input of the PCIe endpoint, longer trace lengths are acceptable.

The length of a perfect or ‘lossless’ transmission line would not affect the signal integrity of a clock signal, and could theoretically be of infinite length. However, all transmission lines have parasitic losses that degrade the signal. The primary parameters that become degraded are Tr/Tf and Vhigh. In addition any discontinuities in trace impedance (changes in trace impedance along the trace) will result in additional losses that reflect back to the source.

Differential clock traces are typically laid out as either a stripline or a microstrip, as shown in Figure 3.2 Two Types of Differential Clock Traces on page 4. A microstrip has roughly twice the parasitic losses compared to a stripline. Since the clock signals originate on the surface of the board and end up driving a component that is also on the surface of the board, the most common clock trace routing is the microstrip which avoids the impedance discontinuity of vias used to get to an inner layer. The most common 50 Ω microstrip width is 6 mils on FR4. Stripline can provide greater isolation due to the shield layer above and below the transmission line, but can result in higher manufacturing cost as well as problematic troubleshooting/access issues.

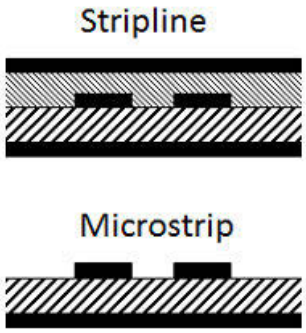

Figure 3.2. Two Types of Differential Clock Traces

4. Performance of Silicon Labs PCIe Clock Drivers

Silicon Labs has a growing portfolio of PCIe clock generators and buffers, supporting both constant current and push –pull driver technologies. Figure 3.2 Two Types of Differential Clock Traces on page 4 shows a simulation of both types of drivers driving a 24” lossy, 50 Ω trace (100 Ω differential). Both types of drivers provide similar performance. Although this is twice the length of the PCIe test circuit, it is evident that the amplitude of 750 mV and an edge rate of 3 V/ns are well within the signal integrity limits for a PCIe clock.

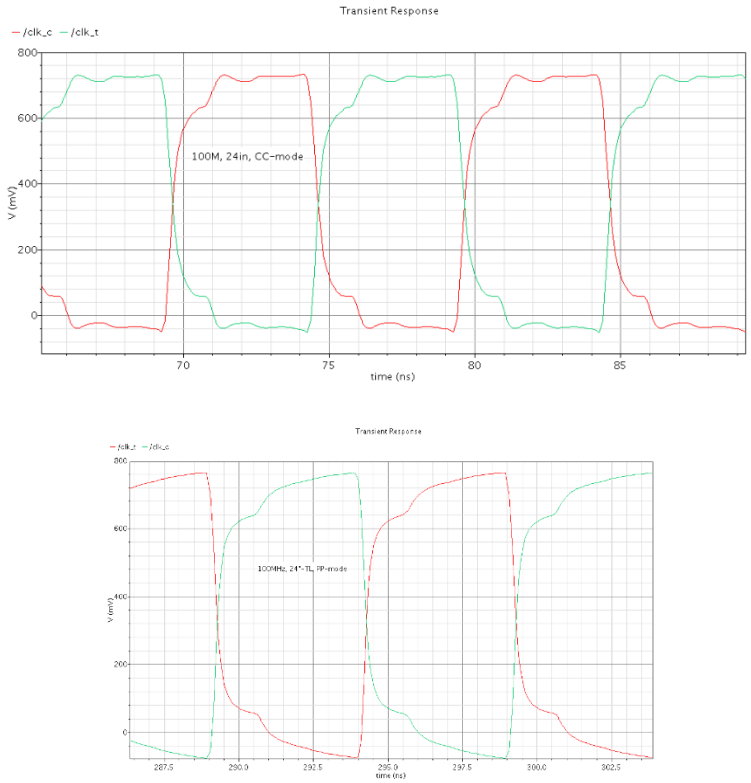

Figure 4.1. Simulated Waveforms Driving 24”, 100 Ω Differential, Lossy Microstrip

5. Maximum Trace Length

The maximum length that can be driven by a PCIe clock driver will depend on the specific properties of the PCIe clock driver and the parasitic losses of a particular trace layout and board manufacturing process. Figure 5.1 Push-Pull Driver Signal Degradation vs. Line Length on page 6 graphs the simulated performance of a Silicon Labs PCIe clock driving a typical 6 mil, 50 Ω, lossy transmission line on an FR4 board with 2 pf end load. The amplitude includes over and undershoot which accounts for the initial amplitude being higher than the 750 mV nominal value. Although the trend lines indicate that lengths up to 96” can be driven, reflections and manufacturing board tolerances limit the maximum trace length to something less than 84” for a continuous transmission line without impedance discontinuities.

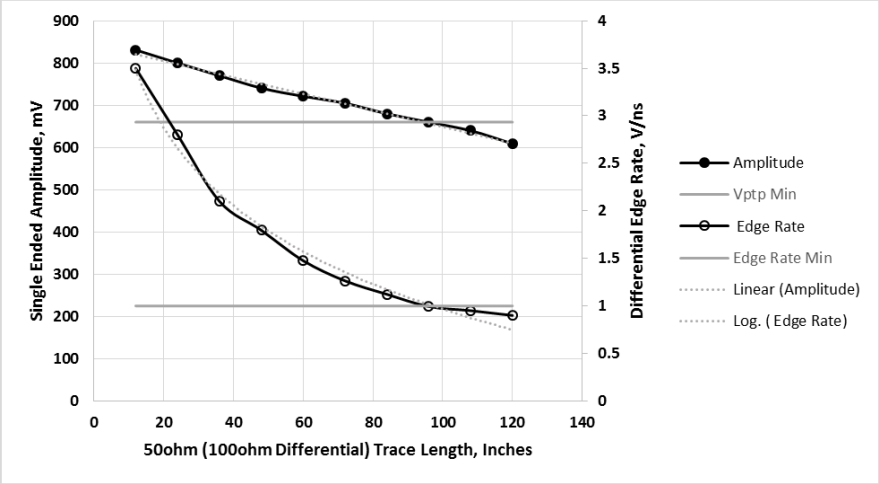

Figure 5.1. Push-Pull Driver Signal Degradation vs. Line Length

The simulated waveforms for both constant current and push-pull drivers at 84” are shown in the figure below. This indicates that the push-pull drivers have a slight advantage when driving long traces. The simulation data shows that the push-pull can effectively drive up to 84”, while the constant current would be limited to less than 60”.

If impedance discontinuities from vias or card connectors will be part of the transmission line, the maximum line length will need to be shortened depending on the magnitude of the discontinuity. The effect of discontinuities can be minimized by keeping their reflections away from the edge being launched at the driver. This means avoiding discontinuities at distances, d, from the clock source where:

d = n x (half period) / (edge velocity) / 2 ± 10%

The half period is used since both the rising and falling edges reflect, and we include a 10% factor to cover modeling uncertainty and board manufacturing tolerances of the edge velocity. For example a 100MHz clock with a board velocity of 180ps/inch should avoid discontinuities at:

n x 14in ±1.4in (= 5ns / 180ps/in / 2 ±10%)

where n is an integer.

Although common-mode noise such as that created by ground plane coupling is rejected by the differential signal, it should be noted that the slower edge rates resulting from longer transmission lines will make the clock signal edges more sensitive to differentially coupled noise (noise coupled to one of the Clock or Clock# signals but not the other). Therefore, care must be taken to protect long clock traces from differentially coupled noise by routing ground shields next to the clock lines, routing normally inactive signals next to the clock lines, or allowing extra spacing to adjacent traces.

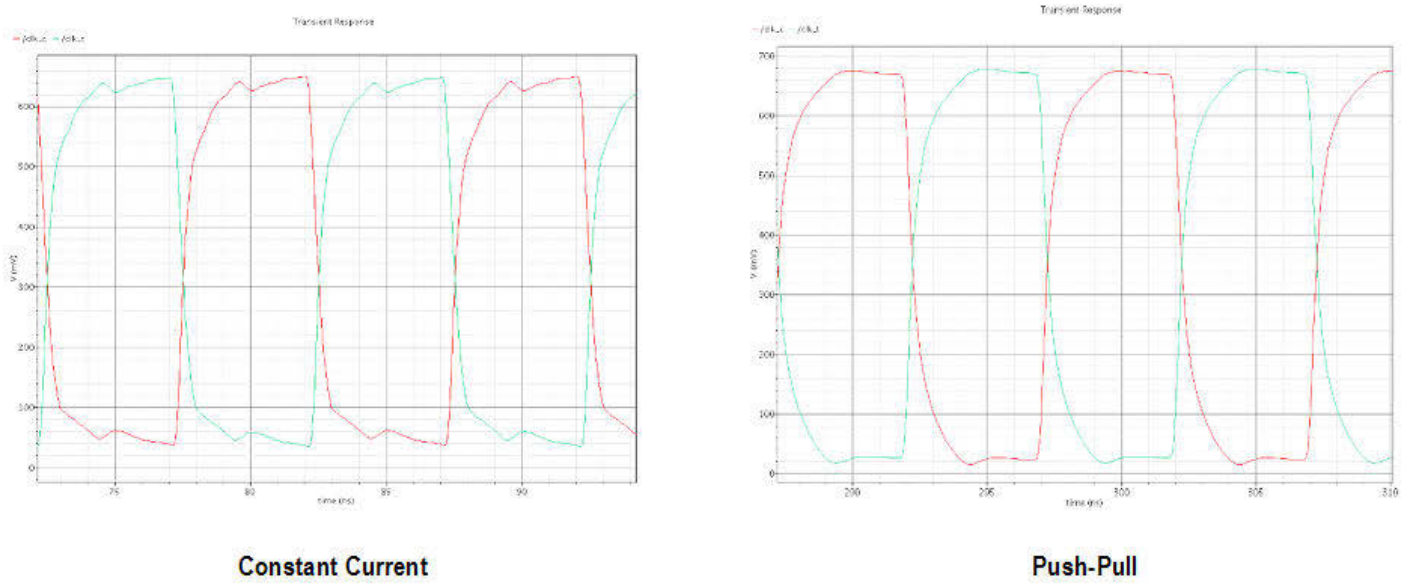

Figure 5.2. Simulated Waveforms Driving 84in, 100 Ω Differential, Lossy Microstrip

6. Summary

The information presented in this application note indicates that Silicon Labs PCIe clock drivers can drive up to 84” or 60” 100 Ω differential (50 Ω single-ended), microstrip, lossy transmission lines for the push-pull or constant current driver formats respectively. These distance limits are for continuous transmission lines without impedance discontinuities. Guidelines for impedance discontinuity “keep-out” areas for avoiding edge corrupting signal reflections were also provided. The slower edge rates created by longer transmission lines require the clock traces to be protected from differentially coupled noise.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
www.silabs.com/timing

SW/HW
www.silabs.com/CBPro

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701