AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84

The Si884xx/Si886xx product families integrate digital isolator channels with an isolated dc-dc controller. The Si8282 and Si8284 are isolated gate drivers with the integrated dc-dc controller. This application note provides guidance for selecting the external components necessary for operation of the dc-dc controller.

Digital isolation (isolated gate driver) applications with primary-side supply voltage V_{IN} > 5.5 V or load power requirements of ≥2 W can use Si884xx, Si886xx, Si8282, or Si8284 products. The dc-dc controller used in these products employs an isolated flyback circuit topology. This type of topology can be easily customized for high-voltage and high-power supply applications.

KEY FEATURES

- Isolated flyback dc-dc converter
- For applications with primary side supply voltage V_{IN} > 5.5 V or load power requirements ≥2 W
- Simplified dc Steady State Analysis
- Dynamic Response
- Design Example: Guidance for transformer design and dc-dc converter external component selection

1. Introduction

The following figure shows the typical isolated flyback converter circuit using Si86xx devices. The components shown in the figure below are input capacitor C2, transformer T1, power switching FET Q1, current sense resistor R12, primary snubber R16 and C19, secondary diode D1, output capacitor C10, secondary snubber R8 and C8,voltage sense resistors R5 and R6, and compensation network components R7 and C11. Q2, R14, and C14 create a regulator circuit to power VDDA from VIN. D8, Q3, R17, R18, and R19 serve to ensure proper turn-off of Q1 upon dc-dc converter shutdown. R13 and C6 set the switching frequency and soft start characteristics for product variants that use external frequency and soft start control.

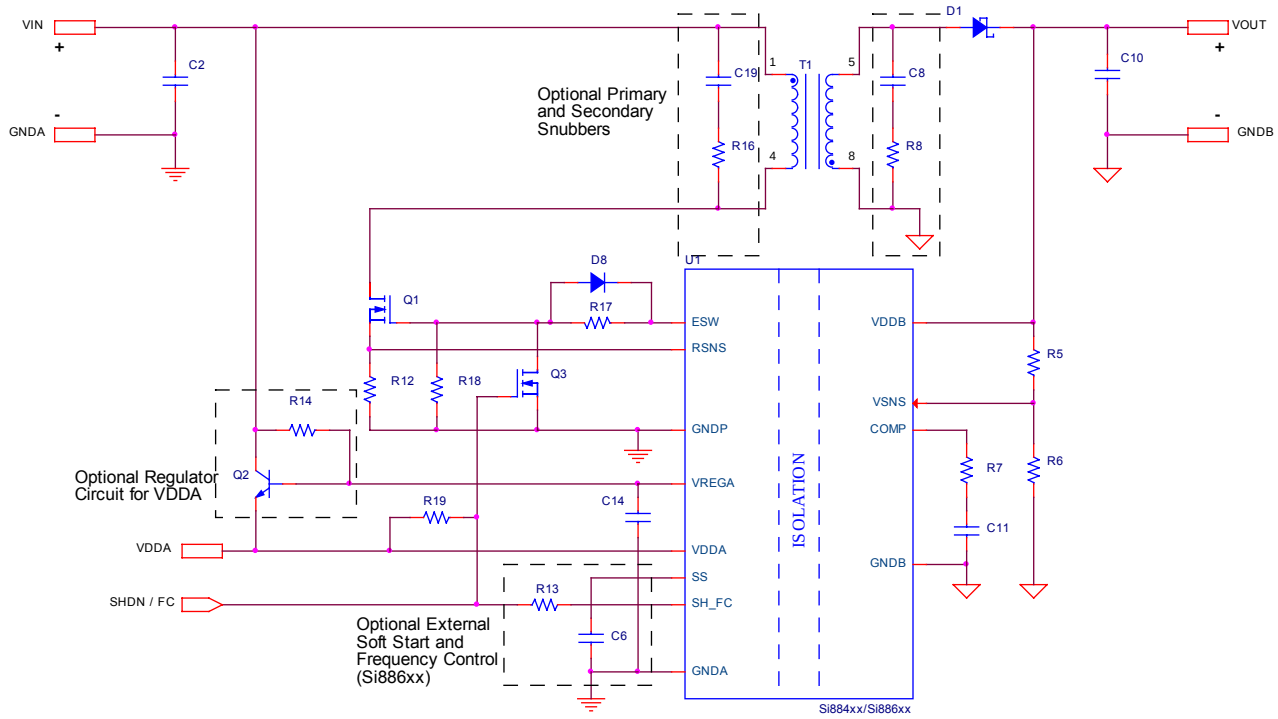


Figure 1.1. Typical Isolated Flyback Converter Circuit Using Si886xx Devices

The following figure shows the typical isolated flyback converter circuit using Si8282/84 isolated gate driver and its optional support circuitry. The circuit topology is almost identical to the circuit above except for the dual output voltage rails. The additional transformer output tap, D2, and C20 create the other output voltage rail. In this configuration, the secondary side ground reference, GNDB, is set to the midpoint of the transformer output taps. Thus, the positive and negative voltage supplies are produced by the dc-dc converter to power the gate driver VDDB/VSSB pins.

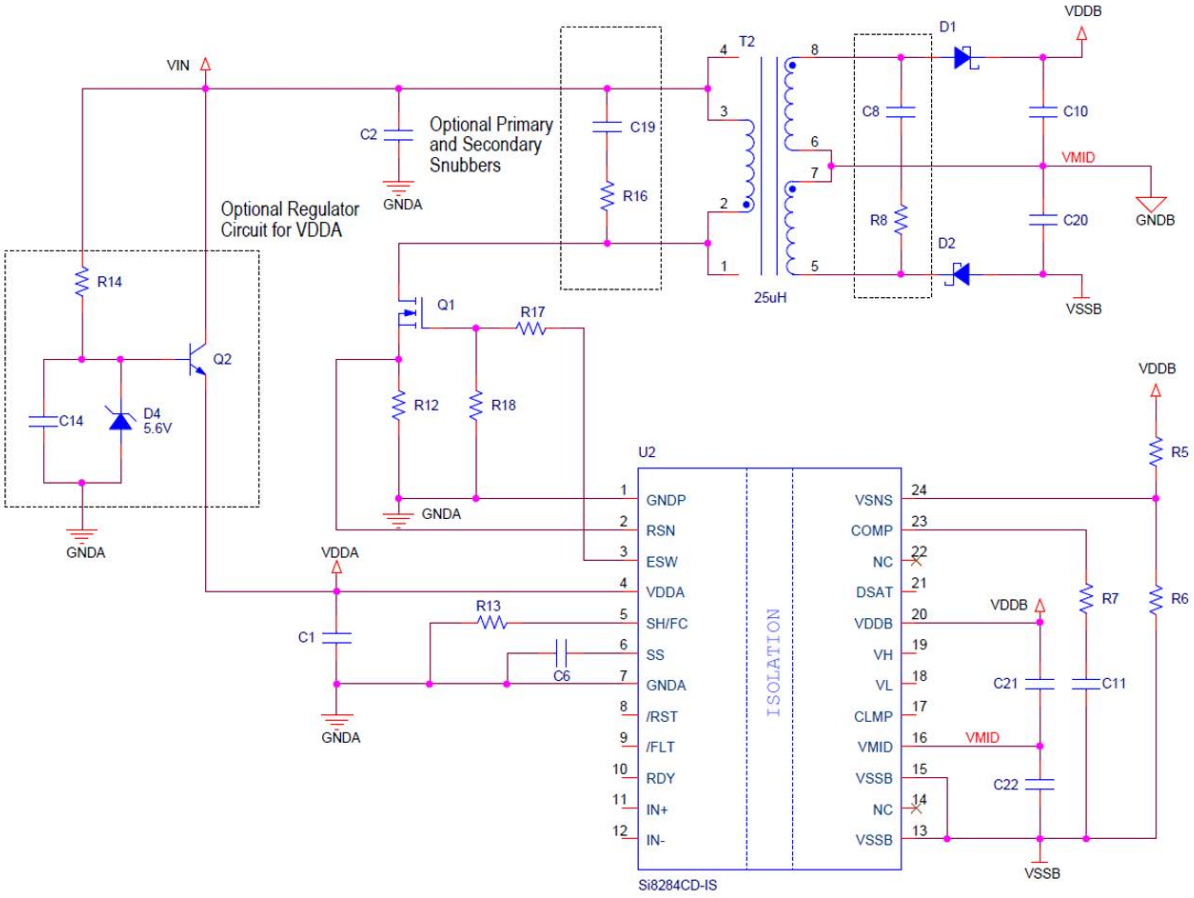


Figure 1.2. Typical Isolated Flyback Converter Circuit Using an Si8284 Isolated Gate Driver

2. Simplified DC Steady State Analysis

Analyzing the flyback behavior in dc steady state provides formulas to assist with selecting values for the components used. In this analysis, it is assumed that components are ideal, at 100% efficiency ($P_{IN} = P_{OUT}$), and the circuit has reached equilibrium.

The figure below shows the critical components of the flyback converter. The transformer model includes magnetizing inductance L_m and leakage inductance L_{lkg}. R_{LOAD} does not necessarily represent a physical resistor, rather it is an expression of V_{OUT}/I_{OUT}.

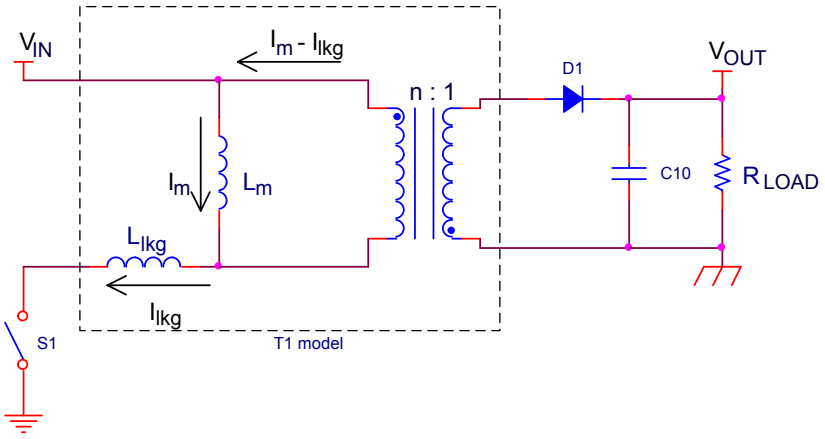


Figure 2.1. Flyback Converter

For dc steady state analysis, the two modes where the system operates the majority of the cycle are only required when S1 is closed and when S1 is open. Figure 2.2 Inductor Currents on page 5 depicts the simplified magnetizing and secondary current waveforms.

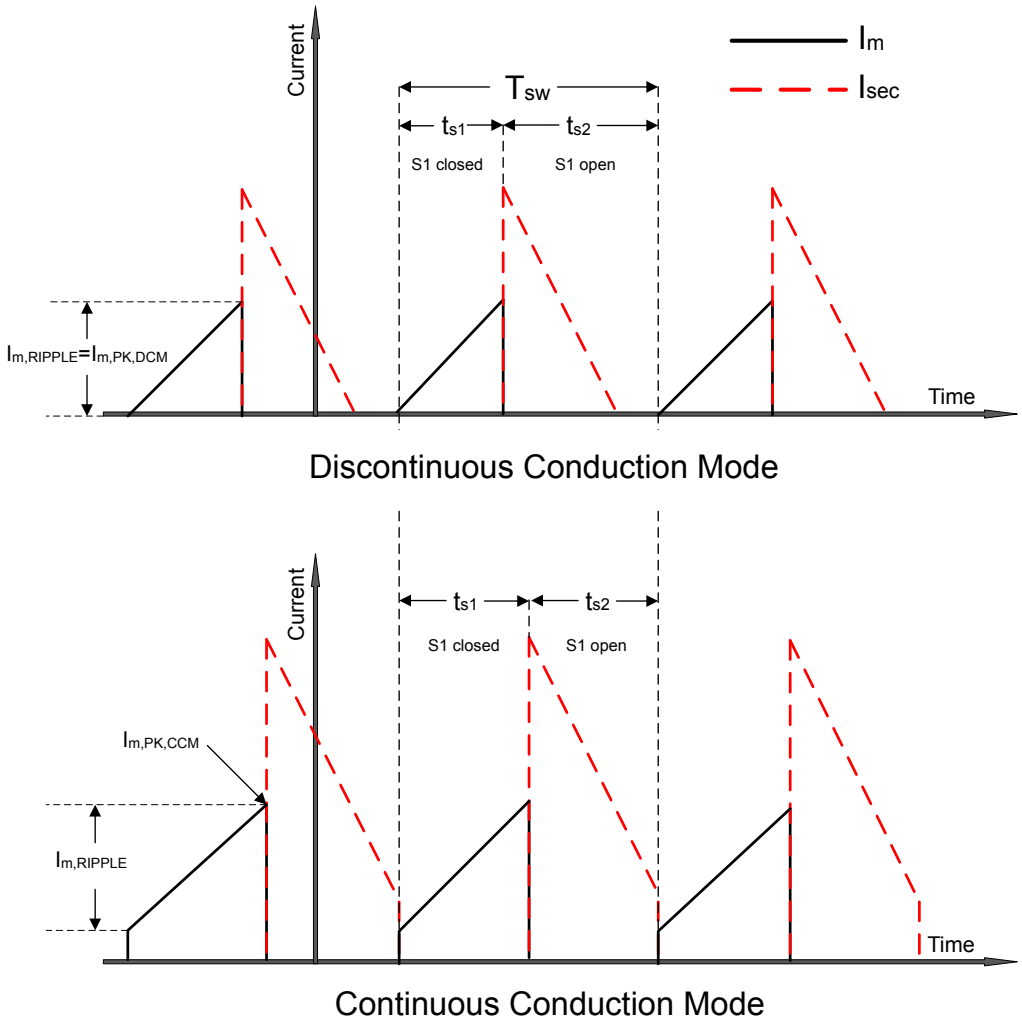


Figure 2.2. Inductor Currents

2.1 S1 Closed

V_{IN} is applied to the primary inductance L_m. As a result, current flows through inductance L_m and energy is stored in the magnetic field of the transformer T1:

$$V_{IN} = \left(L_m + L_{lkg}\right)\frac{I_{m,RIPPLE}}{t_{S1}}$$

Equation 1.

$I_{m,RIPPLE}$ is the magnetizing current ramp during t_{S1}, and t_{S1} is the time that S1 is closed. In Discontinuous Conduction Mode (DCM), $I_{m,RIPPLE}$ is equal to $I_{m,PK}$ as primary and secondary currents return to zero before the next cycle. In Continuous Conduction Mode (CCM), the currents do not reach zero before the next switching cycle.

2.2 S1 Open

The instant S1 opens, current can no longer flow through the primary and the magnetic field collapses, transferring energy to the secondary, causing current to flow out of the dot of the ideal transformer. The energy stored in the leakage inductance is not transferred and it must be dissipated in the primary through the snubber network. The voltage at the secondary will be impressed on the primary. The governing current equation is:

$$\frac{I_{m,RIPPLE}}{t_{S2}} = \frac{nV_{OUT}}{L_m}$$

Equation 2.

where n and t_{S2} are primary to secondary turns ratio and time that S1 is open, respectively.

2.3 DC-DC Converter Disable

When using the dc-dc converter, an active pull down MOSFET (Q3) is required to ensure the gate of Q1 (S1) is pulled to GNDA, as shown in Figure 2.3 on page 6 below. The shutdown control pin is SH_FC, which also serves as a frequency control point for the dc-dc converter. During operation, the signal SHDN/FC is held low, providing a reference ground for the current through R13. When shutdown is required, the signal at SHDN/FC is asserted high, which commands the dc-dc converter to turn off via the SH_FC pin. SHDN/FC also drives the gate of Q3 high. Q3 drain pulls the gate of Q1 low, actively disabling Q1 and keeping the converter off. R17 allows passage of ESW drive current to the gate of Q1, but also provides some buffering between ESW and Q3 drain to avoid contention for Q1 gate. Diode D8 allows ESW to provide more drive to Q1 gate during normal operation pull down. R18 provides pull down for Q1 gate in the absence of VDDA. R19 provides fail-safe dc-dc converter disable when the MCU is unpowered or not driving the signal SHDN/FC.

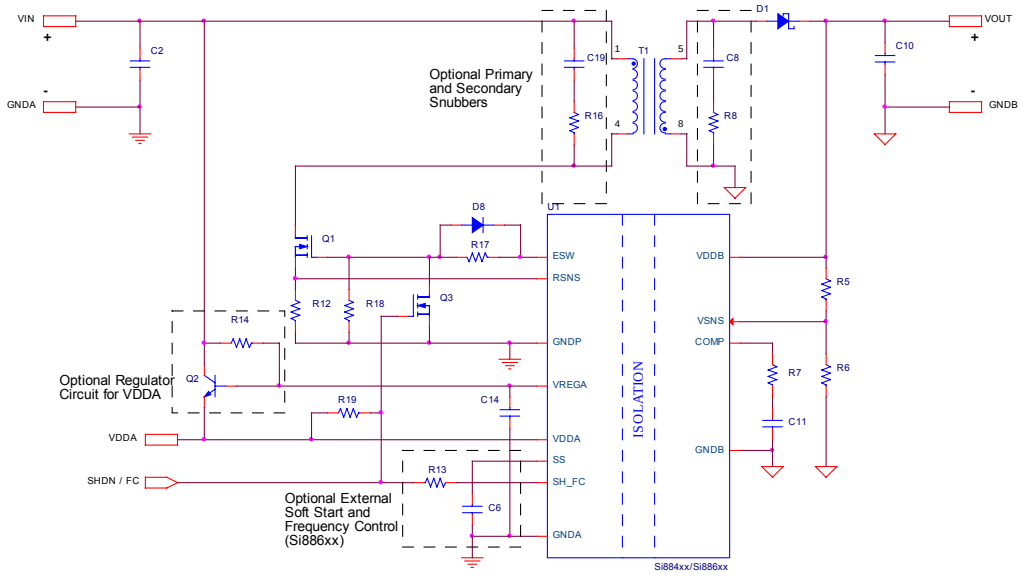


Figure 2.3. DC-DC Converter Disable

Component	Value
Q3	BSS138
D8	1N4148W
R17	20 Ω maximum, ¼ W
R18	10 kΩ, 1/10W
R19	10 kΩ, 1/10W

2.4 Voltage Transfer

Let duty cycle D be defined as the ratio of time S1 is closed over the complete switching period T_{sw}:

$$D = \frac{t_{S1}}{t_{S1} + t_{S2}}$$

Equation 3.

Now t_{S1} and t_{S2} can be expressed in terms of D and switching period as:

$$t_{S1} = DT_{sw}$$

Equation 4.

$$t_{S2} = (1 - D)T_{sw}$$

Equation 5.

and assume diode D1 has no voltage drop when conducting the volt-second balance equation for L_m, which in CCM operation can be written as:

$$V_{IN}DT_{sw} - (nV_{OUT})(1 - D)T_{sw} = 0$$

Equation 6.

The equation simplifies to:

$$V_{OUT} = \frac{V_{IN}D}{n(1 - D)}$$

Equation 7.

For DCM, current does not flow out of the secondary over the entire (1-D) portion, which changes the voltage transfer function shown in Equation 7. Unlike CCM, the voltage transfer characteristics in DCM are dependent on factors such as and switching frequency. The governing equation is:

$$V_{OUT} = V_{IN}D\sqrt{\frac{R_{LOAD}T_{sw}}{2L_m}}$$

Equation 8.

2.5 Magnetizing Current

Substituting Equation 1. into Equation 4., the ripple magnetizing current is:

$$I_{m,RIPPLE} = \frac{V_{IN} t_{S1}}{L_m} = \frac{V_{IN} D T_{sw}}{L_m}$$

Equation 9.

The average magnetizing current is related to the output current as:

$$I_{m,AVE} = \frac{I_{LOAD}}{n(1 - D)}$$

Equation 10.

When a flyback converter is operating in CCM, the peak magnetizing current is given by the average current plus one half of the ripple current:

$$I_{m,PK,CCM} = I_{m,AVE} + \frac{V_{IN} D T_{sw}}{2 L_m}$$

Equation 11.

When a flyback converter is operating in DCM, the peak magnetizing current is equal to the ripple current:

$$I_{m,PK,DCM} = I_{m,RIPPLE}$$

Equation 12.

The controller limits the peak magnetizing current by comparing the voltage across the current sense resistor R12 to an internal reference voltage of approximately 100 mV. If more than 100 mV is developed across R12 during S1 closed, the controller immediately switches S1 open. The controller maintains the same switching period, but reduces the duty cycle D to limit peak current. The cycle by cycle current limit is given by:

$$I_{m,LIMIT} = \frac{100mV}{R12}$$

Equation 13.

2.6 Optional Primary Snubber

Snubbers are used for two purposes in a flyback converter: to limit the peak voltage on the drain of the Q1, and to attenuate high frequency ringing that leads to emissions. There are several methods to create a primary side flyback snubber. The RC snubber is presented here. The energy stored in the leakage inductance L_{lkg} does not transfer to the secondary and must be dissipated in the primary. The power dissipated in the leakage inductance is given by:

$$P_{lkg} = \frac{L_{lkg} I_{m,PK}^2}{2T_{sw}}$$

Equation 14.

When S1 opens, the current flowing in the primary will charge the drain-source capacitance of Q1 causing the voltage at the drain to increase rapidly. When this voltage exceeds $V_{IN} + nV_{OUT}$, a ringing occurs with frequency dependent on the inductance leakage L_{lkg} and C_{ds}. The RC snubber presents a load for which to dissipate the power stored in the inductance leakage. This load limits the switching speed of Q1, which limits the peak voltage across the drain-source. A first order approximation for determining R16 and C19 is to set them to the characteristic impedance of the ringing caused by L_{lkg} of T1 and C_{ds} of Q1.

$$R16 = \sqrt{\frac{L_{lkg}}{C_{ds}}}$$

Equation 15.

Since the ringing frequency:

$$f_{fing} = 1 / \left(2\pi\sqrt{L_{lkg} \times C_{ds}}\right)$$

R16 can be determined by measuring L_{lkg} and ringing frequency:

$$R16 = 2\pi f_{ring} L_{lkg}$$

Equation 16.

C19 can be set to the same impedance using:

$$C19 = \frac{1}{2\pi f_{ring} R16}$$

Equation 17.

2.7 Input Capacitor

The purpose of C2 input capacitor is to provide filtering for V_{IN} during the switching cycle and reduce voltage ripple at the converter input. Neglecting the V_{IN} source impedance, the ripple voltage at C2 is approximately due to supplying the magnetizing ripple current during the switcher turn-on time. The total accumulated charge provided by C2 per cycle is the integration of the magnetizing ripple current over the switcher turn-on period. By using $\Delta V = \Delta Q / C$, the approximate C2 voltage ripple in both CCM and DCM is given by:

$$V_{IN,RIPPLE} = \frac{I_{m,RIPPLE} \times D \times T_{SW}}{2 \times C_2}$$

Equation 18.

2.8 Optional Regulator for VDDA Supply

VDDA valid operating range is between 3.0 V and 5.5 V. In applications where the only source available on the primary side is above 5.5 V, Si884xx/Si886xx provides a voltage reference for an external regulator circuit. The Si8282/84 does not provide the built-in Zener diode, and the external Zener diode is required at the base of Q2.

The regulator circuit consists of transistor Q2, R14, and C14, as shown in Figure 2.4 External Regulator Circuit on page 10. The circuit behind the VREGA pin can be modeled as a zener diode connected from VREGA to GNDA, and requires input current between 350 µA to 950 µA to establish a nominal 4.85 V reference at the VREGA pin. This reference is tied to the base of Q2 and the emitter outputs approximately a 4.3 V supply suitable to power VDDA.

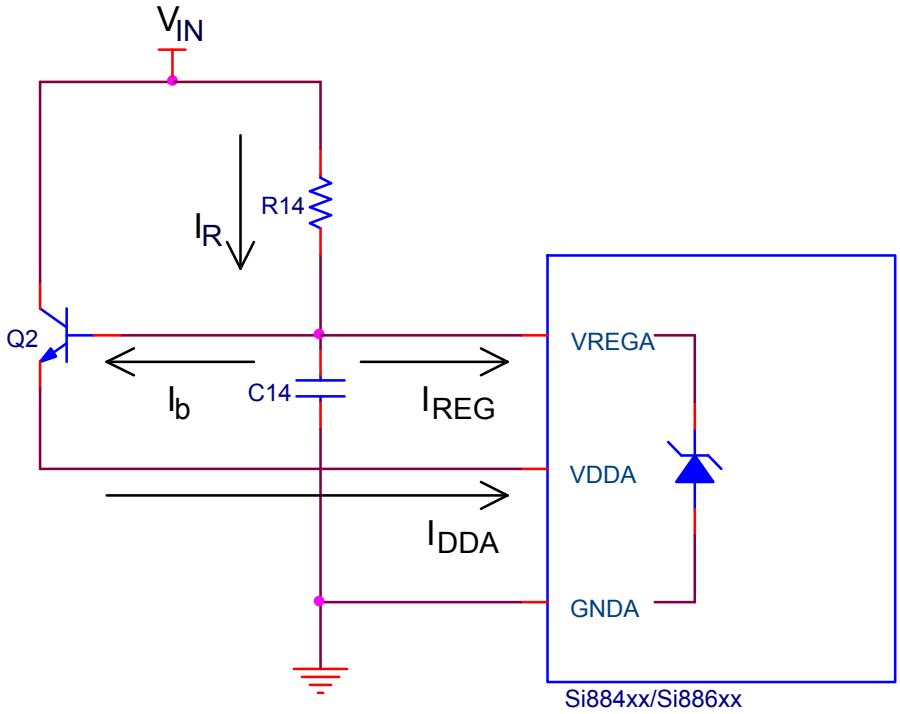


Figure 2.4. External Regulator Circuit

The governing equations for the circuit are:

$$I_R = I_B + I_{REG} = \frac{V_{IN} - V_{REGA}}{R_{14}}$$

Equation 19.

$$I_{DDA} = I_B(\beta + 1)$$

Equation 20.

$$V_{DDA} = V_{REGA} - V_{be}$$

Equation 21.

It is recommended to set I_R to no more than 950 µA no matter I_{DDA} load. As I_{DDA} increases, more of I_R will flow into the base of Q2. V_{REGA} reference voltage will be maintained as long as the I_{REG} > 350 µA. Choose Q2 with adequate gain β to source the maximum expected I_{DDA}. The recommended value for C14 filter capacitor for the VREGA reference is 100 nF.

To ensure reliable dc-dc operation, the following layout guidelines are recommended:

- VDDA and VREGA should be connected by the shortest possible trace. A minimum trace width of 15 mils is recommended.
- GNDA and GNDP should be directly connected by the shortest possible trace. A minimum trace width of 15 mils is recommended.
- Bypass capacitor should be directly connected between VREGA/VDDA and GNDP. A minimum trace width of 15 mils is recommended.
- GNDA should be directly connected to a ground plane.

2.9 Diode and Output Capacitor

In CCM, current flows through D1 only during the (1-D)T_{sw} portion of the steady state cycle. During the DT_{sw} portion of the cycle, I_{LOAD} is sourced solely by the output capacitor, C10. Output voltage ripple on C10 can be calculated by:

$$V_{OUT,RIPPLE} = \frac{I_{LOAD} DT_{sw}}{C10}$$

Equation 22.

In DCM, the output voltage ripple on C10 can be calculated by:

$$V_{OUT,RIPPLE} = \frac{I_{LOAD}(1-\alpha)T_{sw}}{C_{10}}$$

Equation 23.

where αT_{SW} is the duration that D1 remains the conduction while the switcher is off. In DCM, $\alpha T_{SW} < (1-D)T_{SW}$. Using $\alpha T_{SW} = D \cdot T_{SW} \cdot V_{IN}/nV_{OUT}$:

$$V_{OUT,RIPPLE} = \frac{I_{LOAD} \ T_{sw}}{C_{10}} \left(1 - \frac{DV_{IN}}{nV_{OUT}}\right)$$

Equation 24.

Since the output capacitor doesn't consume the power, the average current of output diode D1 in both CCM and DCM cases is equal to the load current.

$$I_{D1,AVE} = I_{LOAD}$$

Equation 25.

The diode peak current is the product of transformer turn ratio and peak magnetizing current:

$$V_{D1,PK} = n \times \ I_{m,PK}$$

Equation 26.

When D1 is reverse-biased, it must withstand:

$$V_{D1,REV(D)} = \frac{V_{IN}}{n} + V_{OUT}$$

Equation 27.

When operating the converter at high ambient temperatures (>70 °C), low-leakage rectifying diodes are needed in the power supply output. The following table describes a diode that was tested in the circuit and will fulfill these requirements:

Table 2.1. DC-DC Supply Output Rectifier Diode for High Working Temperatures

Mfr P/N	Mfr / Website	Vf(max)	Leakage Current (Reverse Current, Max)
MBR0580S1	Diodes Inc. www.diodes.com	800 mV @ 0.5 A, 25 °C	280 µA typ @ VR = 80 V, TA = +125 °C, Short duration pulse test used to minimize self-heating effect.

The other low-leakage rectifying diodes has been tested was PMEG6020ELR. Since PMEG6020ELR only has 60 V VR reverse voltage rating, PMEG6020ELR can be only used when the application allows.

2.10 Optional Secondary Snubber

At the instant S1 closes, this reverse voltage applied to D1 can overshoot and ring before settling to $V_{D1,REV(D)}$ as given by Equation 27. A RC snubber can be used to limit the voltage stress across D1. Like the design of the optional primary snubber, a first order approximation for determining R8 and C8 is to set them to the characteristic impedance of the ringing caused by secondary side L_{lkg} of T1 and parasitic capacitance of D1.

$$R8 \sim = Z_{C8} \sim = \sqrt{\frac{L_{lkg,\mathrm{sec}}}{C_{D1}}}$$

Equation 28.

R8 can be determined by measuring L_{lkg} and ringing frequency:

$$R8 \sim = 2\pi f_{RING} L_{lkg,\mathrm{sec}}$$

Equation 29.

C8 can be set to the same impedance using:

$$C8 \sim = \frac{1}{2\pi f_{RING} R8}$$

Equation 30.

2.11 VSNS Voltage Divider

For the purpose of selecting sense resistors R5 and R6, the entire dc-dc converter can be modeled as a non-inverting amplifier as shown in Figure 2.5 Simplified V_{OUT} Gain Model on page 13. Notice that the non-inverting input, supply voltage (V+), and output voltage of the amplifier correspond to the internal 1.05 V reference, V_{IN}, and V_{OUT} of the dc-dc converter.

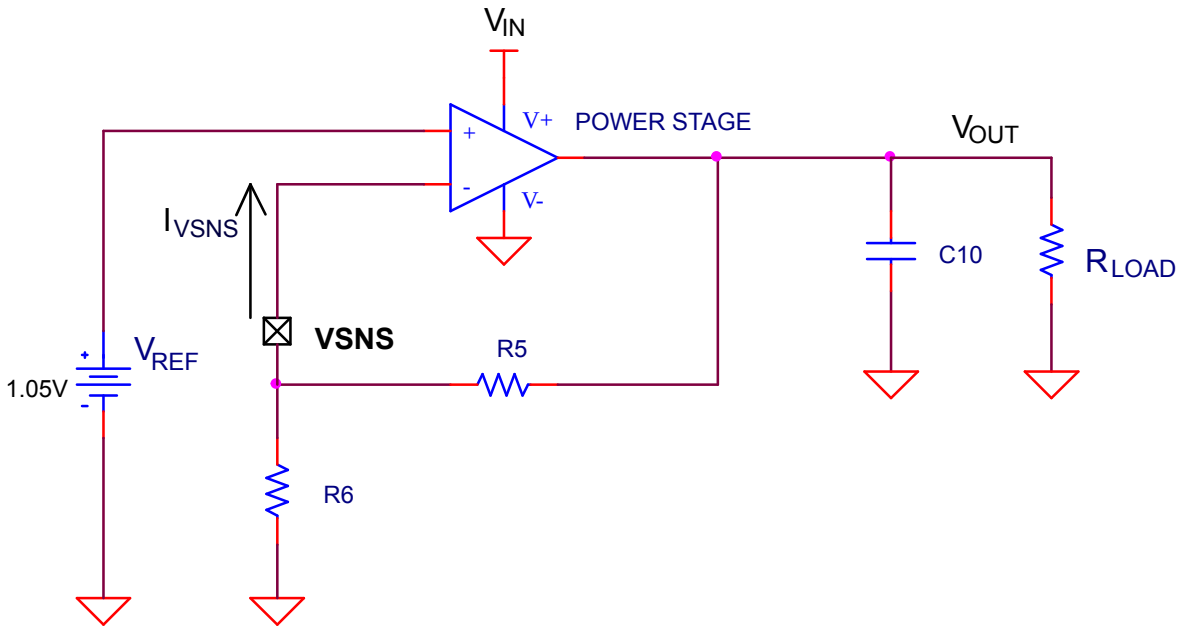


Figure 2.5. Simplified V_{OUT} Gain Model

Assuming infinite dc gain and applying KCL at the inverting input of the amplifier, V_{OUT} can be expressed by:

$$V_{OUT} = 1.05\left(\frac{R5}{R6} + 1\right) + R5 \times I_{VSNS}$$

Equation 31.

where I_{VSNS} represents the input offset current at VSNS pin. From Equation 31, it can be observed that a very large R5 could reduce the output voltage accuracy. In the Si8282/84 application, where the output may have positive and negative voltage rails, Equation 31 is still applicable, and the feedback output, Vout, is the sum of |VDDB| + |VSSB|.

3. Dynamic Response

The Si886xx/Si8284 start-up response consists of four regions of operation: Calibration, Soft-Start (SS), Proportional-Mode (P-Mode), and Proportional Integral Mode (PI-mode). The Si884xx/Si8282 has fixed switching frequency and soft-start behavior hence its dc-dc operation skips Calibration and begins with Soft-Start. Figure 3.1 V_{OUT} During Start Up on page 14 shows a typical V_{OUT} response during start up for the Si886xx operating at 500 kHz:

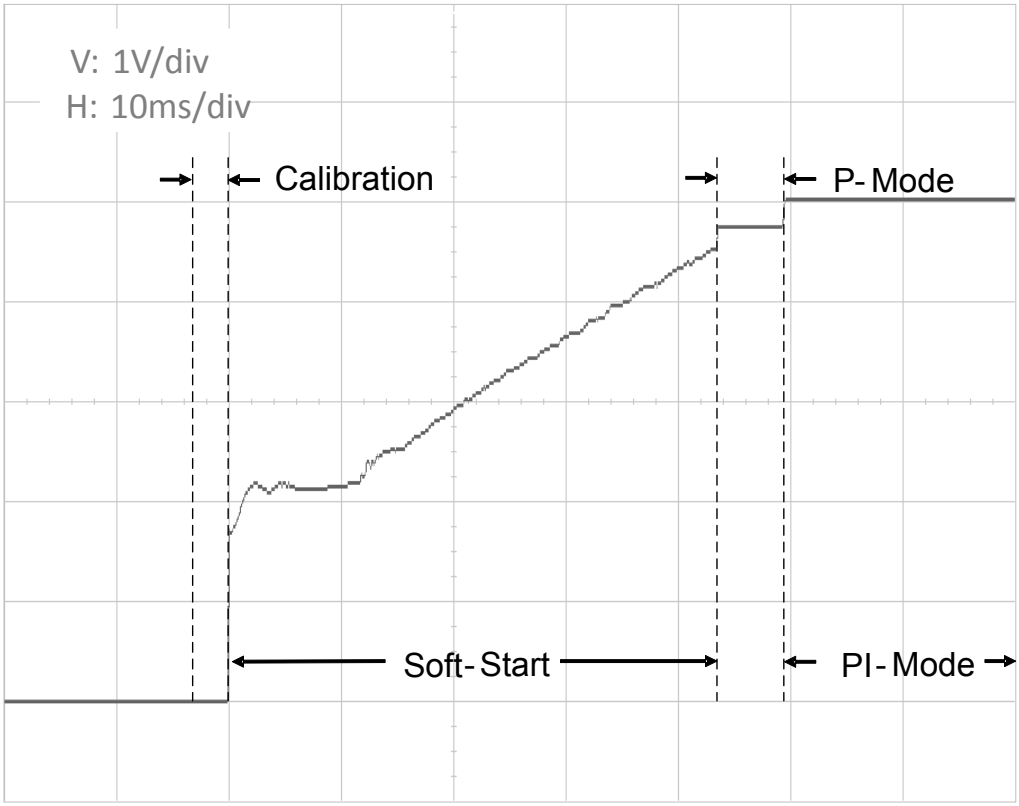


Figure 3.1. V_{OUT} During Start Up

3.1 External Soft-Start and Switching Frequency Calibration

The Si886xx/Si8284 has two additional external pins compared to Si884xx/Si8282 for setting switching frequency and adjusting soft start time, SH_FC and SS. The capacitor C6 is connected between pin SS and GNDA and sets the soft start time. The resistor R13 is connected between pin SH_FC and GNDA when the dc-dc is operating. Si886xx/Si8284 supports switching frequencies from 200 kHz to 900 kHz, and is set by:

$$T_{sw} = \frac{R13 \times C6}{1025.5}$$

Equation 32.

A practical C6 value for soft start is:

$$C6 = 470nF$$

Equation 33.

With C6 = 470 nF, R13 range to set acceptable T_{sw} is 2.42 kΩ to 10.9 kΩ. For any given T_{sw}, soft start time may be increased or decreased by increasing or decreasing C6 while adjusting R13 to maintain the same R13 x C6 time constant.

The time spent in calibration mode is approximately the time constant created by R13 and C6.

3.2 Soft Start

In soft start mode, the dc-dc peak current limit is gradually increased to limit the sudden demand of current needed from the primary supply. This mode of operation guarantees that V_{OUT} monotonically increases and minimizes the probability of a voltage overshoot. Once 90% of the final V_{OUT} is reached, soft start mode ends, and Proportional (P) Mode starts. The total duration of soft start is load dependent as it affects how many switching cycles are required for V_{OUT} to reach 90% of final value. In this mode of operation, the voltage feedback loop is inactive, and hence, loop stability is not a concern.

3.3 Proportional Mode

Once the secondary side senses 90% of V_{OUT}, the control loop begins its P-mode operation. During this mode of operation, the dc-dc converter closes the loop (dc-dc converter secondary side communicates with the primary side), and therefore, analyzing the loop stability is required.

Figure 3.2 Simplified Feedback Loop on page 16 shows a simplified block diagram of the dc-dc control feedback loop. gm_p represents the equivalent modulator and power stage transconductance of the dc-dc converter, and resistors R5 and R6 are the feedback resistors used to sense V_{OUT}. C10 is the output capacitor, and R_{LOAD} represents output load. Parameter gm_{fb} and $R_{o,gmfb}$ are the effective error amplifier transconductance and the error amplifier output resistance, respectively. During the P-Mode, an integrated resistor R_{INT} is connected to the COMP pin.

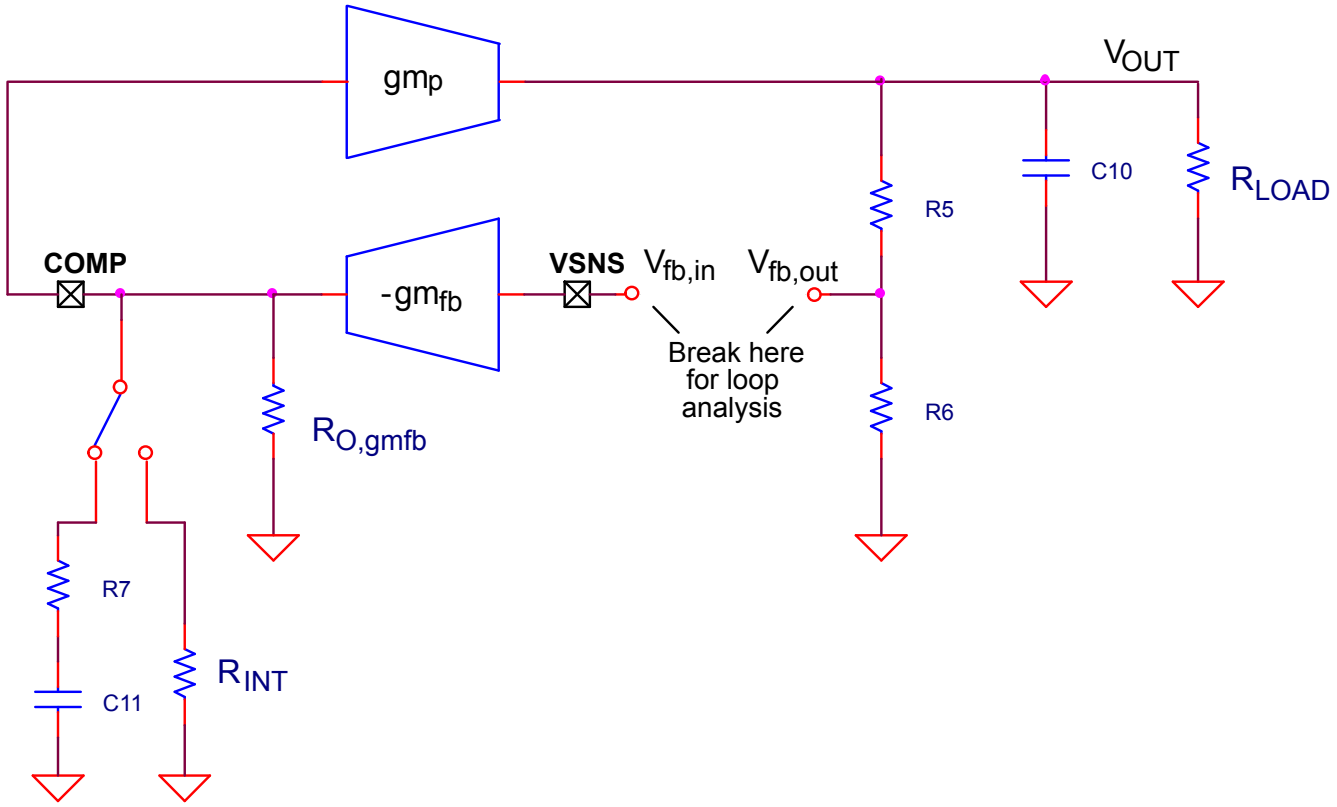


Figure 3.2. Simplified Feedback Loop

For stability analysis, the loop at the input of the error amplifier is broken to obtain the small-signal transfer function from $V_{fb,in}$ to $V_{fb,out}$:

$$H_p(s) = \frac{V_{fb,out}}{V_{fb,in}} = A_{DC,P}\frac{1}{1+\frac{s}{\omega_p}}$$

Equation 34.

$$\omega_p = \frac{1}{R_{load}C_{10}}$$

Equation 35.

$$A_{DC,P} = -\frac{R6}{R5+R6}gm_{fb}\left(R_{INT}\,||\,R_{o,gmfb}\right) \times gm_p\left(R_{LOAD}\,||\,\left(R5+R6\right)\right)$$

Equation 36.

$$gm_{fb} = \frac{1}{gm_{ea}\left(R5+R6\right)+1}$$

Equation 37.

gm_{ea} is the error amplifier transconductance. gm_{ea} ~= $1x10^{-3}$, R_{INT} ~= 100 kΩ for Si884xx/Si886xx (Rint ~= 200 kΩ for Si8282/Si8284), and $R_{O,gmfb}$ » R_{INT}. If R5 and R6 are chosen such that their parallel resistance is sufficiently larger than $1/gm_{ea}$, Equation 37 simplifies to:

$$gm_{fb} = \frac{1}{(R5 + R6)}$$

Equation 38.

gm_p is given by:

$$gm_P = \frac{n}{10 \times R12}$$

Equation 39.

Typically, R_{LOAD} « (R5 + R6) and the dc gain in P-mode simplifies to:

$$A_{DC,P} = -\frac{10x10^3 \times n \times R_{LOAD}}{R5}$$

Equation 40.

Notice that the dc gain of P mode is proportional to R_{LOAD} and inversely proportional to R5. At heavy loads (small R_{LOAD}), a very large R5 could significantly increase the output voltage error as the dc gain reduces. Conversely, a very small R5 increases power consumption and gm_{fb} variability due to higher dependency on gm_{ea}, which can significantly vary more than 1/(R5||R6) over temperature or from part to part. The total duration of this mode is approximately 7 ms.

3.4 Proportional Integral Mode

After P-mode, the controller switches to PI-mode, the steady state and final operation mode. During this mode of operation, the error amplifier drives an impedance that consists of the series combination of resistor R7 and capacitor C11. To achieve a smooth transition between P and PI modes, it is recommended to set R7 to match R_{INT}.

$$R7 = R_{INT}$$

Equation 41.

In PI-mode, the loop transfer is given by:

$$H_{PI}(s) = A_{DC,PI}\frac{\left(1+\frac{s}{\omega_{z1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\times\left(1+\frac{s}{\omega_{p2}}\right)}$$

Equation 42.

where:

$$\omega_{p1} = \frac{1}{R_{o,gmfb}\times C11}$$

Equation 43.

$$\omega_{z1} = \frac{1}{R7\times C11}$$

Equation 44.

$$\omega_{p2} = \frac{1}{R_{LOAD}\times C10}$$

Equation 45.

$$A_{DC,PI} = -\frac{R_{o,gmfb}gm_pR_{LOAD}}{R5}$$

Equation 46.

Notice that the loop transfer function in PI-Mode has an additional pole-zero pair when compared with P-Mode. In addition, the loop dc gain is much higher in PI-Mode than in P-Mode due to $R_{O,gmfb} \gg R_{INT}$.

Figure 3.3 Simplified Bode Magnitude Plot of the Loop in PI Mode on page 19 shows the magnitude Bode plot of the loop in PI mode.

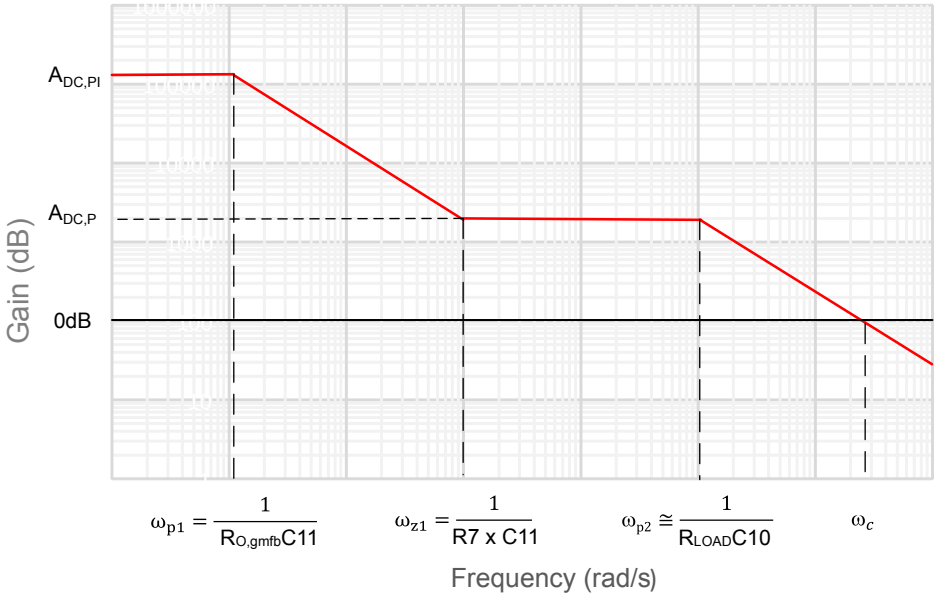


Figure 3.3. Simplified Bode Magnitude Plot of the Loop in PI Mode

4. Design Example 1: Si886xx

Consider the desired requirements listed in Table 4.1 Design Requirements on page 20.

Table 4.1. Design Requirements

Parameter	Value
Input Voltage	24.0 V
Output Voltage	5.0 V
Input Voltage Ripple	≤ 50 mV
Output Voltage Ripple	≤ 50 mV
Maximum Output Current	1 A

4.1 Transformer Design

For this example, operating in CCM was chosen. Equation 7. establishes the relationship between turns ratio n and duty cycle D. Accounting for forward voltage drop across D1 of 0.5 V and targeting a duty cycle of 40%, Equation 7. can be solved for transformer turns ratio n:

$$n\sim = \frac{V_{IN} \times D}{(V_{OUT} + Vf_{D1})(1 - D)}\sim = \frac{24 \times 0.4}{5.5 \times 0.6}\sim = 2.91$$

Equation 47.

A 3:1 turns ratio was chosen.

The next parameters to choose are the switching period and primary inductance. The Si886xx has externally set switching frequency range of 200 kHz to 900 kHz. 500 kHz was chosen for this example. C6 is set to 470 nF and R13 is calculated by rearranging Equation 32:

$$R13 = \frac{1025.5 \times T_{sw}}{C6} = \frac{1025.5 \times 2x10^{-6}}{470x10^{-9}} = 4.36k\Omega$$

Equation 48.

R13 was set to 4.32 kΩ as that is the closest 1% resistor value.

To determine L_m, consider at what minimum load should the converter operate in CCM. For this design, it was targeted to operate in CCM between 70% and full load. At the cross-over point between DCM and CCM:

$$Im_{AVE,XOVR} = \frac{Im_{RIPPLE}}{2}$$

Equation 49.

Substituting,

$$\frac{0.7 \times I_{LOAD}}{n(1 - D)} = \frac{V_{IN} D T_{sw}}{2L_m}$$

Equation 50.

And solving for L_m:

$$L_m = \frac{nV_{IN}D(1 - D)T_{sw}}{1.4 \times I_{LOAD}} = \frac{3 \times 24 \times 0.4 \times 0.6 \times 2x10^{-6}}{1.4} = 24.7uH$$

Equation 51.

A transformer with turns ratio of 3:1 and primary inductance of 25 µH was chosen.

4.2 R12 Sense Resistor Selection

When the voltage on the RSNS pin exceeds 100 mV, the SI8284x dc-dc controller terminates the dc-dc switching cycle early to provide overcurrent protection to the external MOSFET. Each time the ESW pin turns on the external MOSFET, the dc-dc controller monitors the RSNS pin for an overcurrent condition. When the voltage on the RSNS pin goes above 100 mV, the dc-dc controller shuts down the external MOSFET and waits for the next switching cycle. If the short circuit condition persists over many switching cycles, the output voltage collapses due to low duty cycle from the repeated early shut down. When the output voltage goes below the output target voltage (set by the resistor divider on the VSNS pin), the dc-dc controller initiates a restart sequence. In the restart sequence, the converter stays in the off state for 21 seconds before resuming operation. The user can adjust the current limit by selecting the value of the external RSENSE resistor.

R12 is chosen to provide a cycle by cycle current limit. Equation 10. gives the average magnetizing current at specified load.

Magnetizing Current

$$Im_{AVE} = \frac{I_{LOAD}}{n(1-D)} = \frac{1}{3 \times 0.6} = 556mA$$

Equation 52.

The peak current in CCM is:

$$I_{m,PK,RCM} = I_{m,AVE} + \frac{V_{IN} D T_{sw}}{2L_m} = 0.556 + \frac{24 \times 0.4 \times 2 \times 10^{-6}}{2 \times 25 \times 10^{-6}} = 0.94A$$

Equation 53.

Allowing for some variation in performance from design calculations, 1 A current limit is chosen. Applying Equation 13 and calculating for R12:

$$R12 = \frac{100mV}{I_{m,LIMIT}} = \frac{0.1}{1} = 100\,\text{m}\Omega$$

Equation 54.

Figure 4.1 Magnetizing Current on page 22 shows the expected magnetizing current waveform at specified load.

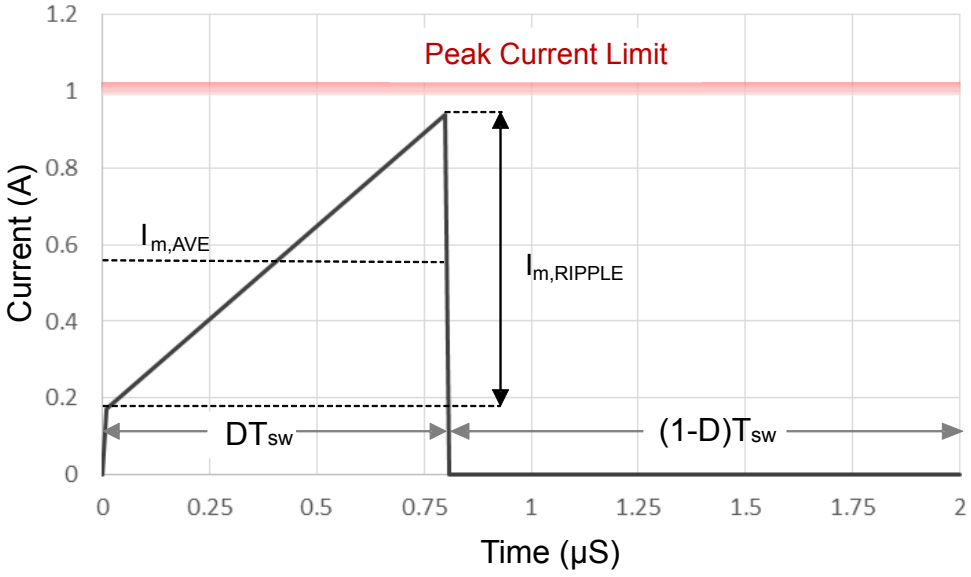


Figure 4.1. Magnetizing Current

4.3 Q1 Selection

The instant S1 opens, Q1's drain voltage increases rapidly from nearly 0 V and settles to:

$$V_{ds1,(1-D)} = V_{IN} + n\left(V_{OUT} + V_{fD1}\right) = 24 + 16.5 = 40.5V$$

Equation 55.

However, energy stored in L_{lkg} must be dissipated in the secondary which causes $V_{ds,(D)}$ to spike a higher voltage. Q1 must be able to tolerate this voltage spike between drain and source.

A N-channel MOSFET with 100 V rating was chosen to accommodate the expected voltage stress caused by L_{lkg}

4.4 D1 Selection

Equation 25. through Equation 27. define the requirements for D1. Substituting into Equation 25.,

$$I_{D1,AVE} = I_{LOAD} = 1A$$

Equation 56.

Diode current capacities are specified in rms. Assuming a linear current through D1, consider the translation of average to rms:

$$I_{D1,RMS} = I_{D1,AVE}\left(\frac{2}{\sqrt{3}}\right) = 1.15A$$

Equation 57.

Substituting into Equation 27:

$$V_{D1,REV(D)} = \frac{V_{IN}}{n} + V_{OUT} = \frac{24}{3} + 5 = 13V$$

Equation 58.

Equation 27 does not include the voltage spike due to the interaction of the diode capacitance and secondary side leakage inductance, and as a result, a diode with a larger withstanding voltage is required in practice.

When selecting D1, diodes with low V_f are the preferred choice as it minimizes the associated power loss.

$$P_{D1} = Vf_{D1} \times I_{D1,AVE}$$

Equation 59.

Several diodes were tested in the circuit. A 5 A, 50 V diode was chosen for more tolerance. For high operating temperature, diode leakage and package heat transfer characteristics affect overall performance and efficiency. Please note that the low leakage diode is required for high working temperature applications. Please refer to 2.9 Diode and Output Capacitor and Table 2.1 DC-DC Supply Output Rectifier Diode for High Working Temperatures on page 11 for more details.

4.5 External Regulator Circuit

For this design, an external regulator circuit was designed to work with the VREGA voltage reference to create a regulated supply for VDDA. R14 was selected for a 950 µA sink current.

$$R14 = \frac{V_{IN} - V_{REGA}}{I_R} = \frac{24 - 4.85}{0.001} = 19.5k\Omega$$

Equation 60.

R14 was set to 19.6 kΩ and C14 to the recommended 0.1 µF. MMBT2222 was selected for Q2.

4.6 C10 Selection

C10 is inversely proportional to output voltage ripple and sets the crossover frequency of control loop gain. Solving Equation 22,

$$C10 = \frac{I_{LOAD} DT_{sw}}{V_{OUT,RIPPLE}} \geq \frac{1 \times 0.4 \times 2 \times 10^{-6}}{0.05} \geq 16uF$$

Equation 61.

Capacitor current in rms is given by:

$$I_{rmsC10} = I_{LOAD}\sqrt{\frac{D}{1-D}} = 1 \times \sqrt{\frac{0.4}{0.6}} = 0.81A$$

Equation 62.

A 22 µF X7R capacitor in 1210 package was chosen.

4.7 C2 Selection

In most applications, V_{IN} also supplies the VDDA pin that powers the dc-dc controller and the primary side digital isolator circuitry. It is recommended to minimize voltage ripple at VDDA. Solving Equation 18:

$$C_2 \geq \frac{I_{m,RIPPLE} DT_{sw}}{2 \cdot V_{IN,RIPPLE}} \geq \frac{0.768 \times 0.4}{2 \times 0.05 \times 500 \times 10^3} \geq 6.14\mu F$$

Equation 63.

The magnetizing ripple current is 0.768 A by Equation 9.

A 10 µF X7R capacitor in 1210 package was chosen.

4.8 R5 and R6 Selection

The ratios of R5 and R6 are determined by the 5 V output voltage requirement. To reduce the dependence of feedback gain on the internal error amplifier transconductance, it is recommended to have the parallel combination resistance to be ≥10 kΩ. Higher values of R5 and R6 reduce power loss through the divider, but at the expense of increasing output voltage error due to I_{VSNS}, which varies part to part. So R5 and R6 are chosen to target 10 kΩ parallel resistance.

$$10 \times 10^3 = \frac{R5 \times R6}{R5 + R6}$$

Equation 64.

$$5 = 1.05\left(\frac{R5}{R6} + 1\right)$$

Equation 65.

Substituting Equation 65 into Equation 64 and solving for R6,

$$10x10^3 = \frac{3.76 \times R6}{4.76},\ R6 = 12.66x10^3,\ R5 = 48.1x10^3$$

Equation 66.

The nearest 1% resistor to 12.66 kΩ is 12.7 kΩ. However, setting R5 to either 47.5 kΩ or 48.7 kΩ does not target exactly 5 V as well as other 1% resistor pairs. A better match was found with R6 = 13.3 kΩ and R5 = 49.9 kΩ.

4.9 Compensation Network

The compensation network is comprised of R7 and C11. R7 is fixed to 100 kΩ to match the Si884xx/6xx internal compensation R_{INT}. That leaves the C11 as the main parameter to place the compensation zero in relationship to the crossover frequency to ensure the loop stability. Below is the equation for estimating the dc-dc crossover frequency:

$$f_c \sim = \frac{100 \times 10^3 \times 3 \times n \times R_{LOAD}}{R_5} \times \frac{1}{2\pi \times R_{LOAD} \times C_{10}}$$

$$= \frac{100 \times 10^3 \times 3 \times 3}{49.9 \times 10^3} \times \frac{1}{2\pi \times 22 \times 10^{-6}} = 130.5 \quad kHz$$

Equation 67.

To achieve good phase margin, it is suggested to place the zero between 1/4th to 1/10th of the estimated crossover frequency. The zero placement in the equation below was chosen to lead the crossover frequency by a factor of 6:

$$C_{11} = \frac{6}{2\pi \times f_c \times R_7} = \frac{6}{2\pi \times 130.5 \times 10^3 \times 100 \times 10^3} = 0.073 \quad nF$$

Equation 68.

Even though the calculation suggested only 0.073 nF capacitor is required, it is common to use C11 $\geq$ 1.5 nF and thus 1.5 nF was chosen.

4.10 Primary Snubber

Without R19 and C16 installed, V_{ds} of Q1 was measured to spike at 108 V and ring briefly at 30 MHz until the energy stored in L_{lkg} dissipated. See Figure 4.2 Undamped Vds Ringing on page 26:

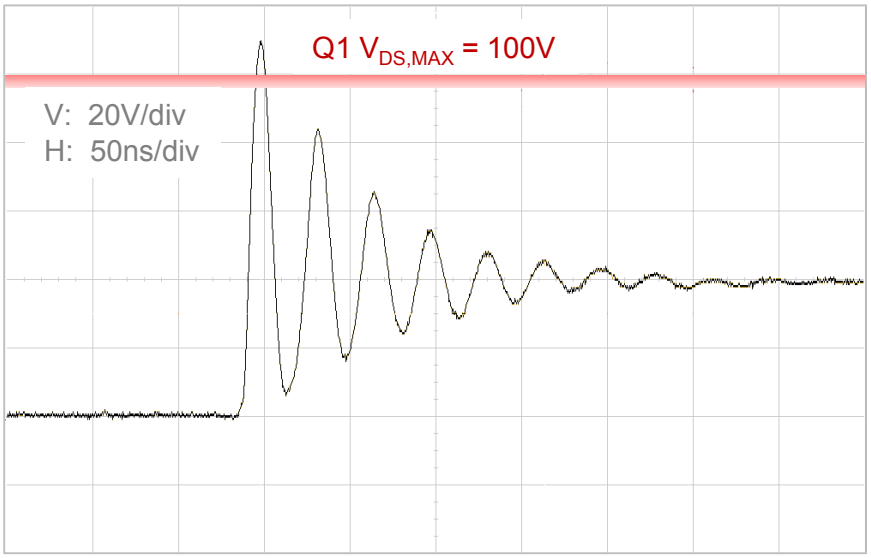


Figure 4.2. Undamped Vds Ringing

T1 was removed from the board and its primary inductance leakage was measured to be 456 nH. Applying Equation 16 and Equation 17, R16 and C19 were calculated:

$$R16 = 2\pi f_{ring} L_{lkg} = 2\pi \times 30x10^{6} \times 456 \times 10^{-9} = 86\Omega$$

Equation 69.

$$C19 = \frac{1}{2\pi f_{ring} R16} = \frac{1}{2\pi \times 30 \times 10^{6} \times 86} = 62pF$$

Equation 70.

Closest standard component values of R16 = 82 Ω and C19 = 68 pF were selected and installed. Q1 Vds was measured again to gage effectiveness of the RC snubber. Voltage spike was reduced to 74 V as shown in Figure 4.3 Damped Vds Ringing on page 27.

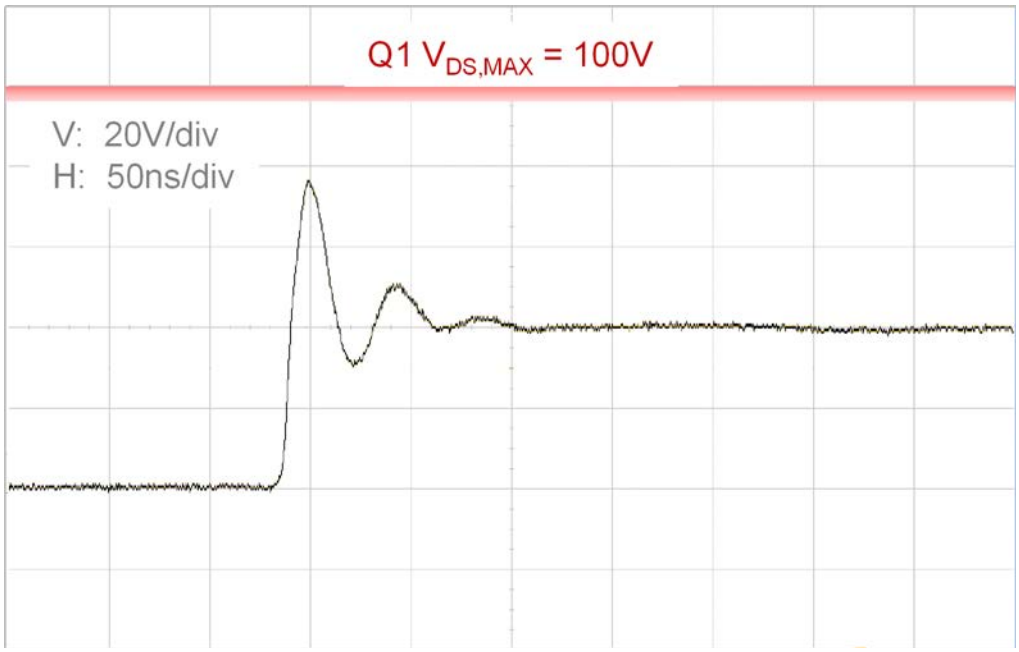


Figure 4.3. Damped Vds Ringing

R8 and C8 on the secondary side can be selected using the same methodology. Without a secondary side snubber, the voltage spike across D1 at the instant that S1 closes was measured to be 35 V with a ringing frequency of 59 MHz. T1 was removed from the board and its primary inductance leakage was measured to be 74 nH.

$$R8 = 2\pi f_{ring} L_{lkg} = 2\pi \times 59 \times 10^{6} \times 74x10^{-9} = 27.4\Omega$$

Equation 71.

$$C8 = \frac{1}{2\pi f_{ring} R8} = \frac{1}{2\pi \times 59 \times 10^{6} \times 27.4} = 98.4pF$$

Equation 72.

R8 is a 1% resistor value and C8 of 100 pF was chosen. The voltage spike was reduced to 23 V and the ringing damped.

4.11 Design Summary

The table below shows the component selection that meets design requirements.

Table 4.2. Ordering Guide

Part Reference	Description	Manufacturer	Manufacturer Part Number
C2	CAP, 10 µF, 50 V, ±20%, X7R, 1210	Venkel	C1210X7R500-106M
C6	CAP, 0.4 µF, 16 V, ±10%, X7R, 0805	Venkel	C0805X7R160-474K
C8	CAP, 100 pF, 50 V, ±10%, X7R, 0603	Venkel	C0603X7R500-101K
C10	CAP, 22 µF, 25 V, ±10%, X7R, 1210	Venkel	C1210X7R250-226M
C11	CAP, 1.5 nF, 25 V, ±10%, X5R, 0603	Venkel	C0603X5R250-152K
C14	CAP, 0.1 µF, 10 V, ±10%, X7R, 0603	Venkel	C0603X7R100-104K
C19	CAP, 68 pF, 100 V, ±10%, C0G, 0603	Venkel	C0603C0G101-680K
D1	DIO, SUPER BARRIER, 50 V, 5.0 A, SMA	Diodes Inc.	SBRT5A50SA
D8	DIO, SINGLE, 100V, 300mA, SOD123	Diodes Inc.	1N4148W-7-F
Q1	TRANSISTOR, MOSFET, N-CHNL, 100 V, 3.7 A, 3 W,Switching, SOT223	Fairchild	FDT3612
Q2	TRANSISTOR, NPN, 30V, 600mA, SOT23	On Semi	MMBT2222LT1
Q3	TRANSISTOR, MOSFET, N-CHNL, 50V, 200mA, 360mW Small signal, SOT23	Diodes Inc.	BSS138
R5	RES, 49.9 KΩ, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-4992F
R6	RES, 13.3 KΩ, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1332F
R7	RES, 100 KΩ, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1003F
R8	RES, 27.4 Ω, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-27R4F
R12	RES, 0.1 Ω, 1/2 W, ±1%, ThickFilm, 1206	Venkel	LCR1206-R100F
R13	RES, 4.32 KΩ, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-4321F
R14	RES, 19.6 KΩ, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1962F
R16	RES, 82.0 Ω, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-82R0F
R17	RES, 20 Ω, 1/4W, ±1%, ThickFilm, 1206	Venkel	CR1206-4W-20R0FT
R18	RES, 10KΩ, 1/10W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1002F
R19	RES, 10KΩ, 1/10W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1002F
T1	TRANSFORMER, Flyback, 25 µH Primary, 500 nH Leak- age, 3:1, SMT	UMEC	UTB02205s
U1	IC, ISOLATOR, dc-dc External Switch, Freq Control, 2 Digital Ch, SO20 WB	Silicon Labs	Si88621ED-IS

5. Design Example 2: Si8284 EVB

Consider the desired requirements listed in the table below. Please refer to Figure 1.2 Typical Isolated Flyback Converter Circuit Using an Si8284 Isolated Gate Driver on page 3 for the application circuit.

Table 5.1. Si8284 EVB Design Requirements

Parameter	Value
Input Voltage	24.0 V
Output Voltage	VDDB = 15.0 V and VSSB = –9.0 V
Input Voltage Ripple	≤ 150 mV (RMS)
Output Voltage Ripple	≤ 150 mV (RMS)
Maximum Output Current	1/12 A

5.1 Transformer Design

Unlike the previous example, the ISOdriver does not require the large average output power so the operation in DCM was chosen. The Si8284 has externally set switching frequency range from 200 kHz to 900 kHz. 250 kHz was chosen for this example. C6 was chosen to be 220 nF.

$$R13 = \frac{1025.5 \times T_{SW}}{C6} = \frac{1025.5}{220 \times 10^{-9} \times 250 \times 10^{3}} = 18.6k\Omega$$

Equation 73.

R13 was set to 18.7 kΩ as that is the closest 1% resistor value.

Equation 8 establishes the relationship between the duty cycle D and the transformer primary inductance. Equation 8 can be rearranged for transformer primary inductance:

$$L_m = \frac{D^2 \times R_{LOAD} \times T_{SW}}{2}\left(\frac{V_{IN}}{V_{OUT}}\right)^2$$

Equation 74.

where Vout can be treated as |VDDB| + |VSSB|.

Accounting for forward voltage drop across D1/D2 of 0.5 V and targeting a duty cycle of 20~25% at the rated load,

$$L_m = \frac{D^2 \times (25 \times 12)}{2 \times 250K}\left(\frac{24}{25}\right)^2 = 552.96 \times D^2[\,\mu H]$$

Equation 75.

Substituting D = 0.2~0.25,

$$22.11\,\mu H \le L_m \le 34.56\,\mu H$$

Equation 76.

25 µH transformer primary inductance was chosen near the lower end of the acceptable inductance range so that we can guarantee the DCM operation when the V_{IN} drops below the rated 24 V voltage level. With 25 µH transformer inductance, the steady state duty cycle becomes 21.26%.

In DCM operation, the transformer primary to secondary turn ratio doesn't affect the converter duty cycle and transformer primary peak current. Based on the desired input and output voltage range, we want the turn ratio to be less than 1. In this way, the MOSFET Vds rating can be limited to a lower level. The larger the reciprocal of the transformer turn ratio, the lower the converter output ripple. On the other hand, a very large value for the reciprocal of the transformer turn ratio makes the converter tends to enter the CCM operation. When Lm is fixed, the turn ratio to maintain the converter to operate in the DCM is

$$\frac{1}{n} < \frac{(1 - D)}{2L_m} \times \frac{V_{IN}}{I_{LOAD}} \times D \times T_{SW}$$

Equation 77.

If we want to maintain the DCM operation when V_{IN} drops to 50% of the rated V_{IN} voltage, from Equation 8, the duty cycle will be increased to

$$D_{half\_Vin} = \frac{V_{OUT}}{V_{IN}}\sqrt{\frac{2L_m}{R_{LOAD}T_{SW}}} = \frac{25}{12}\sqrt{\frac{2 \times 25 \times 10^{-6} \times 250 \times 10^{3}}{300}} = 0.4253$$

Equation 78.

Substituting this duty cycle to Equation 77,

$$\frac{1}{n} < \frac{(1 - 0.4253)}{2 \times 25 \times 10^{-6}} \times \frac{12 \times 12 \times 0.4253}{250 \times 10^{3}} = 2.82$$

Equation 79.

Thus, a 1:2 primary to secondary turns ratio was chosen. In this design, the secondary winding is split to obtain two output taps with the ratio of 15:9.

5.2 R12 Sense Resistor Selection

The selection of R12 is based on the expected transformer switching peak current plus certain margin. From Equation 12, in DCM operation, the peak magnetizing current is equal to the ripple current. By Equation 9, the peak magnetizing current with 25 µH transfer inductance and 250 kHz switching frequency is:

$$I_{m,RIPPLE} = \frac{V_{IN} D T_{SW}}{L_m} = \frac{24 \times 0.2126}{25 \times 10^{-6} \times 250 \times 10^{3}} = 816.4mA$$

Equation 80.

Allowing for some variation in performance from design calculations, 1 A current limit is chosen. Applying Equation 13 and calculating for R12:

$$R_{12} = \frac{100mV}{I_{m,LIMIT}} = \frac{0.1}{1} = 100m\Omega$$

Equation 81.

5.3 Q1 Selection

The instant Q1 opens, Q1's drain voltage increases rapidly from nearly 0 V and settles to:

$$V_{ds1,(1-D)} = V_{IN} + n\left(V_{OUT} + V_{fD1} + V_{fD2}\right) = 24 + 0.5(24 + 0.5 + 0.5) = 36.5V$$

Equation 82.

However, energy stored in L_{lkg} must be dissipated which causes MOSFET drain-source voltage to a higher spike. Q1 must be able to tolerate this voltage spike between drain and source.

A N-channel MOSFET with 100 V rating was chosen to accommodate the expected voltage stress caused by L_{lkg}.

5.4 D1 and D2 Selection

Equation 25 through Equation 27 define the requirements for D1 and D2. From Equation 25, the diode average current is equal to the converter output current. Diode current capacities are specified in rms. Assuming a linear current through D1/D2, consider the translation of average to rms:

$$I_{D1/D2,RMS} = I_{D1/D2,AVE} \times \left(\frac{2}{\sqrt{3}}\right) = 96.2mA$$

Equation 83.

From Equation 27:

$$V_{D1/D2,REV(D)} = \frac{V_{IN}}{n} + V_{OUT} = \frac{24}{0.5} + 24 = 72V$$

Equation 84.

Equation 27 does not include the voltage spike due to the interaction of the diode capacitance and secondary side leakage inductance, and as a result, a diode with a larger withstanding voltage is required in practice.

When selecting D1, diodes with low Vf are the preferred choice as it minimizes the associated power loss.

$$P_{D1/D2} = V_f \times I_{D1/D2,AVE}$$

Equation 85.

Several diodes were tested in the circuit. The 1 A, 100 V diode was chosen to obtain more tolerance. For high operating temperature, diode leakage and package heat transfer characteristics affect overall performance and efficiency. Please note that the low leakage diode is required for high working temperature application. Please refer to 2.9 Diode and Output Capacitor and Table 2.1 DC-DC Supply Output Rectifier Diode for High Working Temperatures on page 11 for more detail.

5.5 External Regulator Circuit

For Si8284 EVB design, an external linear regulator circuit was designed to work with the external 5.6 V Zener diode to create a regulated supply for VDDA. R14 was selected for a 950 µA sink current. This regular circuit is intended to operate between Vin = 12~24 V. Considering the operation of the Zener regulator at 90% of 12 V Vin,

$$R_{14} = \frac{V_{IN} - V_{ZENER}}{0.001} = \frac{10.8 - 5.6}{0.001} = 5.2k\Omega$$

Equation 86.

R14 was set to 5.1 kΩ and C14 was set to the recommended 0.1 µF. MMBT2222 was selected for Q2.

5.6 C10 and C20 Selection

C10 in series with C20 are the output capacitors at the converter output. Their equivalent capacitance is inversely proportional to output voltage ripple and sets the crossover frequency of control loop gain. Solving Equation 24:

$$C_{10} + C_{20} = \frac{I_{LOAD} T_{SW}}{V_{OUT,RIPPLE}}\left(1 - \frac{DV_{IN}}{nV_{OUT}}\right) \geq \frac{1}{12 \times 0.15 \times 250 \times 10^3}\left(1 - \frac{0.2126 \times 24}{0.5 \times 25}\right) \geq 1.3\ \mu F$$

Equation 87.

The 10 µF X7R capacitor in a 1210 package was chosen for C10 and C20. The series capacitance is 5 µF, which gives more margin than the 1.3 µF requirement.

Even though C10 and C20 exist, in Si828x iso-driver application, the large bypass capacitors at the driver VDDB/VSSB supply pins are still required. The typical bypass capacitor at the VDDB/VSSB driver supply pins is 0.1 µF in parallel with 4.7 µF.

5.7 C2 Selection

In most applications, VIN also supplies the VDDA pin that powers the dc-dc controller and the primary side digital isolator circuitry. It is recommended to minimize voltage ripple at VDDA. Substituting Equation 80 into Equation 18:

$$C_2 \geq \frac{I_{m,RIPPLE} \times D \times T_{SW}}{2 \times V_{IN,RIPPLE}} \geq \frac{0.816 \times 0.2126}{2 \times 0.15 \times 250 \times 10^3} \geq 2.3\ \mu F$$

Equation 88.

A 10 µF X7R capacitor in 1210 package was chosen.

5.8 R5 and R6 Selection

The ratios of R5 and R6 are determined by the 24 V output voltage requirement. To reduce the dependence of feedback gain on the internal error amplifier transconductance, it is recommended to have the parallel combination resistance to be ≥10 kΩ. Higher values of R5 and R6 reduce power loss through the divider, but at the expense of increasing output voltage error due to I_{VSNS}, which varies part to part. So R5 and R6 are chosen to target 10 kΩ parallel resistance.

$$10 \times 10^3 \approx \frac{R5 \times R6}{R5 + R6}$$

Equation 89.

$$24 = 1.05\left(\frac{R5}{R6} + 1\right)$$

Equation 90.

Substituting Equation 90 into Equation 89 and solving for R6:

$$10 \times 10^3 = \frac{21.86 \times R6}{22.86}, \quad R6 = 10.45 \times 10^3, \quad R5 = 228.6 \times 10^3$$

Equation 91.

The 228 kΩ is the relatively large resistor and increases the sensitivity to I_{VSNS}. R6 = 8.66 kΩ and R5 = 182 kΩ were selected as the compromise between the output voltage accuracy and the extra power consumption.

5.9 Compensation Network

The compensation network is comprised of R7 and C11 connecting between COMP pin and VSSB. R7 is fixed to 200 kΩ to match the Si8282/84 internal compensation R_{INT}. That leaves the C11 as the main parameter to place the compensation zero in relationship to the crossover frequency to ensure the loop stability. Below is the equation for estimating the dc-dc crossover frequency:

$$f_C \sim = \frac{200 \times 10^3 \times 3 \times n \times R_{LOAD}}{R_5} \times \frac{1}{2\pi \times R_{LOAD} \times C_{10\text{-}20}}$$

$$= \frac{200 \times 10^3 \times 3 \times 0.5}{182 \times 10^3} \times \frac{1}{2\pi \times 5 \times 10^{-6}} = 52.5kHz$$

Equation 92.

To achieve good phase margin, it is suggested to place the zero between 1/4th to 1/10th of the estimated crossover frequency. The zero placement in the equation below was chosen to lead the crossover frequency by a factor of 6:

$$C_{11} = \frac{6}{2\pi \times f_C \times R_7} = \frac{6}{2\pi \times 52.5 \times 10^3 \times 200 \times 10^3} = 0.09 \quad nF$$

Equation 93.

Even though the calculation suggested only 0.09 nF capacitor is required, it is common to use C11 $\geq$ 1.5 nF and thus 1.5 nF was chosen.

5.10 Primary and Secondary Snubber

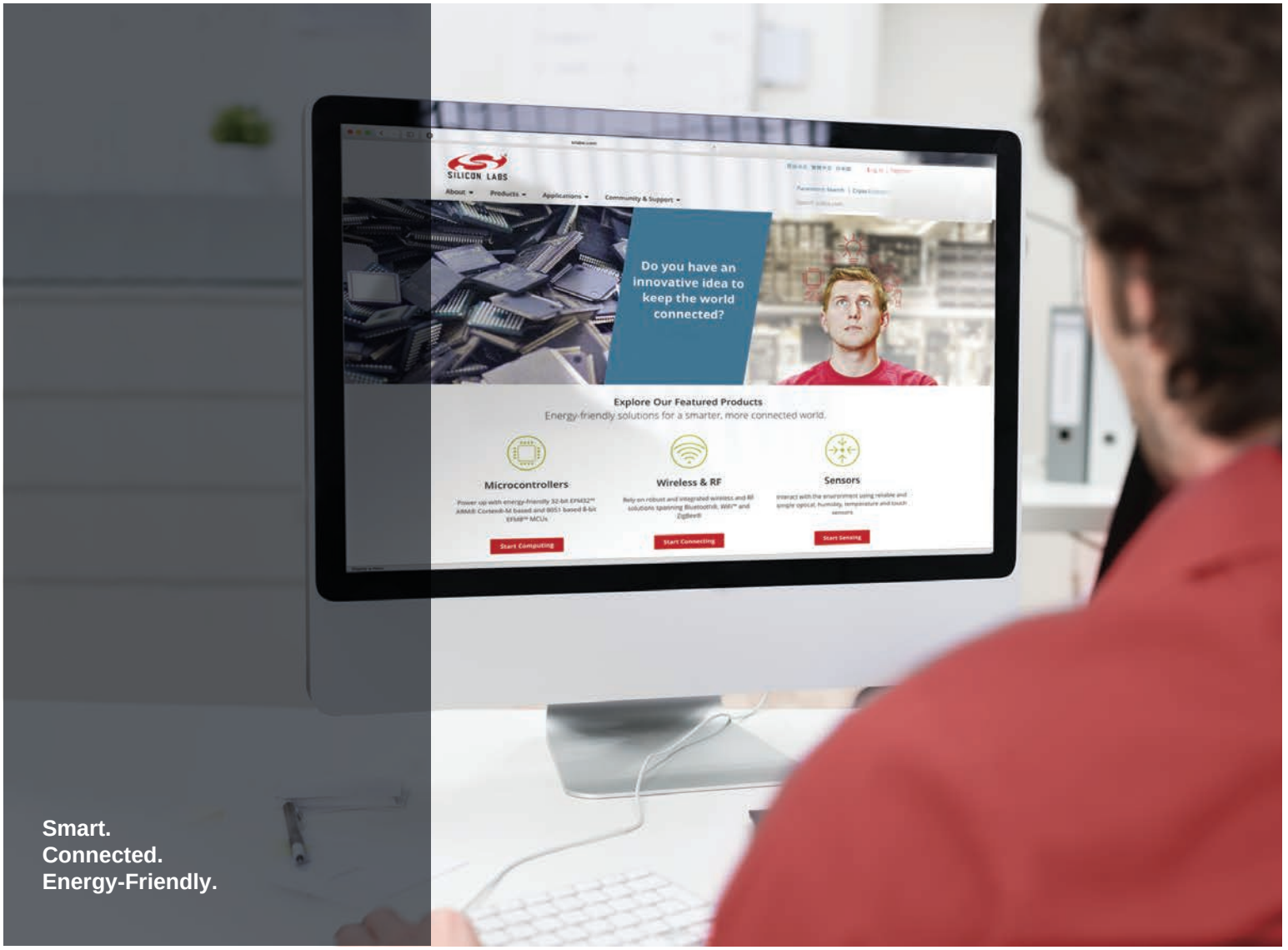
The procedure to determine primary and secondary snubber components are similar with the previous example. The detail was skipped here. R16=100 Ω, C19=100 pF, R8=100 Ω, and C8=100 pF were selected and installed.

5.11 Design Summary

The following table shows the component selection that meets design requirements.

Table 5.2. Si8284 EVB Converter Bill of Materials

Part Reference	Description	Manufacturer	Manufacturer Part Number
C1	0.1 µF 50 V ±10% X7R 0805	Venkel	C0805X7R500-104K
C2	10 µF 50 V ±20% X7R 1210	Venkel	C1210X7R500-106M
C6	0.22 µF 25 V ±10% X7R 0603	Venkel	C0603X7R250-224K
C8	100 pF 50 V ±20% C0G 0603	Venkel	C0603C0G500-101M
C10	10 µF 50 V ±20% X7R 1210	Venkel	C1210X7R500-106M
C11	1.5 nF 25 V ±10% X7R 0603	Venkel	C0603X5R250-152K
C14	0.1 µF 10 V ±10% X7R 0603	Venkel	C0603X7R100-104K
C19	100 pF 50 V ±20% C0G 0603	Venkel	C0603C0G500-101M
C20	10 µF 50 V ±20% X7R 1210	Venkel	C1210X7R500-106M
C21	0.1 µF 50 V ±10% X7R 0805	Venkel	C0805X7R500-104K
C22	0.1 µF 50 V ±10% X7R 0805	Venkel	C0805X7R500-104K
D1	Diode 1 A 100 V Schottky SOD-123	On Semi	MBR1H100SF
D2	Diode 1 A 100 V Schottky SOD-123	On Semi	MBR1H100SF
D4	Zener 5.6 V 200 mW 7% SOD-323	Diodes Inc.	BZT52C5V6S-F-7
Q1	MOSFET 3.7 A 100 V N-Channel SOT223	Fairchild	FDT3612
Q2	BJT Transistor 600 mA 30 V NPN SOT23	On Semi	MMBT2222LT1
R5	182 kΩ 1/10 W ±1% ThickFilm 0603	Venkel	CR0603-10W-1823F
R6	8.66 kΩ 1/16 W ±1% ThickFilm 0603	Venkel	CR0603-16W-8661F
R7	200 kΩ 1/10 W ±1% ThickFilm 0603	Venkel	CR0603-10W-2003F
R8	100 Ω 1/10 W ±1% ThickFilm 0603	Venkel	CR0603-10W-1000F
R12	0.1 Ω 1/2 W ±1% ThickFilm 1206	Venkel	LCR1206-R100F
R13	18.7 kΩ 1/16 W ±1% ThickFilm 0603	Venkel	CR0603-16W-1872F
R14	5.1 kΩ ¼ W ±1% ThickFilm 0805	KOA Speer Electronics, Inc.	RK73H2ATTD5101F
R16	100 Ω 1/10 W ±1% ThickFilm 0603	Venkel	CR0603-10W-1000F
R18	10 kΩ 1/10 W ±1% ThickFilm 0603	Venkel	CR0603-10W-1002F
T2	Transformer 25 µH 1.4A 1:1.25:0.75 SMT	Coilcraft	TA7788-AL
U2	ISOdriver, DCDC external switch, frequency control, WB SOIC24	Silicon Labs	Si8284CD-IS



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