

EXTERNAL REFERENCES: OPTIMIZING PERFORMANCE

1. Introduction

Devices include:

- Si534x
- Si5380
- Si539x

The Si5341/2/4/5/6/7 and Si5380 each have XA/XB inputs, which are used to generate low-phase-noise references and are an integral part of the PLL, as shown in Figure 1. Silicon Labs recommends using a crystal as a low-cost, high-performance option for the XA/XB input; however, a crystal oscillator can also be used. A TCXO or even an OCXO can be used for demanding applications requiring tight holdover stability, low wander generation, or wander filtering. This application note provides insights into the advantages of each of these techniques and guidance for optimizing performance.

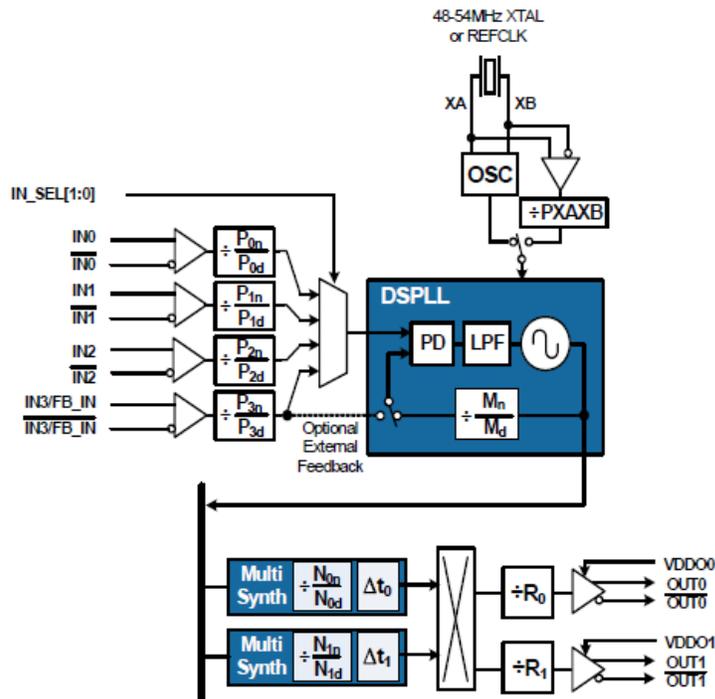


Figure 1. Si5342 Block Diagram

2. Optimizing Performance Using a Crystal

2.1. Advantages in Selecting a Crystal

The Si534x XA/XB oscillator drive circuit is a differential amplifier and provides excellent phase noise performance meeting demanding jitter requirements when using a crystal. Other advantages include lower cost, fewer components, and ease of design (e.g. signal integrity/layout compared to using a crystal oscillator). Just to note, the crystal load capacitors are part of the Si534x design and external load capacitors are not required. Additionally, power supply decoupling becomes a non-issue when using a crystal instead of a crystal oscillator, further reducing BOM cost. Several crystals meet the technical requirements, have been approved, and are listed in the Reference Manuals.

2.2. Advantages in Selecting a Higher Frequency Crystal

The recommended crystal frequencies are 25.000 MHz, 48.000 MHz, and 54.000 MHz. Figure 2 and Table 1 show the phase noise performance for a Si5345 156.250 MHz output, comparing performance using a 25.000, 48.000, and 54.000 MHz crystal at the XA/XB input. The Si5345 loop BW was set to 4 Hz when making phase noise measurements. Using the higher frequency 48.000 MHz and 54.000 MHz crystal improves overall phase noise performance compared with a 25.000 MHz crystal. The 25.000 MHz crystal is a lower cost option and can be used in cost sensitive applications where minimizing jitter is not paramount.

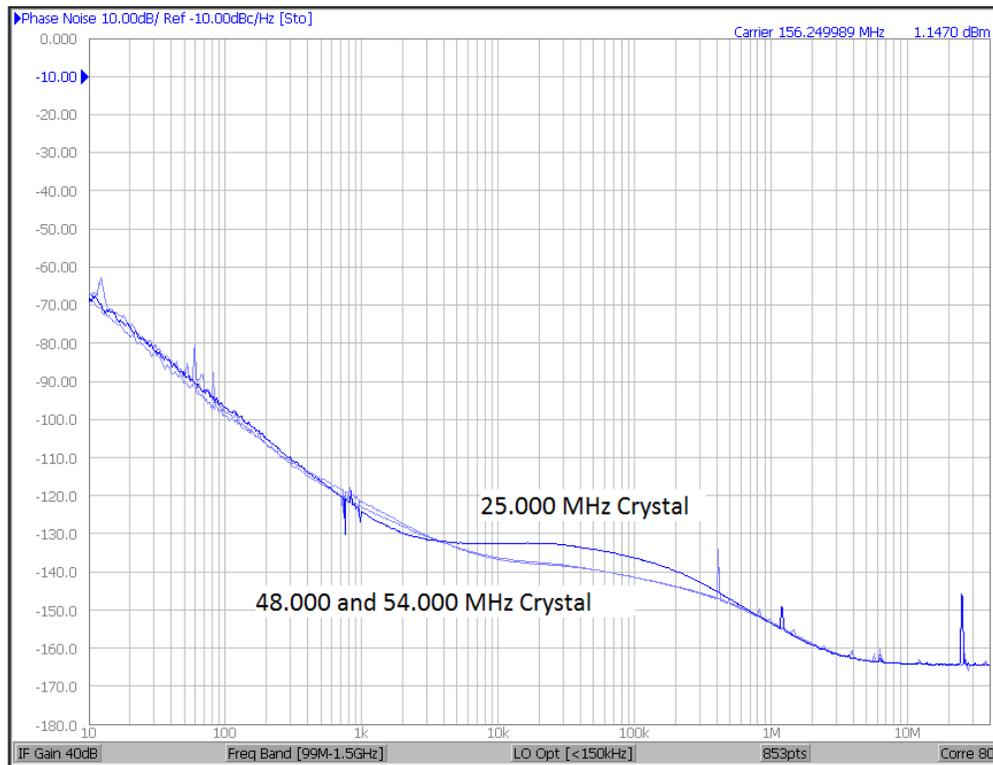


Figure 2. Si5345 156.250 MHz Phase Noise Comparison Using 25.000, 48.000, and 54.000 MHz Crystals as the XA/XB Reference

Table 1. Phase Jitter vs. XAXB Crystal Frequency

Crystal Frequency	Si5345 f _{out} = 156.250 MHz Phase Jitter over 12 kHz to 20 MHz
54.000 MHz	88 fs
48.000 MHz	90 fs
25.000 MHz	135 fs

2.3. Advantages in Selecting a Higher Q Crystal

Another consideration is crystal Q, or quality factor. Quality factor is not an indication of the reliability, but rather is the ratio of the energy stored versus energy lost in the crystal. A higher Q crystal can also be equated with a spectrum plot, having a narrower spread or lower BW versus one with a lower Q.

A higher Q crystal will result in better close-in phase noise performance as shown in Figure 3. In this example, the phase noise at 10 Hz offset is 8 db better when using a higher Q crystal. However, phase jitter over 12 kHz–20 MHz is only marginally better at 90 fs using a higher Q ~150 K versus 95 fs using a lower Q ~50 K. Crystal Q will need to be considered in applications where every last femtosecond reduction is critical. Typical crystal Q performance can be provided by the manufacturer.



Figure 3. Si5345 156.250 MHz Phase Noise Using a High Q vs. Low Q 48.000 MHz Crystal

3. Recommended Crystal Layout

The Si534x reference manual includes recommended crystal layout guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. Do not connect the crystal's GND pins to the PCB ground.
3. Connect the crystal's GND pins to the DUTs X1 and X2 pins via a local crystal GND shield place around and under the crystal.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.
5. In general do not route GND, power planes/traces, or local components on the other side below the crystal GND shield. As an exception, if it is absolutely necessary to use the area on the other side of the board for layout or routing, place the next reference plane in the stack-up at least two layers or 0.05 inches away. The Si534x/Si5380 should have all layers underneath the ground shield removed.

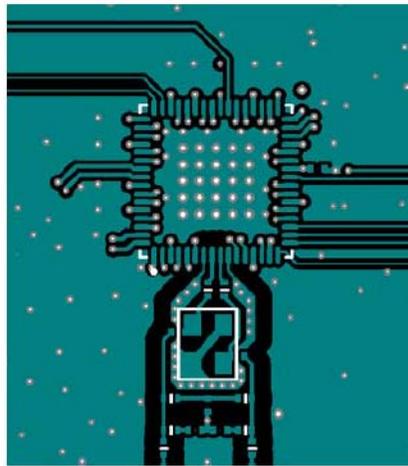


Figure 4. 64-pin Crystal Layout Recommendations, Top Layer

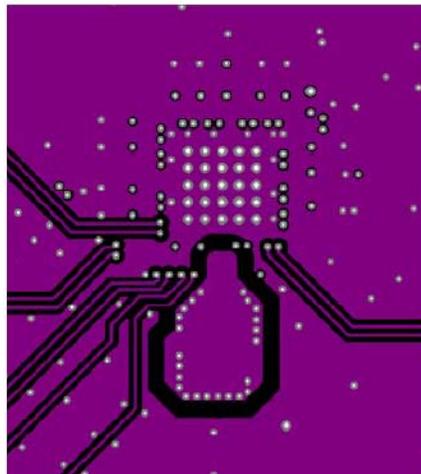


Figure 5. Zoom View Crystal Shield Layer, Below the Top Layer

4. Advantages to Selecting a Crystal Oscillator

Alternatively, a crystal oscillator can be used as the XA/XB source. There are some applications which place a premium on close-in performance, in which case a low-phase noise crystal oscillator is a better choice than a crystal. Figure 6 shows the close-in phase noise advantage of using a low-phase noise crystal oscillator versus a high Q crystal. Figure 7 is the oscillators phase noise performance used in making Figure 6 measurements.

Other advantages in selecting a crystal oscillator include the ability to customize specifications such as temperature range, temperature stability, and guaranteed start-up time.

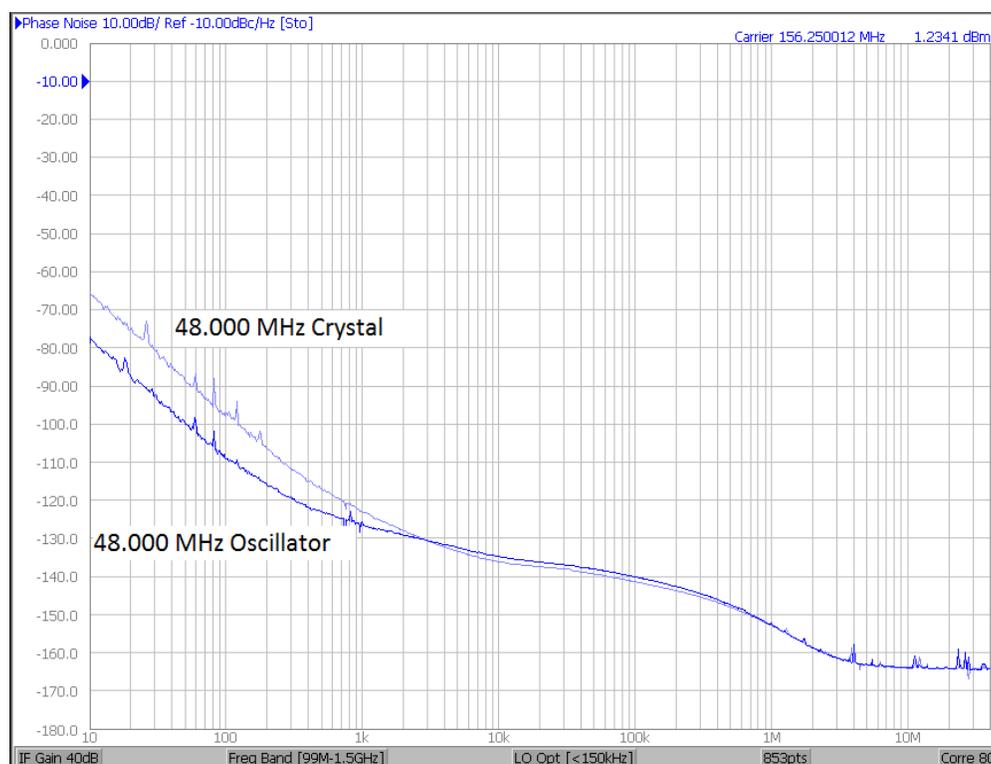


Figure 6. Si5345 Phase Noise
Using a Crystal vs. a Low Phase Noise Crystal Oscillator as the XA Reference

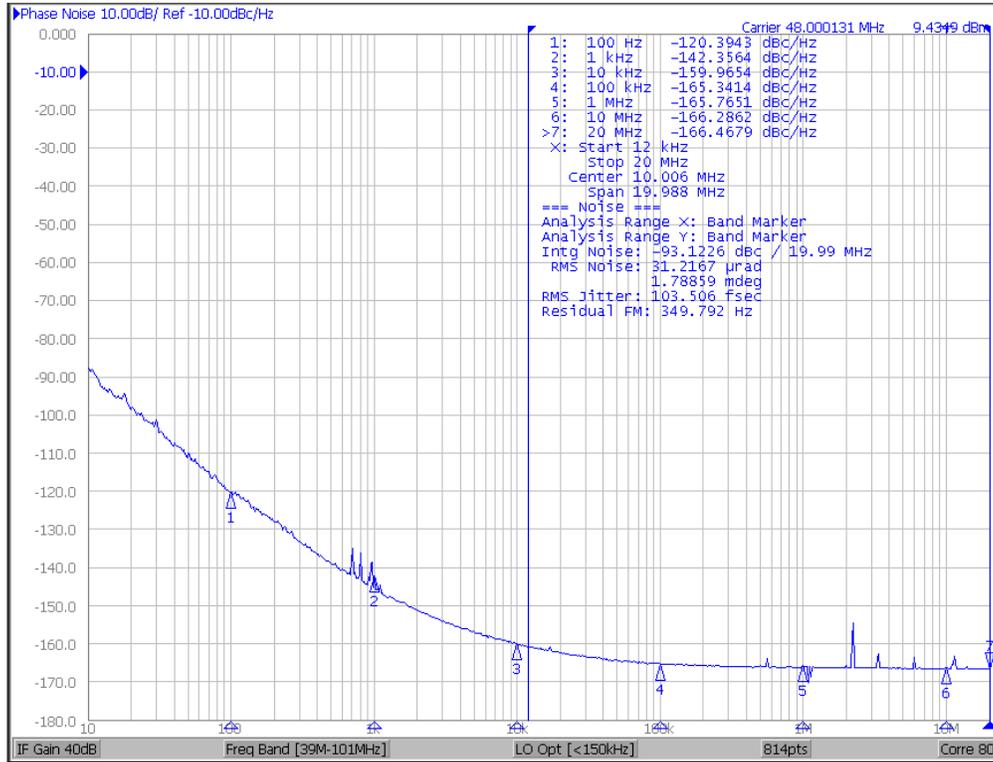


Figure 7. Low-Phase Noise Crystal Oscillator Performance Used in Making Figure 6 Measurements

5. Single-Ended XO Interface Considerations

A single-ended CMOS oscillator will most likely be used due to lower cost compared to a differential output option. The maximum XA/XB input amplitude is 2.0 V and most 3.3 V and even 2.5 V CMOS crystal oscillators' can exceed these maximum levels. However, this requires an attenuation circuit adding to the BOM cost. The overall device phase noise performance is dependent on both the crystal oscillator's phase noise performance and rise and fall times, or more accurately slew rate. The recommended slew rate is 400 V/ μ s or higher. The attenuation circuit required to reduce the output amplitude will also reduce slew rate. The interface circuit needs to be optimized considering the maximum amplitude rating and slew rate. Figure 8 is the recommended circuit which attenuates the signal while minimizing the impact on rise and fall times.

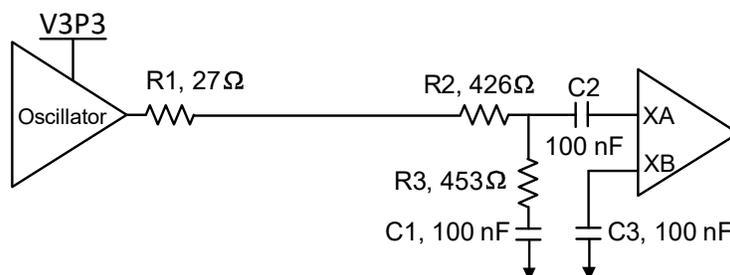


Figure 8. Recommended Single Ended CMOS Oscillator Interface Circuit

If a single-ended CMOS crystal oscillator is used, component selection as well as signal integrity layout will be critical; it's best to locate the oscillator as close to the XA/XB input as possible. Referring to Figure 8, the 27 Ω resistor is used to optimize signal integrity and is located as close as possible to the XO output. R27 can be modified as required, such as due to change in supply voltage or output impedance and is not required if the oscillator is located close to the XA/XB input. The R2/R3 attenuator would be located as close as possible to the XA input. Note that R2 and R3 can be modified to optimize the XA amplitude levels and rise/fall time while considering the loading on the oscillators output drive. Modifications should also be made for other oscillator supply voltages. As an example, R2 = 301 Ω and R3 = 698 Ω for a 2.5 V CMOS oscillator. Lower R2 and R4 values can be used if the XO has a higher drive capability. Also the XB input should be tied to ground through a capacitor for all single ended XA/XB applications.

6. Differential Crystal Oscillators

A differential output oscillator, LVPECL, LVDS, etc., can also be used as the XA/XB input. In general, these will not require attenuation circuits but will require AC coupling and a 100 Ω termination resistor across the XA/XB input. Locating a differential oscillator close to the XA/XB input is not as critical as a single ended CMOS option. The disadvantage is that differential output oscillators tend to increase BOM cost and typically have slightly higher phase noise compared to single ended CMOS oscillators.

Most differential sources have fast rise and fall times, well in excess of the 400 V/μs requirement. However, if the input slew rate was below the requirement, such as a sine wave, then a differential input offers an advantage over single ended input as shown in Table 2. If the oscillator is located some distance away from the XA/XB input then a differential output device should be considered, otherwise a single ended option is a more cost effective solution. A crystal is still the best overall solution for cost and 12 kHz–20 MHz phase jitter performance.

Table 2. Phase Jitter Performance, Single Ended vs. Differential XAXB Inputs

Source	Phase Jitter Over 12 kHz to 20 MHz Using a Low Phase Noise 48 MHz Sine Wave Generator, SMA100A	Phase Jitter Over 12 kHz to 20 MHz Using a 48 MHz LVPECL XO
Differential	106 fs	114 fs
Single Ended	136 fs	115 fs

7. Crystal Oscillator Phase Noise Requirements

For optimal phase jitter performance, the recommended minimum XA input slew rate is 400 V/μs. While there are no defined limits regarding oscillator phase noise requirements, Table 3 provides insight as to the trade-off between the XA reference phase noise versus the Si5345 phase jitter over 12 kHz to 20 MHz. A 48 MHz crystal will outperform even the lowest phase noise 48 MHz oscillator over 12kHz to 20MHz, and at a lower cost. MEMs is not a recommended solution as the XA/XB reference due to its relatively high phase noise and excess wander performance.

Table 3. Phase Jitter vs. XA Input Oscillator Phase Noise

Device	48.000 MHz XA Phase Noise at 10 kHz	20 kHz	50 kHz	100 kHz	Si5345, 156.250 MHz Phase Jitter, 12 kHz – 20 MHz
1	-162	-163	-165	-169	98 fs
2	-160	-162	-164	-165	101 fs
3	-153	-154	-157	-158	112 fs
4	-152	-153	-156	-158	113 fs
5	-149	-151	-154	-155	135 fs
6	-136	-140	-143	-150	312 fs

8. Recommended Crystal Oscillator Layout

The Si534x reference manual includes recommended crystal oscillator layout guidelines, using an eight layer board as an example:

- Layer 1: device layer, with low speed CMOS control/status signals, ground flood
- Layer 2: crystal shield
- Layer 3: ground layer
- Layer 4: power distribution, ground flooded
- Layer 5: power routing layer
- Layer 6: ground input clocks, ground flooded
- Layer 7: output clocks layer
- Layer 8: ground layer

Figure 4 is the top layer layout of the Si534x device mounted on the top PCB layer. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. The crystal oscillator/oscillator area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

For applications that do not use a crystal, leave X1 and X2 pins as “no connect”. Do not tie to ground. There is no need for a crystal shield or the voids underneath the shield. The XAXB connection should be treated as a high speed critical path that is ac-coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA to the XB pin. Jitter is very critical at the XAXB pins and therefore split termination and differential signaling should be used whenever possible.

9. Using a TCXO/OCXO

Due to cost, a TCXO or OCXO will only be used in demanding applications such as G8262, Stratum 3/3E, IEEE1588 wander filtering or when long term holdover is a primary concern. These applications generally use a lower loop BW in the 1 mHz to 10 Hz range where low wander on the XA input is critical to optimize lock time, improve wander generation and holdover stability. A TCXO or OCXO must be used to meet the G.8262/ Stratum3/3E and IEEE1588 requirements as a crystal or crystal oscillator will result in excess wander, lock time, and holdover stability. For best wander performance, a TCXO or OCXO should be considered for applications with a 50 Hz or lower loop bandwidth.

9.1. TCXO OCXO Interface

If the TCXO or OCXO output is being used as the XA/XB input then Figure 8 is recommended to attenuate the amplitude. Due to slower rise and fall times, a clipped sine wave TCXO or sine wave OCXO is not recommended as the XA/XB input, but could be used if phase jitter performance is not paramount. Figure 9 compares the phase noise performance for the Si5345 using a CMOS TCXO versus clipped sine wave TCXO. Even though the clipped sine wave TCXO has slightly better phase noise, we see the superior slew rate offered by the CMOS TCXO results in better overall performance. Table 4 compares the XA source phase noise and slew rate with the resulting Si5345 12 k to 20 MHz phase jitter.

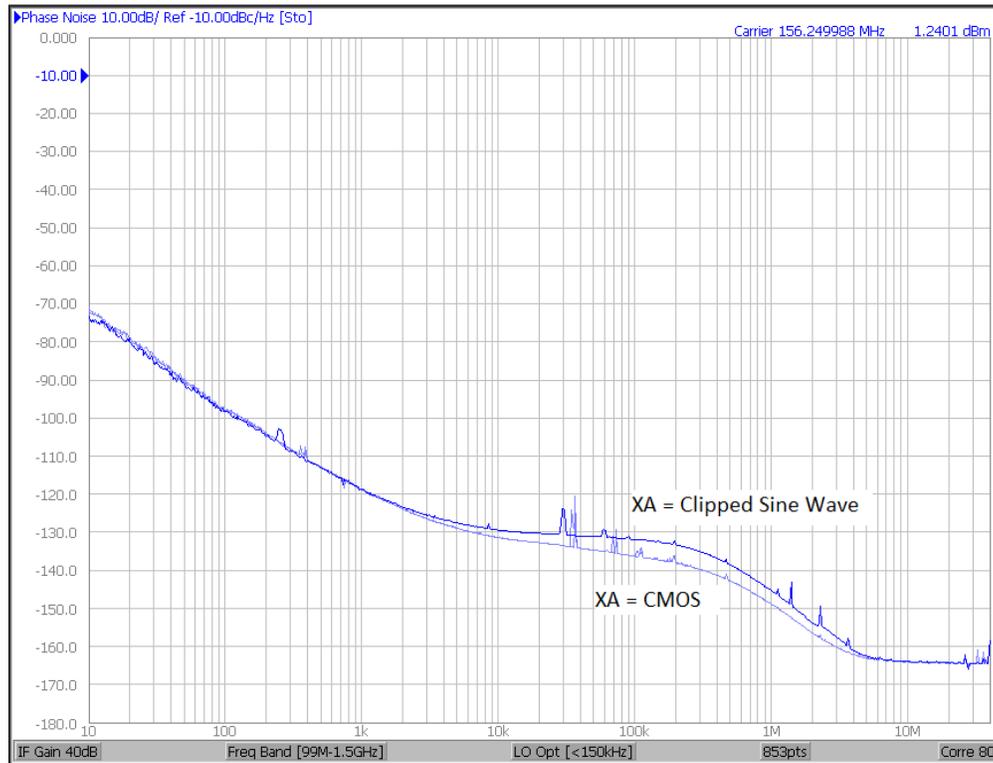


Figure 9. Si5345 156.250 MHz Phase Noise Using a CMOS TCXO vs. Clipped Sinewave TCXO

Table 4. Phase Jitter vs. XAXB Input Slew Rate

XA Source	XA Input Phase Jitter 12 kHz – 5 MHz	XA Input Slew Rate	Si5345, f _{out} = 156.250 MHz Phase Jitter 12 kHz – 20 MHz
40.000 MHz CMOS TCXO	170 fs	390 V/μs	155 fs
40.000 MHz Clipped Sine Wave TCXO	155 fs	140 V/μs	227 fs

9.2. Phase Noise Using a Low Frequency TCXO or OCXO

Lower output frequency OCXO's and TCXO's can cost less and have lower aging rates compared to higher frequency options. 10.000 MHz and 12.800 MHz are most commonly used, considered industry standards and may be the preferred choice. A low frequency source can be used as the XAXB, however, this creates a spur at an offset equivalent to the TCXO or OCXO output frequency. As an example, Figure 10 shows the phase noise performance using a 12.800 MHz OCXO as the XA source for a Si5345 and the resulting a spur located at 12.800 MHz offset. In this example, the 12 kHz to 20 MHz phase jitter is 411 fs with the spur included, and 225 fs when omitting the spur. The Si5348 should be considered when the application requires low phase jitter performance and a low frequency TCXO or OCXO is going to be used. An Si5348 in the same configuration and using the same 12.800 MHz OCXO has 118 fs phase jitter over 12 kHz through 20 MHz including spurs.

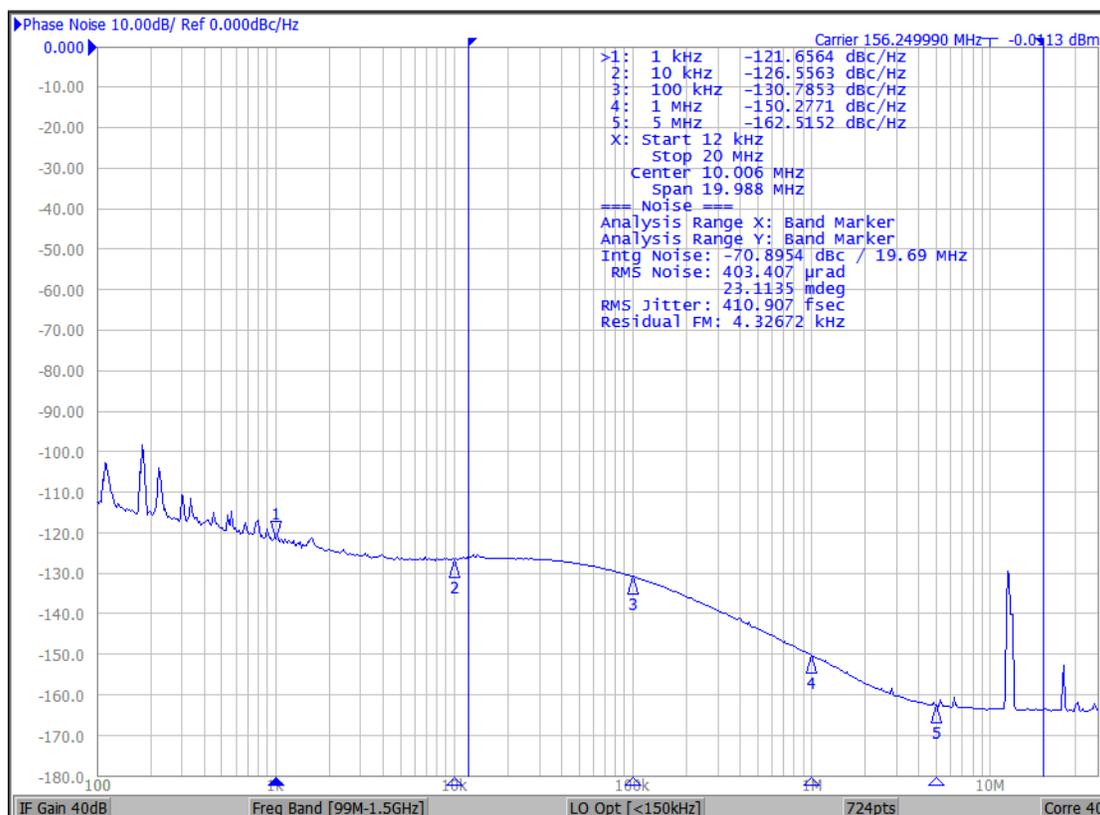


Figure 10. Si5345 Phase Noise Performance Using a 12.800 MHz OCXO as the XA Input

9.3. Using a Buffer for Best Isolation when Driving Multiple Loads

Generally OCXO's and TCXO's are not low output impedance devices and are sensitive to loading. Wander performance and temperature stability can be degraded due to high capacitive loading and or low resistive loading. If the TCXO or OCXO output must be routed to several devices, then it's best to use a fan-out buffer, such as Silicon Labs Si53302.

9.4. Power Supply Considerations

OCXO's can require over 1 amp of current during warm-up. PC traces and the number of ground vias need to be considered to minimize DC losses. The OCXO's power supply current will change with temperature variations. Any resulting change in power supply voltage will contribute to wander generation. Current sensing resistors will most likely cause excessive and varying voltage drops and should not be used. Ferrite beads with a low impedance and high current rating can be considered.

Power supply decoupling will be required when an XO, TCXO, or OCXO is used. It's best to use the recommended values in the data sheet as a minimum. Noise and coupling between reference frequencies becomes more problematic as frequencies become closer in value. Power supply filtering may need to be more robust in these applications. Multiple values (e.g. 10 μ F, 100 nF, and 10 nf) provides a wider spectrum of decoupling while multiple capacitors of the same value reduces impedance. Each de-coupling capacitor should have a dedicated ground via.

9.5. Mechanical and Environmental Considerations

Air flow, temperature changes, and vibration will impact a crystal or crystal oscillator's performance. Air flow and thermal gradients can be reduced by placing a cover over the crystal, crystal oscillator, TCXO, and in some cases even an OCXO. Figure 11 shows the low frequency time domain performance advantage of using a cover versus no cover and no cover plus air flow, using a 40 MHz TCXO as the XA/XB reference.

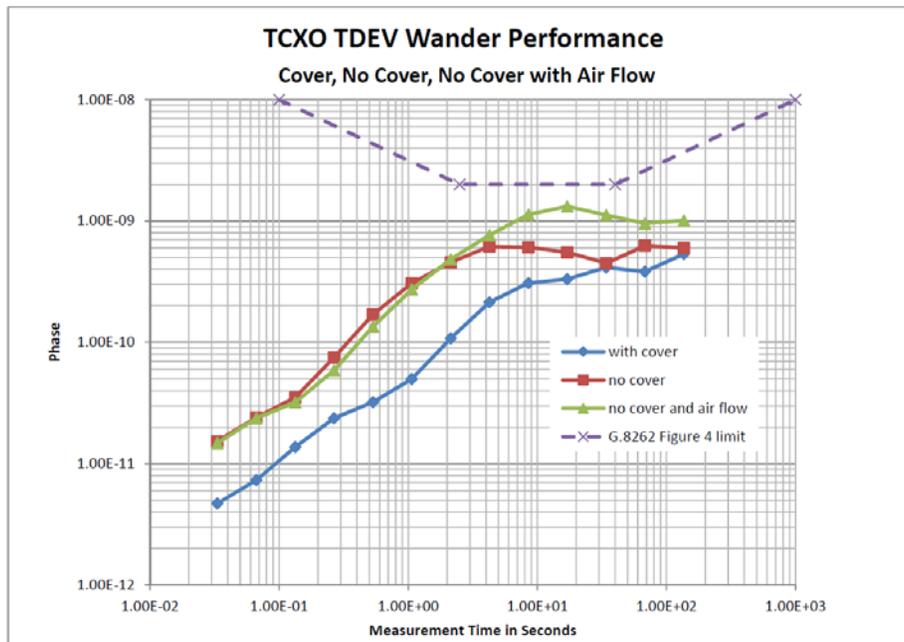


Figure 11. Optimizing TCXO Performance Using a Cover

In some applications it may be more interesting to compare results using a phase noise measurement. Figure 12 is a phase noise plot of a 48.000 MHz crystal oscillator, comparing performance using a cover versus no cover. Figure 11 and Figure 12 both highlight the advantage of using a cover in the low frequency time and phase domains whereas Figure 10 additionally shows it is less critical in the higher frequency offset range such as 12 kHz through 20 MHz. A Rakon PCV00015AA1 cover was used in both cases. Significant performance advantages can be realized using a simple cover.

A TCXO or OCXO should not be placed next to a heat source. Heat sinking should not be used with TCXO's or OCXO's. Ground planes should be eliminated underneath a TCXO or OCXO and other methods of thermal isolation should be considered.

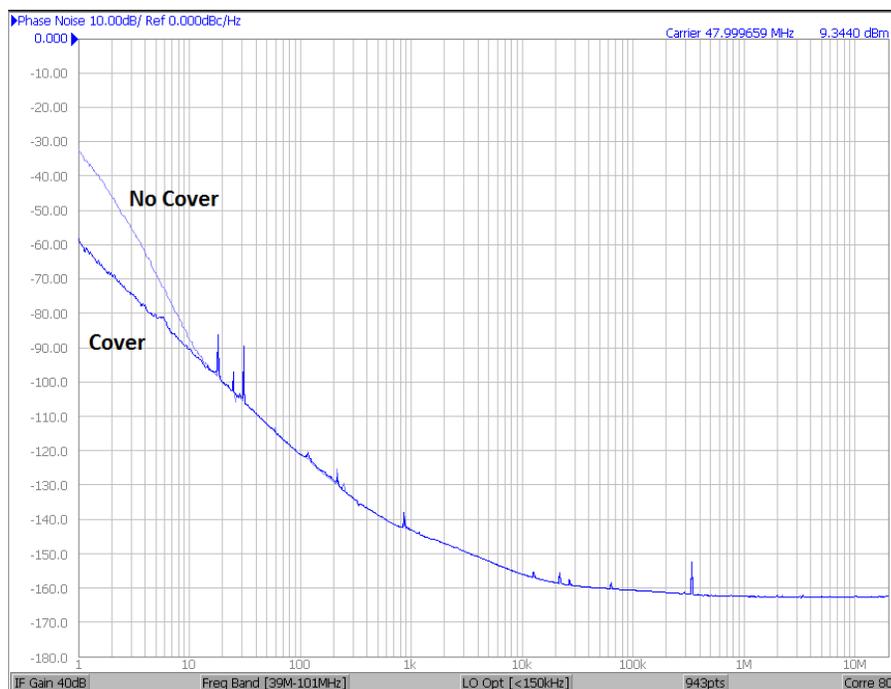


Figure 12. Phase Noise Performance for a 48.000 MHz Crystal Oscillator Using a Cover vs. Uncovered

Mechanical vibration will also affect performance including wander, phase noise, and lock time. Special consideration such as mechanical isolation or damping may be required in extreme or sensitive applications. Alternatively, a vibration resistance crystal or crystal oscillator could be considered but would most likely be cost prohibitive for most commercial applications.

10. Summary

Most applications are best served using a low cost crystal.

Crystal Advantages:

- Performance
- Cost
- Simplicity
- Signal Integrity

A crystal oscillator can be used instead of crystal.

Crystal Oscillator Advantages:

- May already be available.
- Can provide better close-in phase noise performance depending on the crystal oscillator used.
- Easier to customize specifications including temperature range, stability, and phase noise.

For applications requiring a TCXO include Stratum 3, G.8262/SyncE:

TCXO Advantages:

- Improved Hold Over Stability.
- Improved MTIE TDEV Noise generation / wander performance.

For applications requiring an OCXO include Stratum 3E, 1588 and extended temperature range Stratum 3 and G.8262/SyncE:

OCXO Advantages:

- Best Hold Over Stability.
- Best MTIE TDEV Noise generation / wander performance.

For Best Phase Jitter Performance, the XA/XB input should:

- Use a recommended 48.000 or 54.000 MHz crystal.
- Follow the PC board layout guidelines in the Reference Manual.
- Consider the physical environment.

If an Oscillator, TCXO or OCXO is used:

- Use a lower phase noise option.
- Use a higher frequency, e.g. 40 MHz instead of 25 MHz.
- Locate the oscillator close to the Si534x Si5380 XA/XB input.
- Optimize rise and fall times.
- Optimize signal integrity.
- Incorporate power supply decoupling.
- Consider the OCXO current consumption requirements, both power-up and steady state.
- Keep the TCXO away from heat sources and thermal gradients.
- Do not heat sink a TCXO or OCXO, eliminate copper planes underneath. Thermal isolation is preferred.
- Use a cover.
- Use a buffer on the XO, TCXO, or OCXO output if multiple sources must be driven.
- Adhere to data sheet minimum and maximum electrical, environmental, and process limits.
- A single ended oscillator is usually lower cost and typically has better phase noise performance.
- Consider the physical environment.



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