AN923.1: EFR32 Series 1 sub-GHz Matching Guide

The EFR32 family of RFICs includes chip variants that provide 2.4 GHz-only operation, sub-GHz-only operation, or dual-band (2.4 GHz and sub-GHz) operation. This application note provides a description of the RF matching for those EFR32 chip variants that provide sub-GHz operation.

Note: This document does ***not*** address the matching procedure for the 2.4 GHz path. The 2.4 GHz matching procedure is described in application note, AN930.1: EFR32 Series 1 2.4 GHz Matching Guide.

KEY POINTS

- Provides an overview of matching procedure
- Specifically discusses design procedures for the lowpass filter, balun, and impedance transformation network
- Shows how to apply the information provided

1. Introduction

The EFR32 family of RFICs includes chip variants that provide 2.4 GHz-only operation, sub-GHz-only operation, or dual-band (2.4 GHz and sub-GHz) operation. This application note provides a description of the RF matching for those EFR32 chip variants that provide sub-GHz operation.

Note: This document does ***not*** address the matching procedure for the 2.4 GHz path. The 2.4 GHz matching procedure is described in AN930.1: EFR32 Series 1 2.4 GHz Matching Guide.

This application note provides technical details and description of EFR32 Series 1 sub-GHz matching solutions applied on the publicly available Silicon Labs reference radio boards. These matching networks discussed in this document aim single- and narrow-band applications, and utilize an external ceramic balun in the RF path. AN1180: EFR32 Series 1 sub-GHz Discrete Matching Solutions provides matching solutions when utilizing discrete components only in the RF path, and also covers application use-cases for dual- and/or wide-band frequency operation. Discrete single-band matching networks in AN1180 have similar RF performance as the radio board matches with the external ceramic balun documented in this application note.

Furthermore, IPD (integrated passive device) solutions are also available with EFR32 Series 1 family of SoC for the sub-GHz frequency bands of 434 and 868 MHz. An IPD compromises all the required external passive matching components into one device (i.e., IPD), which reduces the occupied PCB area, manufacturing and pick-and-place costs and simplifies the design. Details about the IPD solutions with EFR32 Series 1 family are summarized in the AN1081: Integrated Passive Devices for EFR32 Series 1 Sub-GHz RF Matching.

The layout design of the match is critical to achieve the targeted power and efficiency. This is especially true for the RX path, which can be easily detuned by the PCB parasitics. Because of this, Silicon Labs suggests copying the RF part of the reference PCB design, or if it is not possible, applying the layout design rules and guidelines described in application note, AN928.1: EFR32 Series 1 Layout Design Guide.

The matching effort strives to simultaneously achieve several goals:

- Provide for tying together the TX and RX signal paths, external to the RFIC.
- Provide the desired nominal TX output power level (measured at the connector to the antenna / load).
- Obtain this nominal TX output power at the nominal supply voltage.
- Provide optimal RX Sensitivity.
- Minimize current consumption (i.e., maximize efficiency).
- Comply with regulatory specifications for spurious emissions.

The matching procedures outlined in this document will help achieve the goals listed above.

Table 3.1 Summary of Matching Component Values vs. Frequency (CLNA = 1.0 pF) on page 25 and Table 3.2 Summary of Matching Component Values vs. Frequency (CLNA = 1.25 pF) on page 26 are provided for users more interested in quickly obtaining matching component values than in the methodology used to develop the matching network.

Table 3.3 Summary of Matching RF performance in TX mode (CLNA = 1.0 pF) on page 26 summarizes the RF performance of the matches used in Silicon Laboratories reference designs.

2. Matching Procedure

2.1 Overview

The sub-GHz LNA and PA circuits in EFR32 RFICs are fully differential and are not tied together inside the chip. As a result, a total of four pins are required on the RFIC to provide access to the LNA and PA circuits: SUBGRF_OP/ON for the TX output, and SUBGRF_IP/IN for the RX input. These four pins are adjacently located, as shown in the figure below, regardless of chip variant. The RF matching circuit must provide for connecting the TX and RX signal paths together, external to the RFIC.

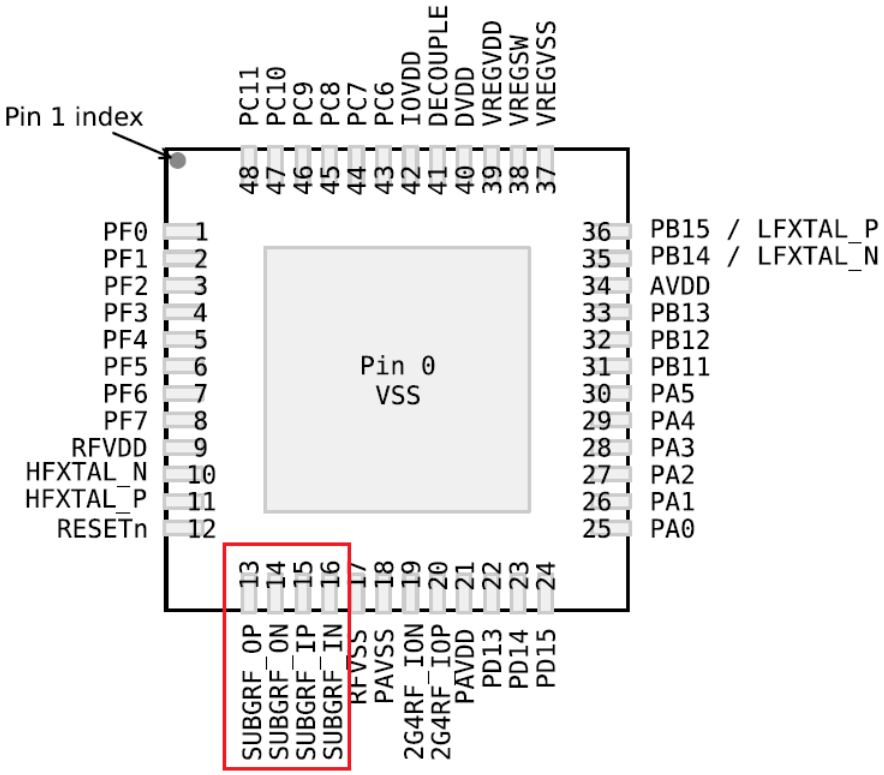


Figure 2.1. Example Pin Locations of sub-GHZ TX and RX Functions

The general topology of the sub-GHZ RF matching network is shown in the figure below. The RF matching network consists of the following blocks:

- A lowpass filter section (for suppression of harmonics and spurious emissions in TX mode).
- A balun (to provide a single-ended to differential conversion function).
- An impedance transformation section (to present the correct impedances to the TX and RX pins of the RFIC).

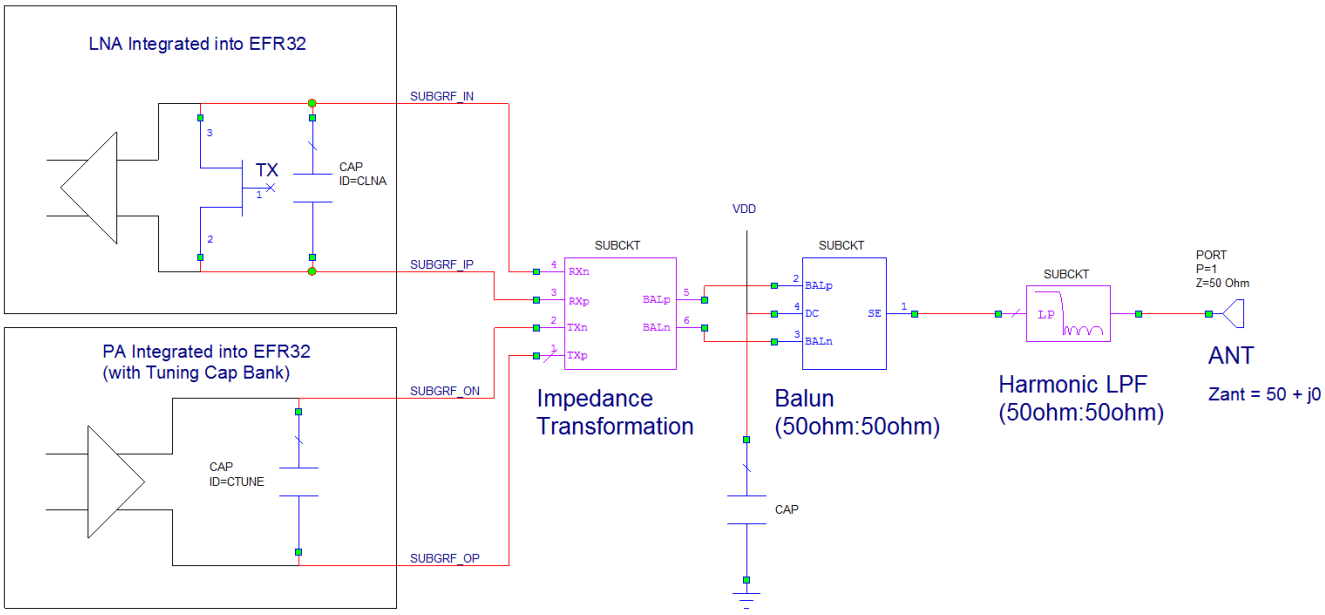


Figure 2.2. General Topology of sub-GHZ RF Match

The TX pins of the RFIC (SUBGRF_OP/ON) must be supplied with the V_{DD} supply voltage. Many commercially available baluns provide a center tap on their balanced port through which the DC voltage may be applied, as shown in the figure above. If the selected balun does not provide such a center tap, it is necessary to supply the DC voltage to the TX pins through a pair of high-value DC pull-up inductors.

The circuit block that provides the impedance transformation function is the “interesting” part of the match, and will receive the most discussion within this application note. This circuit block is also where the TX and RX signal paths are tied together.

2.2 Lowpass Filter

The lowpass filter network is designed to attenuate the TX harmonics and spurious emissions below the level required to meet applicable regulatory standards (e.g., FCC, ETSI, or ARIB).

It is difficult for Silicon Labs to recommend one single lowpass filter design that is appropriate for all customers, as customers may operate at significantly different TX power levels as well as under widely differing regulatory standards and harmonic requirements. Also, the radiation efficiency of the antenna selected by the customer is not known in advance. These factors make it difficult for Silicon Labs to conclusively state the required filter attenuation characteristics.

The selected filter type (e.g., Butterworth, Chebyshev, Elliptic) is not a mandatory design constraint. If the selected filter provides acceptable attenuation of the harmonic signal energy and reasonable insertion loss, it is a “good” filter. Silicon Labs typically uses Chebyshev lowpass filter networks with small (0.25 dB to 0.5 dB) passband amplitude ripple as a good trade-off between flat passband response and rate of attenuation in the stopband. The filter design should, however, be designed for a 1:1 impedance transformation (i.e., 50 Ω input and 50 Ω output impedance). This will greatly simplify the subsequent connection of the additional matching network blocks (i.e., balun and impedance transformation network).

Filter component values may be obtained by usual design methods, such as use of Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation, and will not be further discussed here. However, Silicon Labs has developed matching networks across a wide range of frequencies, supporting a range of TX output power levels. The measured results from those matching exercises lead to the following general statements:

- An application with +20 dBm TX output power level will likely need a 5^{th}-order or 7^{th}-order lowpass filter, depending upon the stringency of the applicable regulatory standard.
- An application with +10 dBm (or less) TX output power level will only need a 3^{rd}-order lowpass filter.
- An application with +14 dBm TX output power level will need either a 3^{rd}-order or 5^{th}-order lowpass filter, depending upon the limits of the applicable standards.

The topology of the lowpass filter(s) used by Silicon Labs is shown in the figure below.

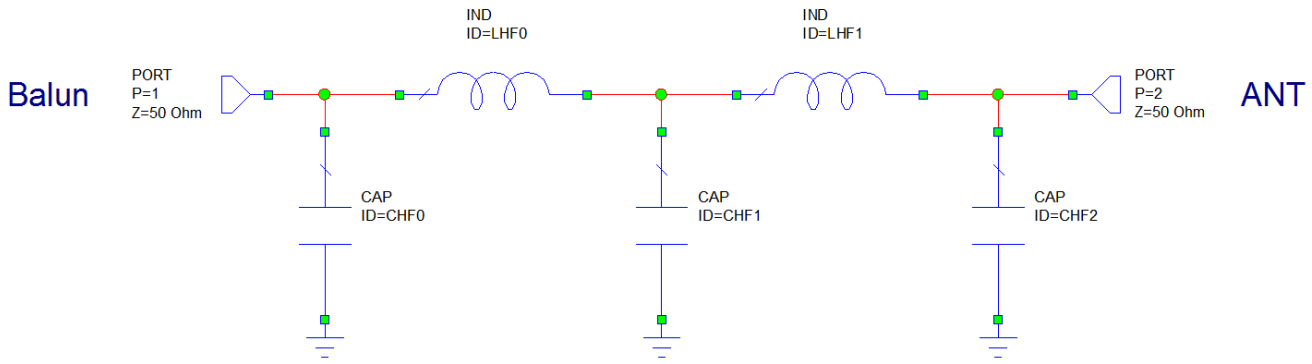


Figure 2.3. Lowpass Filter Topology

A summary of lowpass filters developed for use in Silicon Labs’ reference designs is shown in the table below. All filters summarized in this table are symmetrical designs (due to the 1:1 impedance transformation ratio). In those few instances where the component values are not perfectly symmetrical (i.e., CHF0 ≠ CH2 or LHF0 ≠ LHF1), the reason is that the design has been slightly adjusted to compensate for parasitic effects of the actual board layout.

Table 2.1. Lowpass Filter Component Values vs. Frequency

Freq Band	Order	CHF0	LHF0	CHF1	LHF1	CHF2	LHF2	CHF3
169 MHz	N = 3	18 pF	47 nH	18 pF	N/A	N/A	N/A	N/A
	N = 5	20 pF	56 nH	33 pF	56 nH	20 pF	N/A	N/A
	N = 7	15 pF	51 nH	33 pF	56 nH	33 pF	51 nH	15 pF
230 MHz	N = 7	12 pF	39 nH	24 pF	43 nH	24 pF	39 nH	12 pF
262 MHz	N = 7	2.7 pF	33 nH	18 pF	51 nH	18 pF	33 nH	2.7 pF
315 MHz	N = 3	8.2 pF	24 nH	8.2 pF	N/A	N/A	N/A	N/A
	N = 5	8.2 pF	30 nH	15 pF	30 nH	8.2pF	N/A	N/A
	N = 7	6.8 pF	30 nH	15 pF	36 nH	15 pF	30 nH	6.8 pF
345 MHz	N = 5	6.2 pF	36 nH	12 pF	36 nH	6.2 pF	N/A	N/A
	N = 7	6.2 pF	36 nH	10 pF	51 nH	10 pF	36 nH	6.2 pF
434 MHz	N = 3	6.8 pF	18 nH	6.8 pF	N/A	N/A	N/A	N/A
	N = 5	6.2 pF	24 nH	11 pF	24 nH	5.6pF	N/A	N/A
490 MHz	N = 3	5.6 pF	15 nH	5.6 pF	N/A	N/A	N/A	N/A
	N = 5	6.2 pF	22 nH	10 pF	22 nH	6.2 pF	N/A	N/A
868 MHz	N = 3	3.9 pF	9.1 nH	3.9 pF	N/A	N/A	N/A	N/A
	N = 5	3.0 pF	11 nH	5.6 pF	11 nH	3.0 pF	N/A	N/A
915 MHz	N = 3	3.6 pF	9.1 nH	3.6 pF	N/A	N/A	N/A	N/A
	N = 5	3.3 pF	10 nH	5.6 pF	10 nH	3.3 pF	N/A	N/A
950 MHz	N = 3	3.3 pF	8.7 nH	3.3 pF	N/A	N/A	N/A	N/A
	N = 5	3.3 pF	9.1 nH	5.6 pF	9.1 nH	3.3 pF	N/A	N/A

The inductors used in Silicon Labs reference designs are currently wire-wound surface mount inductors, such as the Murata LQW15A or LQW18A series, or the CoilCraft 0402CS, 0402HP, 0603CS, or 0603HP series. Wire-wound inductors provide the best performance, but are more expensive. It is possible to use a cheaper series of inductors (i.e., multi-layer inductors such as the Murata LQG15HS series), however, there will be some slight increase in insertion loss that will result in a decrease in TX output power and/or a degradation in RX sensitivity. This degradation in performance is small, typically less than 0.5 dB.

For informational purposes, the frequency response of a typical 5th-order lowpass filter using wire-wound inductors is shown in the figure below.

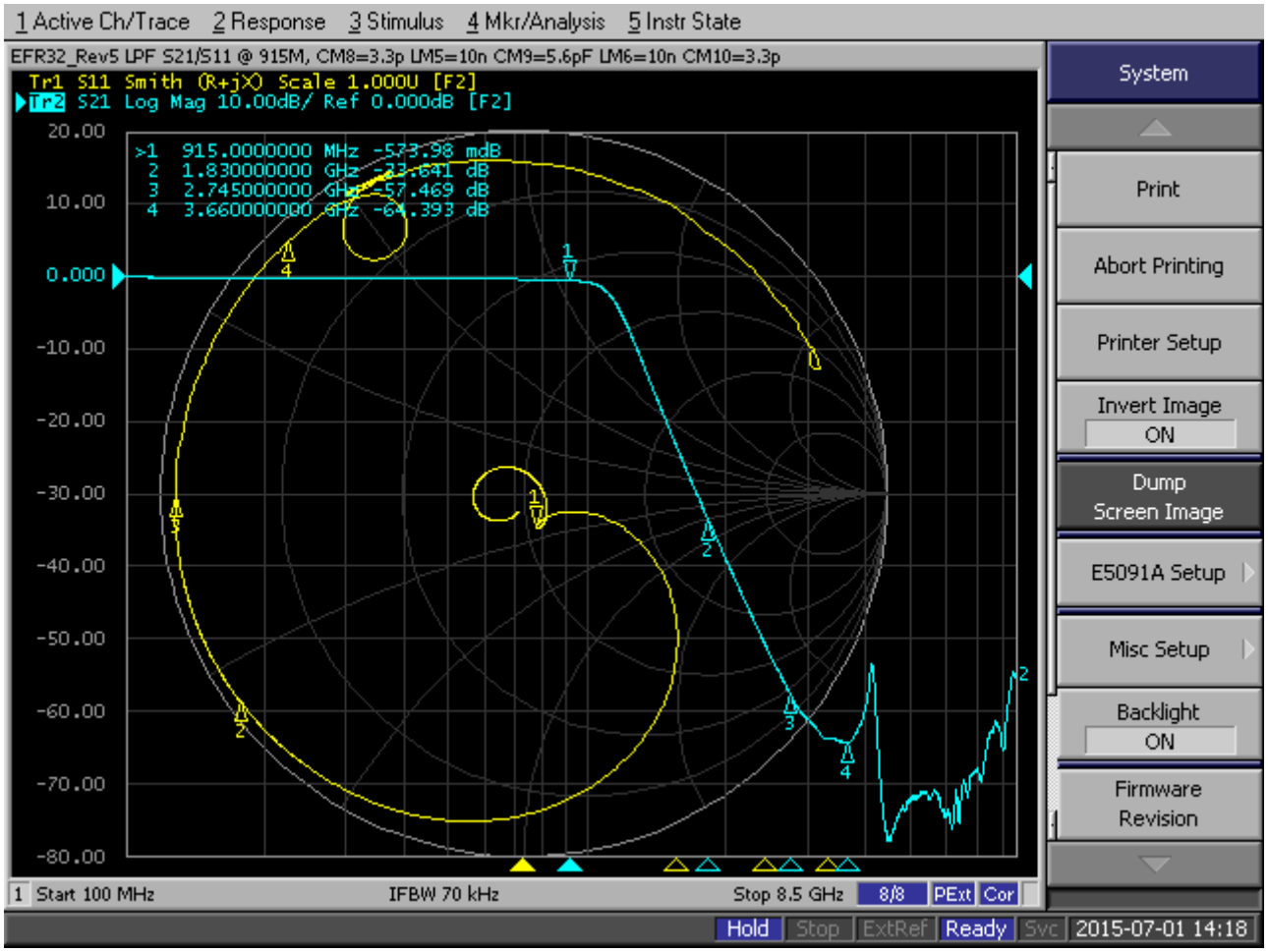


Figure 2.4. Typical Lowpass Filter Frequency Response (915 M, N = 5)

2.3 Balun

The balun is selected to provide a single-ended to differential conversion function with minimal insertion loss over the frequency band of interest. As mentioned previously, it is also highly desirable for the balun to provide a center tap through which DC voltage is supplied to the TX output pins.

Silicon Labs currently uses the 0900BL15C050 balun from Johanson Technology for applications within the 868 MHz and 915 MHz frequency bands, and the ATB2012_50011 balun from TDK for applications within all frequency bands from 169 MHz to 490 MHz. The TDK balun does not provide a center tap and thus it is necessary to supply the V_{DD} supply voltage to the TX output pins through a pair of high-value DC pull-up inductors.

The baluns from Johanson Technology listed below are drop-in replacements for 0900BL15C050 and can be also used for high-band frequency applications:

- 0900BL15D0050
- 1720BL15B0050

These baluns selected by Silicon Labs are 50 Ω:50 Ω baluns. As shown in Figure 2.2 General Topology of sub-GHZ RF Match on page 4, the balun is followed by a circuit block that provides an impedance transformation function. While it may prove possible to select a balun that provides a different impedance transformation ratio (e.g., 50 Ω:125 Ω), thus simplifying the subsequent impedance transformation block, Silicon Labs has not yet investigated this matching approach.

Silicon Labs also provides a list of second source (TDK), alternative ceramic balun options (however in a slightly smaller package) below for high-band frequency applications. 50:50 Ω balun needs to be used for drop-in replacement, but for example 50:100 or 50:125 Ω balun can also be used (100 or 125 Ω is the balanced impedance). However, matching network component value changes will be required in the TX match between the ceramic balun and EFR32 part.

- HHM1776B2: https://product.tdk.com/info/en/documents/data_sheet/rf_balun_hhm1776b2_en.pdf
- HHM1776B3: https://product.tdk.com/info/en/documents/data_sheet/rf_balun_hhm1776b3_en.pdf
- HHM1522B1: https://product.tdk.com/info/en/documents/data_sheet/rf_balun_hhm1522b1_en.pdf

The typical combined performance of a balun and 5^{th}-order lowpass filter is shown in the figure below, for informational purposes. This plot depicts the typical insertion loss from the ANT port to the differential port of the balun.

Be aware that Silicon Labs also provide matching solutions when the external ceramic balun discussed in this section is replaced by discrete components only. For full discrete reference matching designs, refer to AN1180: EFR32 Series 1 sub-GHz Discrete Matching Solutions.

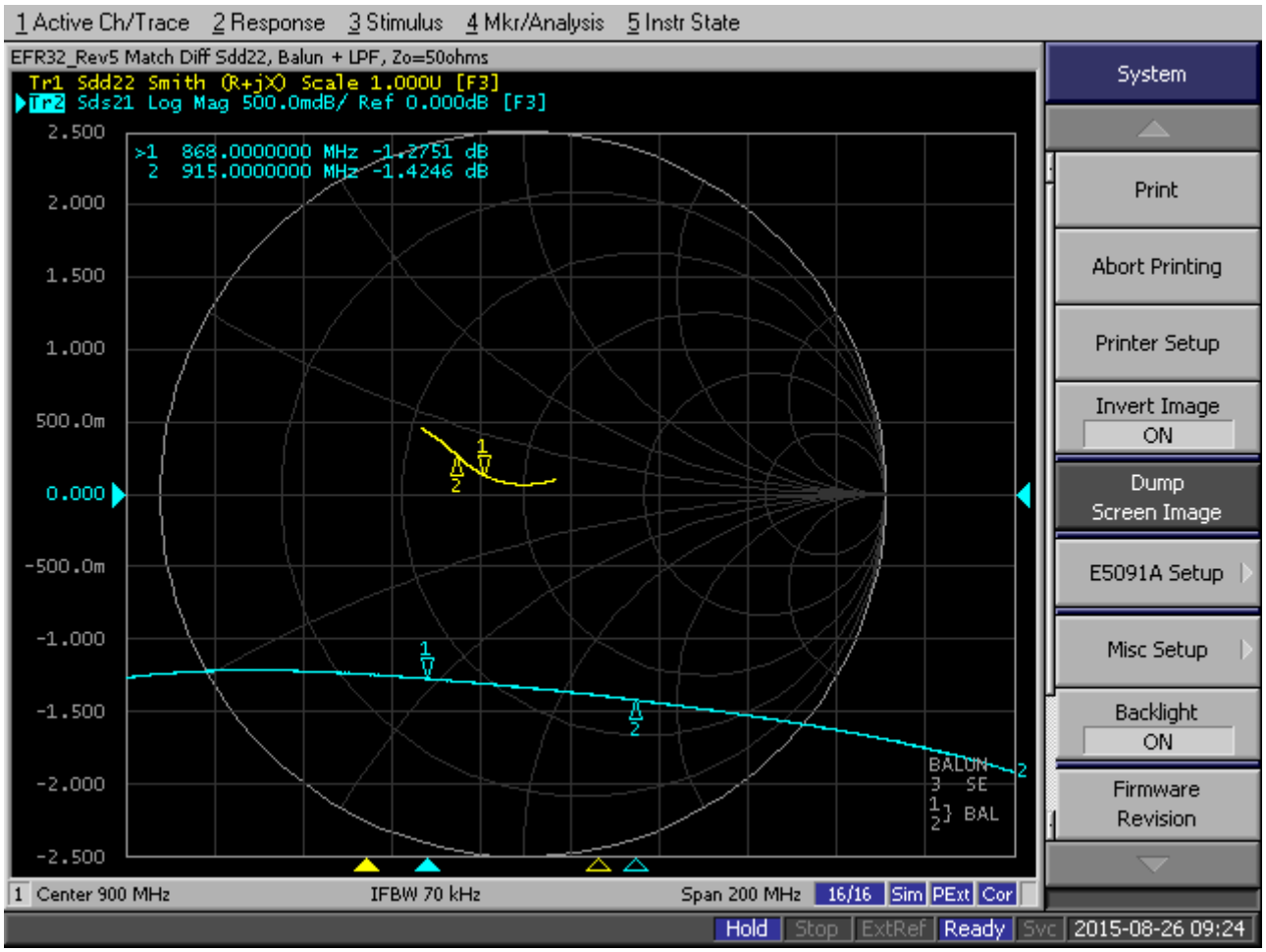


Figure 2.5. Typical Performance through LPF + Balun (915 MHz, N = 5, 0900BL15C050 Balun)

2.4 Impedance Transformation and TX/RX Tie

The circuit block that provides the impedance transformation and TX/RX tie functions is the most complex part of the match. The general topology of this block (and how it interconnects to the LPF and balun) is shown in the figure below.

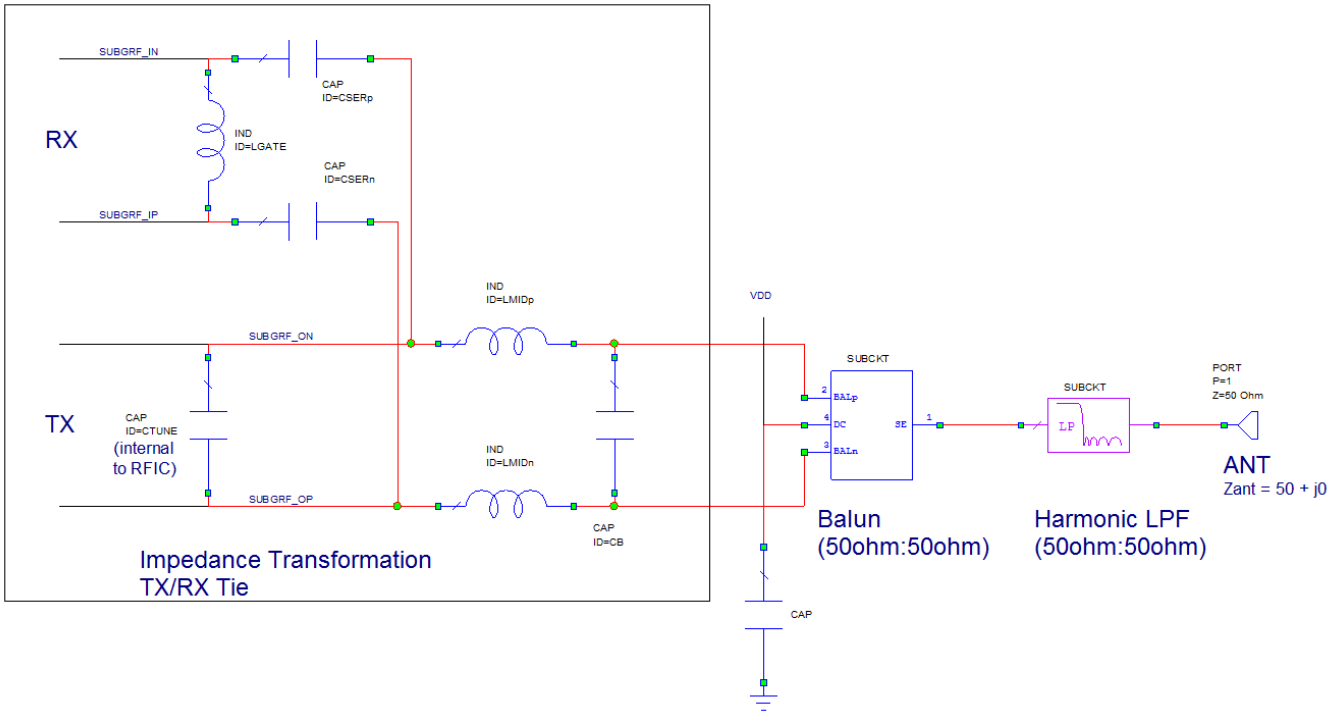


Figure 2.6. Impedance Transformation Block Topology

The RX match interacts weakly with the TX path, and thus the recommended design approach is to construct the match for the TX path *first*, followed by the addition of the RX match. As a result, the TX match is discussed first.

2.4.1 TX Signal Path and Match

The sub-GHz PA in EFR32 chips uses a Class AB design. The maximum available TX output power (for a given chip variant) is a function of the V_{DD} voltage supplied to the TX output pins and of the differential load impedance presented to the TX output pins. In a very simplistic sense,

$$P_{OUT\_DIFF} = 2*P_{OUT\_SE} = 2*\frac{\left(0.707*V_{SWING\_PK\_SE}\right)^2}{R_{LOAD\_SE}} = \frac{V_{SWING\_PK\_SE}^{\ 2}}{R_{LOAD\_SE}} \approx \frac{V_{DD}^{\ 2}}{R_{LOAD\_SE}}$$

Equation 1

The task of the designer is to construct the impedance transformation block to present a desired differential load impedance to the output of the PA circuit, given knowledge of the target V_{DD} supply voltage. Silicon Labs states (without proof presented here) that the following differential load impedances are appropriate for obtaining the listed maximum output powers, for the specified values of V_{DD} supply voltage.

Table 2.2. Differential PA Load Impedance vs Output Power and VDD

P_{OUT}	V_{DD}	R_{LOAD_DIFF}
+20 dBm	3.3 V	100 to 125 Ω
+17 dBm	3.3 V	170 Ω
+14 dBm	1.8 V	100 to 125 Ω
+13 dBm	1.8 V	170 Ω
+10 dBm	1.7 V	220 Ω
0 dBm	1.7 V	330 Ω

From the values listed in the table above, it is apparent that one common RF match may (potentially) be used to obtain different output power levels, simply by changing the V_{DD} voltage supplied to the TX output pins. Although not shown in the table, it is often possible to obtain different output power levels for the same V_{DD} supply voltage, by changing the differential load impedance presented to the PA. For example, the table above shows that it is possible to obtain +14 dBm from the chip for V_{DD} = 1.8 V and a differential load impedance of 100 to 125 Ω. It is also possible to obtain +14 dBm from the chip for V_{DD} = 3.3 V and a differential load impedance of ~330 Ω. The PA current consumption from the 3.3 V supply will be less than the PA current consumption from the 1.8 V supply. However, the EFR32 family of chips provide for an on-chip DCDC Converter, and it is assumed that the 1.8 V (or 1.7 V) PA supply voltage will be obtained from the output of the DC-DC Converter, thus gaining the current efficiency of the converter (i.e., converting V_{BATT} = 3.3 V to V_{DD} = 1.8 V). In most cases, overall chip current consumption is minimized by using the DC-DC Converter as the voltage source for the PA for all applications with TX output power ≤+14 dBm. Moreover, with the DCDC the output power level is stable and immune against V_{DD} variations.

The output power levels shown in the table above are maximum power levels. For any given match and V_{DD} supply voltage, the TX output power can be reduced to a less-than-maximum value through the `SetPower(x)` Rail API command. The effect of such an API command is to reduce the number of enabled fingers in the output device(s), thus reducing the bias current and voltage swing across the presented differential load impedance. The designer does not have direct control over the number of enabled fingers of the output device(s), instead the `SetPower(x)` command adjusts the power level nearly to `x` dBm if the Silicon Labs reference matching designs given in Table 3.1 Summary of Matching Component Values vs. Frequency (CLNA = 1.0 pF) on page 25 are used with 125 Ω termination impedance and the VDD is 3.3 V. For the cases where the PA is fed from 1.8 V generated by the internal DCDC, the Radio Configurator window should be used in the Simplicity Studio to adjust the `SetPower(x)` Rail API command to the reduced power levels. In this case the maximum power is around 14 to 15 dBm, as shown in Table 2.2 Differential PA Load Impedance vs Output Power and VDD on page 11. With different matching impedances and with different V_{DD} values, the `SetPower(x)` command yields a power level, which deviates from `x` dBm.

The TX path of the impedance transformation network is shown in the figure below. It is clear that this network is a fully-differential PI-network (i.e., shunt-C, series-L, shunt-C). So it is the task of the designer to select values for CB, LMID, and CTUNE to transform 50 Ω (the impedance seen looking back into the balun and lowpass filter) into the desired differential TX load impedance, as listed in Table 2.2 Differential PA Load Impedance vs Output Power and VDD on page 11. This design task is readily accomplished with the aid of a Smith Chart or simple impedance matching application.

Two items present minor complications to this design task. First, one of the components of the PI-network is an adjustable capacitor bank (CTUNE, adjustable from ~2 to 7 pF) that is integrated into the RFIC. The value of CTUNE is set by the API and chip firmware for a value appropriate to support Silicon Labs' reference designs for a particular output power level and V_{DD} supply voltage. The integral CTUNE value can however be set and adjustable separately in both TX and RX modes by the SGPACTUNE register ("setpactune" command) in the RAILtest application, but Silicon Labs recommend to apply the default values set by the chip firmware (typically close to the minimum settings of CTUNE values). For applications at lower frequencies (≤ 390 MHz), the available adjustment range of CTUNE may not be sufficient to properly tune the PI-network match. In such cases, it may be necessary to augment the value of CTUNE by the addition of external discrete parallel capacitors to GND from the TX pins. Second, the internal bonding wire inductances (~1nH for RX LNA; ~1.5...2nH for TX PA) and board layout parasitics can significantly modify the discrete component values required to accomplish a desired impedance transformation. For example, the series inductance of the PCB traces and bonding wires may provide a significant portion of the required value of the LMID inductors. This series trace inductance should not be ignored or discounted, and may result in use of a lower value inductor for LMID than that predicted by Smith Chart matching calculations.

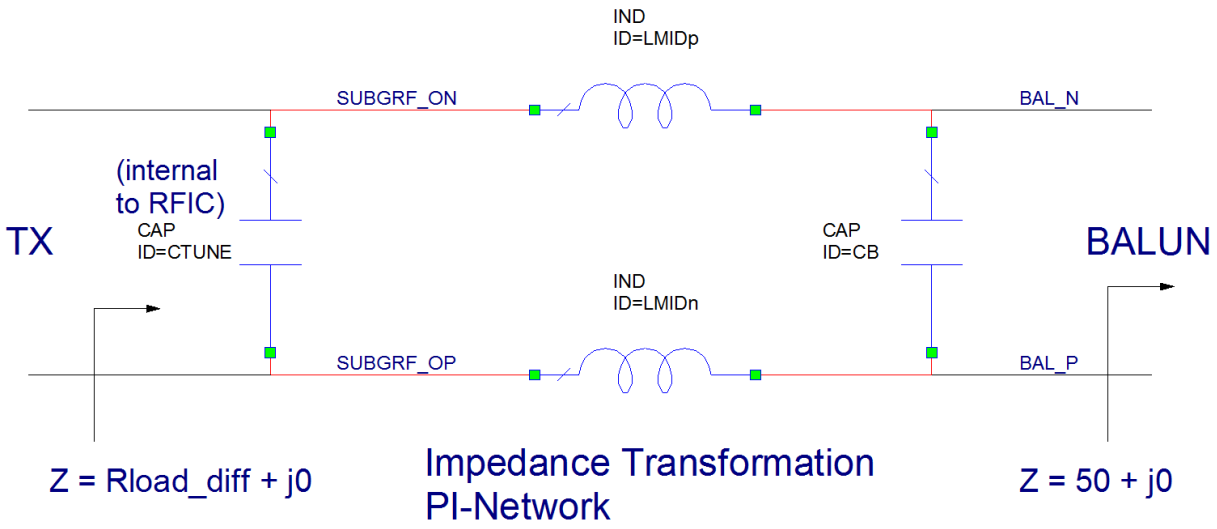
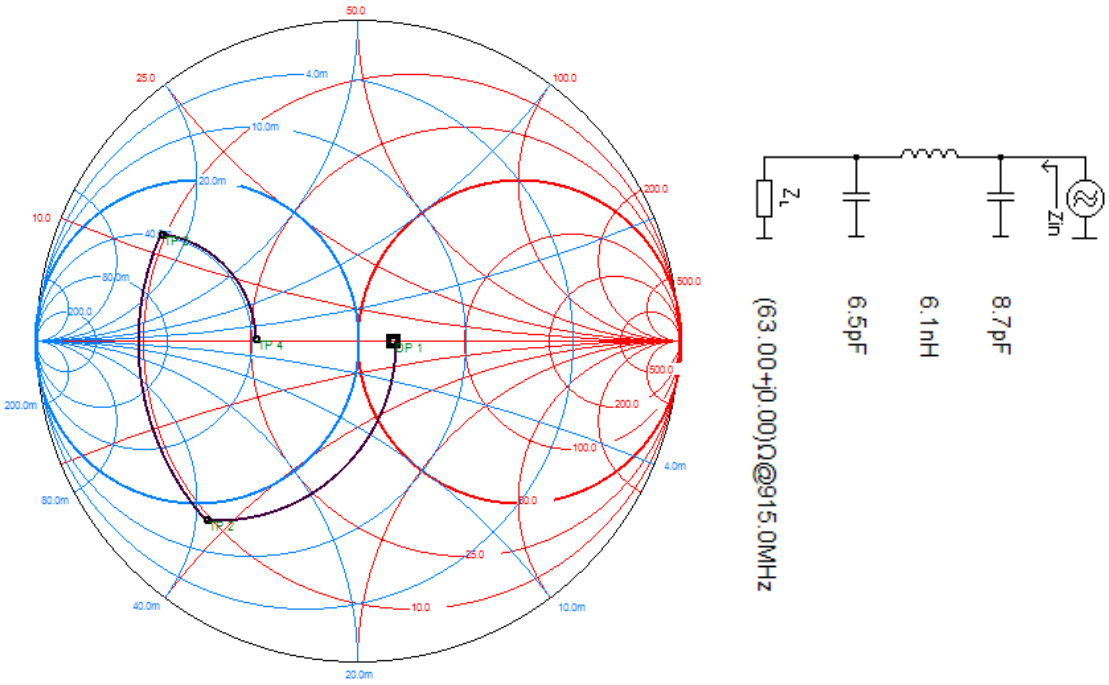


Figure 2.7. TX Impedance Transformation Network

The figure below shows a possible simplified matching process on Smith chart where one half of the differential PI network is matched between the half of the differential impedances i.e. between 50/2 = 25 Ω and 125/2 = ~63 Ω. This example applies ideal reactances. As mentioned above, with real SMD components and PCB parasitics the element values may differ significantly from the ideal values.

In the figure below, the half pi network uses 6.5 pF and 8.7 pF shunt capacitors. In the doubled differential network, where two halves are unified, the half of the shunt capacitor values are used i.e. 3.25pF and ~4.3pF. The resulted differential matching component values are shown in Figure 2.9 Calculated TX Match for Zload = 125 Ω at 915 MHz on page 13. It presents a differential load impedance of ~125 Ω to the PA output, while shows 50 Ω differential impedance for the balun at an operating frequency of 915 MHz. This solution is not unique; there are many possible combinations of CB-LMID-CTUNE that will transform 50 Ω to 125 Ω. However, this solution results in reasonable component values, using readily-available standard 5% tolerance values, with reasonable circuit Q-factor.



Point	Z	Q	Frequency
DP 1	(63.000 + j0.000) Ω	Q=0.000	915.0MHz
TP 2	(9.509 - j22.553) Ω	Q=2.372	915.0MHz
TP 3	(9.509 + j12.447) Ω	Q=1.309	915.0MHz
TP 4	(25.792 + j0.487) Ω	Q=0.019	915.0MHz

Figure 2.8. TX Match Process Demonstrated at 915 MHz with One-half of the Differential Network

Note: In the figure above, the half Pi network matches the 50/2 = ~25 Ω to Zload/2 = ~63 Ω.

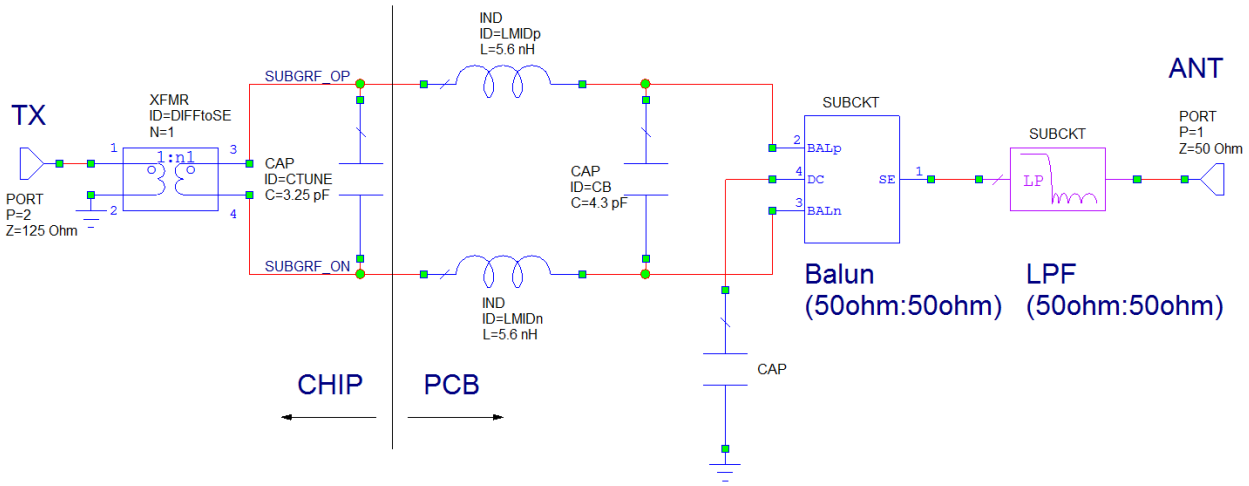


Figure 2.9. Calculated TX Match for Zload = 125 Ω at 915 MHz

Note: In the figure above, the component values are calculated and the bonding wire and PCB trace inductances are not taken into account. If modelling the on-chip, internal bonding wire inductances as well (in series with the LMID inductors on both differential ports between CTUNE and LMID components), then CTUNE capaciance should be set to ~2...2.5 pF (which is basically the minimum setting of SGPACTUNE register). Also, the tuned inductor values of LMID need to be decreased to compensate the bonding wire and external PCB trace inductances.

The simulated differential load impedance for this network is shown below, and is very close to the desired target value of 125 Ω. Note that the Smith Chart has also been normalized here to Zo = 125 Ω.

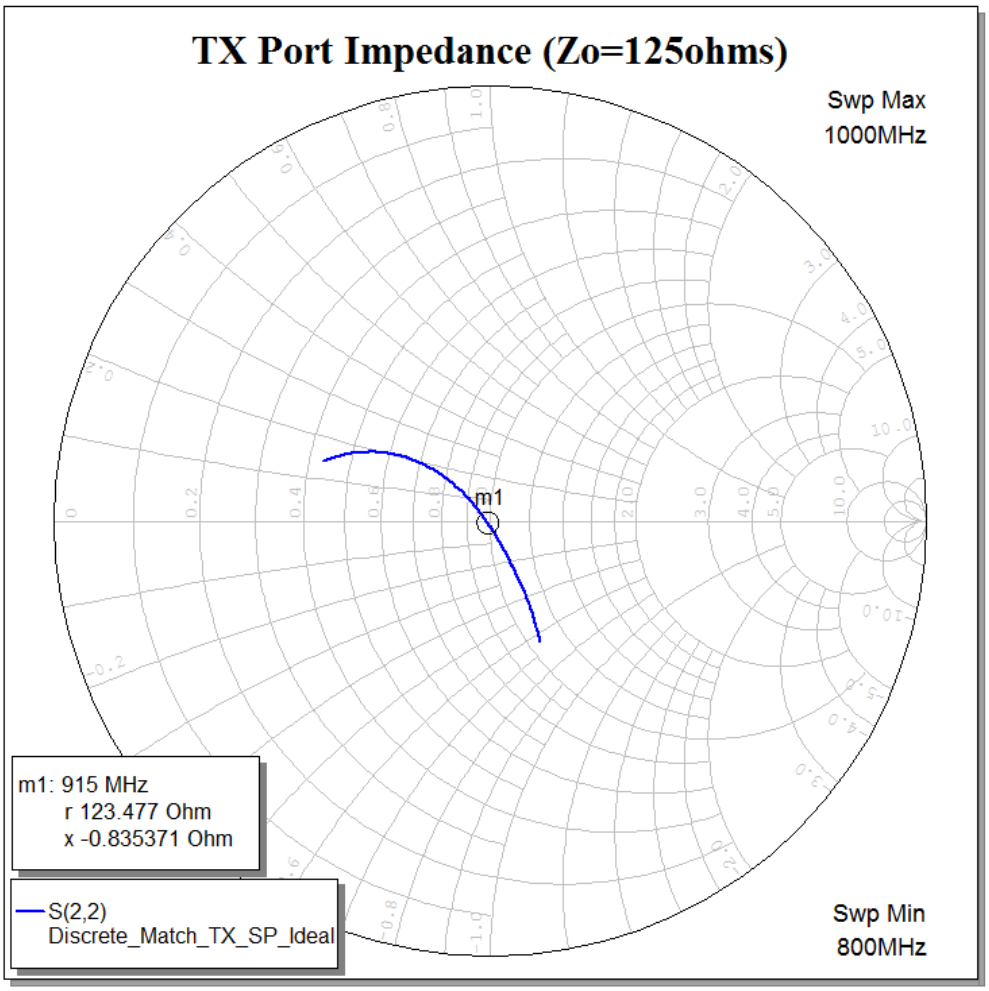


Figure 2.10. Differential TX Load Impedance at 915 MHz

If the user desires a TX-only application, the match topology of Figure 2.9 Calculated TX Match for Zload = 125 Ω at 915 MHz on page 13 is sufficient. A boundary line has been drawn in this plot to clearly show those components which lie outside the RFIC.

2.4.2 APC Mechanism

There is AC and DC detection and protection features and associated automatic power control (APC) mechanism applied on the PA output device, which protects the PA and help avoid long-term reliability issues (e.g., device damage, PA output power degradation in long term, and so on). The APC circuity monitors both AC and DC voltage on the device output. If one or both of the AC and DC thresholds is reached, the protection circuit kicks in and backs off the PA power level.

DC protection menchanism: The PA protection circuit kicks in above 3.6 V DC supply voltage on the PA to protect it for long-term reliability. DC protection (tries to) looks at the supply voltage on the PA, if it is >3.6 V, it will trip the comparator saying power is too high. The PA is specified for operation at max output power level of +20 dBm, so above 3.6 V DC voltage the PA backs off the power to not overshoot the specified +20 dBm power and therefore ensures long-term reliability. For DC protection, it "tries" because for 2.4 GHz, there is a separate PAVDD pin coming into the radio and feeding the 2.4 GHz PA. If the PAVDD DC voltage level is too high, PA back-off is triggered. However, for the sub-GHz radio font-end, PAVDD does not come into the radio. Instead, it connects to the drain of the output stage (at the TX pins) through a RF choke off chip. So, for sub-GHz DC protection, it uses AVDD, assuming AVDD = PA VDD for +20 dBm operation. Therefore, for the sub-GHz PA's protection circuit the DC voltage is monitored at the AVDD pin due to the lack of separate PAVDD pin for the sub-GHz PA. The default configuration for +20 dBm TX power assumes AVDD=PAVDD= DC voltage on the sub-GHz PA, so it reasonably backs off the power if the AVDD is above that given threshold (3.6 V DC voltage).

AC protection menchanism: An AC envelope detector monitors the AC swing at the device output and APC is triggered if the AC peak voltage hits a given threshold and backs-off the PA power level until the output voltage swing falls under that threshold. The AC threshold corresponds to about 6.67 V differential peak voltage at the PA. The APC circuitry can be triggered by AC over-voltage for several reason as follows. For example, PA load impedance is larger than the optimal values shown in Table 2.2 Differential PA Load Impedance vs Output Power and VDD on page 11, which can occur if, for example:

- The recommended matching BOM is not exactly followed using the Silicon Labs reference layout. For example, larger-valued series inductors are used in the TX match, not 50:50 ohms ceramic balun is used without re-tuning the match for the specific balun impedance, and so on.
- For custom matching designs, the bonding wire / PCB trace inductances are not taken into account.
- Improper RF layout drawing of the matching network, e.g., longer traces used between the matching components and RF chip.
- Antenna port is terminated by bad, too large, antenna VSWR (i.e., antenna mismatch).

The PA is sliced and striped for configuring and fine-setting. The PA has 8 slices with 31 stripes of each slice.

The APC mechanism is implemented in chip firmware and is used for protecting the PA, and therefore only implements the event when the high peak detector trips. If AC detection happens, the firmware gets an interrupt and backs off slices until the event is cleared. On the next packet, the slices are reseted to the programmed value and the mechanism lets the interrupt back off again if the overvoltage condition still exists. RAIL may not be kicking in the power adjustment after peak detection until next transmission (unless it was found during ramping).

If DC detection happens, the same logic is followed, but if this occurs the mechanism backs off one slice.

The thresholds cannot be programmed, since those are implemented in the chip firmware. However, a RAIL callback is available. When the PA protection kicks in, see RAIL_EVENT_PA_PROTECTION, also on CLI querying for "status" and counter PaProtect provides the count of times protection logic is kicked in.

If it is suspected that APC kicks in due to the higher impedance load at the PA (exceeding AC threshold) without any layout and matching BOM modification, the SGPACTUNE register value may be increased until the desired TXP is still achieved but without triggering the protection circuitry. This register write increases the parallel capacitance at the PA (CTUNE), would lower the impedance to have lower voltage peak, and could help avoid triggering the APC.

Typical TX output power versus power setting curve when APC kicks in can be seen in the Figure below. Sharp, discrete power back off can be observed as highlighted in blue. The APC circuitry kicks in when the AC threshold is reached and the protection circuitry backs off the power by one slice and starts increasing the stripe levels (when further increasing the power level) until the AC threshold is reached again where an additional slice is backed off. The level of the power back-off depends on the level of the over voltage (e.g., mismatch, antenna VSWR) condition. When the DC protection is kicking in, a similar power curve could observed with one back-off in power.

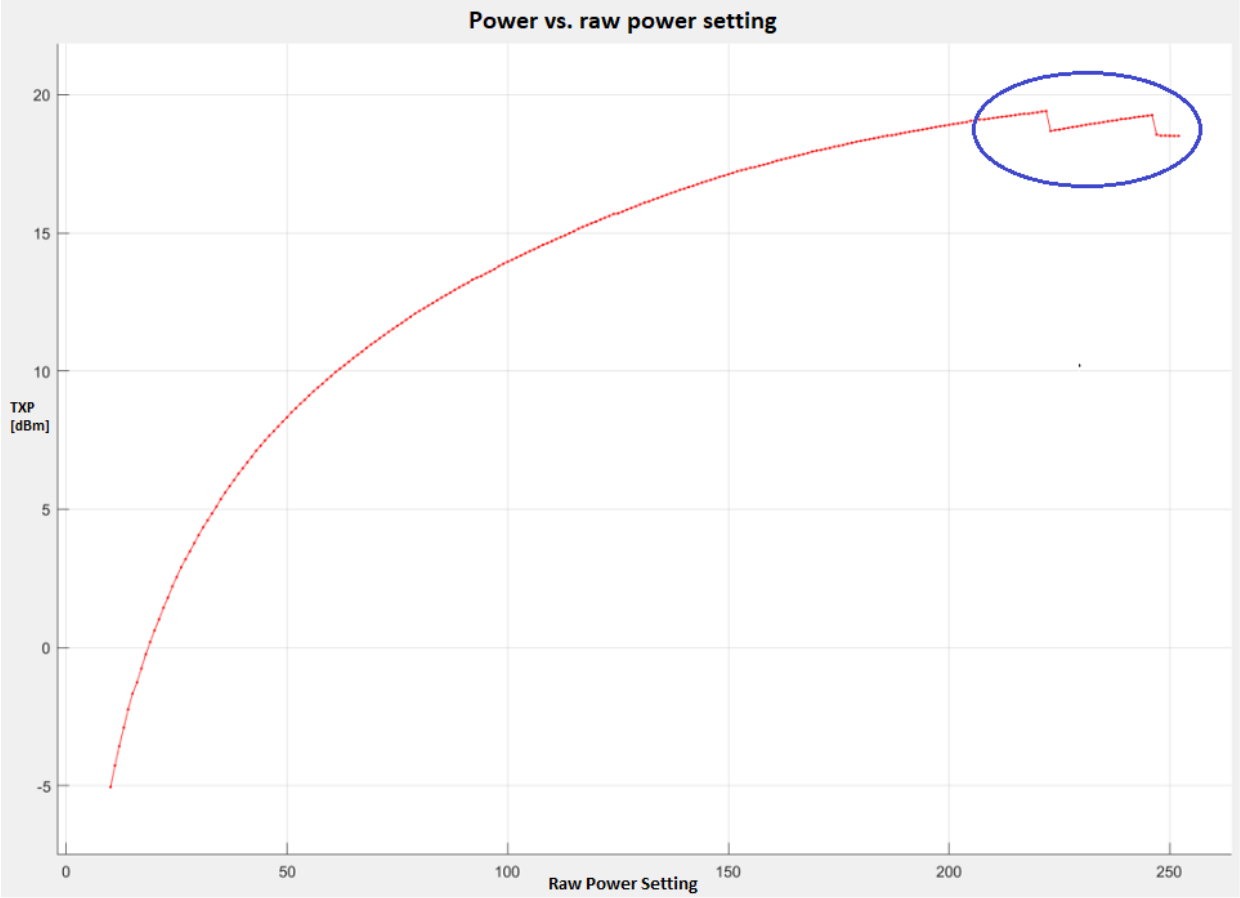


Figure 2.11. Typical TXP vs. Power Setting Curve when APC Kicks in

2.4.3 RX Signal Path and Match

The RX signal path makes use of all of the TX signal path and match presented in the previous section. The RX signal path "taps off" the end of the TX match and additionally provides a differential series-C, shunt-L impedance transformation network (refer back to Figure 2.6 Impedance Transformation Block Topology on page 10).

The differential RX input impedance of the EFR32 family of chips is very high, as shown in the Smith Chart admittance plot in the figure below. The RX input may be approximated by an equivalent circuit consisting of a high-value resistance (~5 kΩ to several 10's of kΩ) in parallel with a small capacitance (~0.76 pF to ~1pF), with the values varying somewhat as a function of frequency.

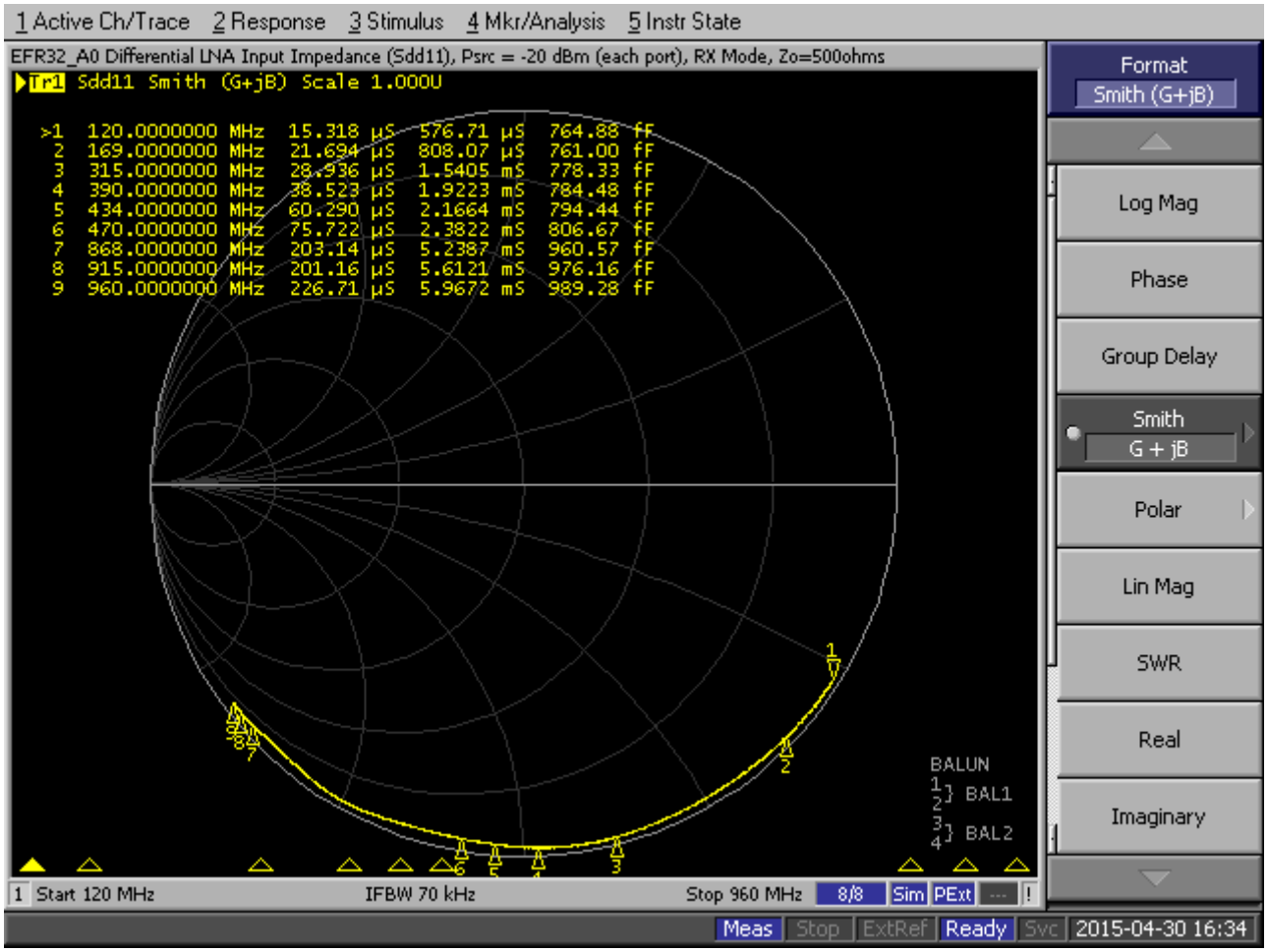


Figure 2.12. EFR32 Differential RX Input Admittance

Due to the high value of equivalent parallel resistance (~5 kΩ at 915 MHz), Silicon Labs makes no attempt to construct a true complex conjugate match at the RX interface. Such an extreme impedance transformation ratio (e.g., ANT=50 Ω to RX=5000 Ω) would require an extremely high-Q, narrowband, and difficult-to-tune matching network. The LNA circuitry acts more as a voltage amplifier than a power amplifier, and thus less emphasis is placed on maximum power transfer to the LNA input and more emphasis is placed on the passive voltage gain of the RX matching network. A large value of passive voltage gain in the match network, prior to the active circuitry of the LNA, helps suppress the 2nd-stage contributions of noise from the LNA and downstream circuits, as expressed in Friis' Equation:

$$F_{TOTAL} = F_1 + \left(\frac{F_2 - 1}{G_1}\right)$$

Equation 2

The concept of passive voltage gain is simple: if a lossless network is used to accomplish an impedance transformation (from Z1 to Z2), the power gain (or loss) through the network is zero, but the voltage at the terminals of the network are different. If Z2 > Z1, then mathematically,

$$Z_2\left(=\frac{V_2}{I_2}\right) > Z_1\left(=\frac{V_1}{I_1}\right) \rightarrow V_2 > V_1$$

Equation 3

Referring back to Figure 2.6 Impedance Transformation Block Topology on page 10, the impedance transformation ratio of the RX portion of the match (and thus its passive voltage gain) is set by the LGATE:CSER ratio. This is demonstrated using the simple AC test bench of the figure below, in which the LGATE:CSER ratio is swept while maintaining (approximately) a constant LGATE*CSER product. The resulting AC voltage gain curves are shown in Figure 2.14 RX Passive Voltage Gain vs LGATE:CSER Ratio on page 19.

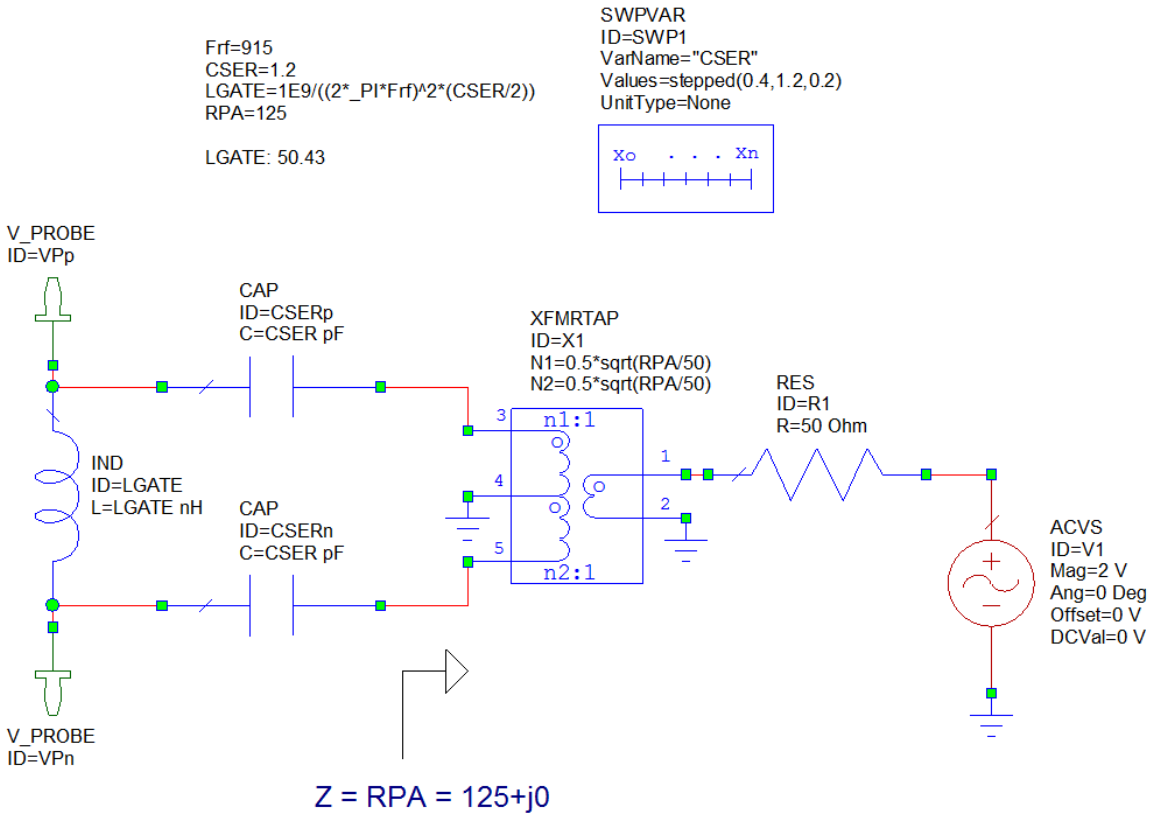


Figure 2.13. RX Gain Test Bench

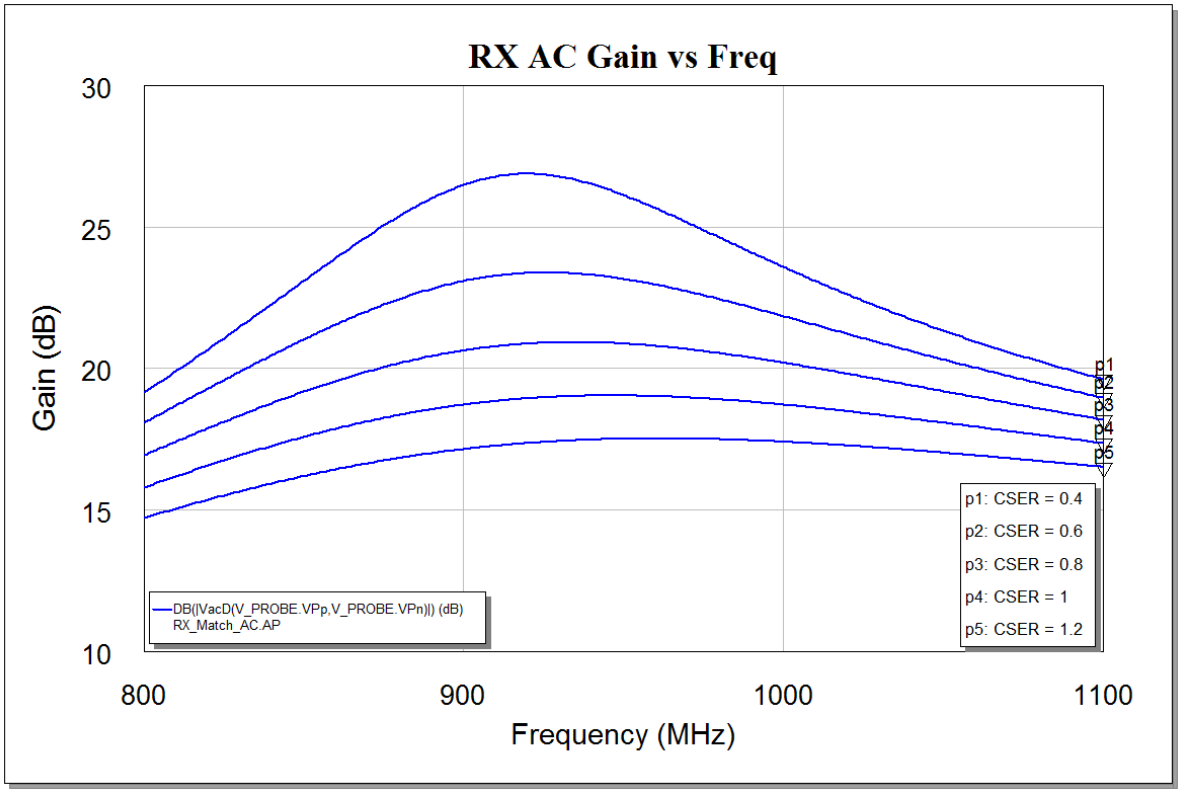


Figure 2.14. RX Passive Voltage Gain vs LGATE:CSER Ratio

The reader is cautioned against designing for extremely large values of RX voltage gain through use of very large LGATE:CSER ratios. The resulting design may have a very narrowband frequency response and may be difficult to tune due to the very small value of capacitance and/or large value of inductance. Additionally, the finite Q-factor of the inductor (as well as the input resistance of the LNA) will limit the maximum achievable gain (an effect not shown in the ideal simulation of Figure 2.14 RX Passive Voltage Gain vs LGATE:CSER Ratio on page 19). For this reason, use of a high-quality inductor (i.e., wire-wound inductor) is recommended for LGATE.

As shown in the admittance plot of Figure 2.12 EFR32 Differential RX Input Admittance on page 17, the differential RX input of the EFR32 family of chips may be viewed as a large-value resistance in parallel with a small-value capacitance. A more accurate representation of the RX match is shown in Figure 2.15 RX Match (Including RLNA and CLNA) on page 20. This schematic demonstrates that while only one discrete parallel inductance (LGATE) is used in the actual match, it may be viewed as consisting of two inductors in parallel, where

$$L_{GATE} = L_{LNA} \,//\, L_{SH}$$

Equation 4

The LLNA component of the inductance parallel-resonates with CLNA at the desired frequency of operation and effectively cancels it, leaving the LSH component of inductance to work with CSER to accomplish the RX impedance transformation and passive voltage gain.

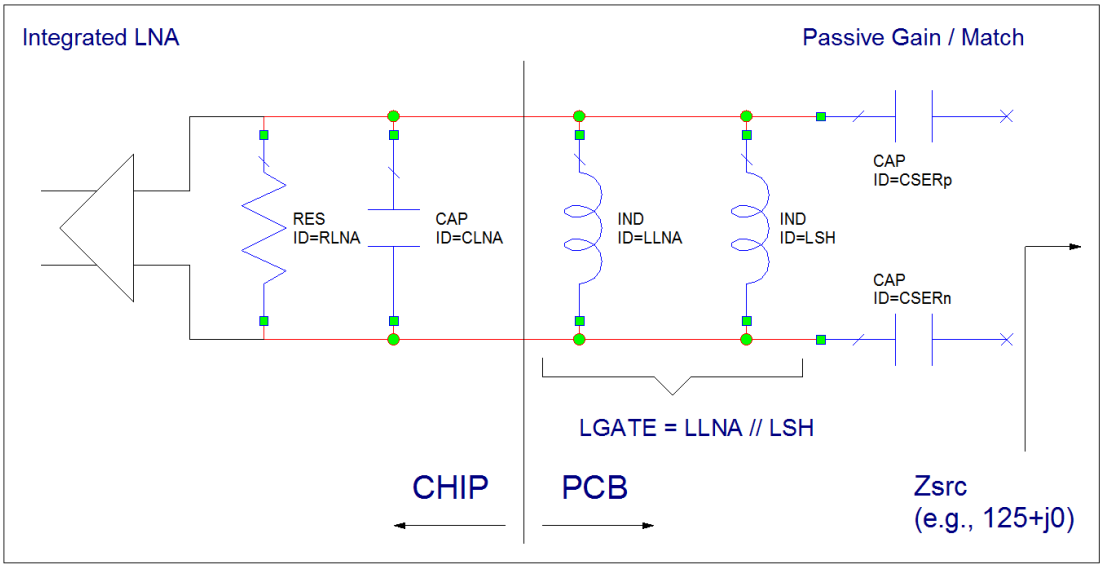


Figure 2.15. RX Match (Including RLNA and CLNA)

Although not demonstrated here, it may be shown that the overall frequency response of the RX match becomes more narrowband as the value of CLNA is increased. As the total value of CLNA is the sum of LNA input capacitance plus parasitic capacitance from PCB traces and pads, it is thus to the designer's advantage to minimize CLNA through optimization of the PCB layout. The value of CLNA (0.76pF to 0.99pF, as a function of frequency) shown in the admittance plot of Figure 2.12 EFR32 Differential RX Input Admittance on page 17 represents its minimum possible value, as the measurement was taken with all PCB traces and pads removed and thus represents the value of the LNA input capacitance by itself. A value of CLNA = 1.0 pF is reasonable for highly-optimized board layouts, while a value of CLNA = 1.25 pF may be appropriate for less-optimal board layouts.

Just as there was no single, unique solution for the CB-LMID-CTUNE TX impedance transformation path (refer to Figure 2.9 Calculated TX Match for Zload = 125 Ω at 915 MHz on page 13), there is also no unique solution for LGATE and CSER in the RX matching path. As discussed above, the designer may (within reasonable limits) adjust the LGATE:CSER ratio to trade off the bandwidth of the RX frequency response for the transformed RX impedance and magnitude of passive voltage gain. Given the value of CLNA, it is a simple matter to calculate the inductance LLNA required to parallel-resonate CLNA at the desired frequency of operation:

$$L_{LNA} = \frac{1}{\omega_{RF}^{2} * C_{LNA}}$$

Equation 5

Continuing the design example at 915 MHz with CLNA = 1.0 pF, the calculated value of LLNA = 30.25 nH.

The calculation of LSH is unfortunately not as simple. A reasonable target LGATE:CSER ratio must first be selected using a combination of simulation, bench experience, or guidance from Silicon Labs (as provided within this application note). A trial value of CSER is next selected as the starting point for the remaining calculations. For the design example at 915 MHz, Silicon Labs states that CSER = 1.8 pF is a reasonable selection.

The value of LSH that resonates with CSER is subsequently calculated. As the two CSER capacitors in the differential RX match of Figure 2.15 RX Match (Including RLNA and CLNA) on page 20 are effectively in series with LSH (after cancellation of CLNA by LLNA), it would at first glance seem that the required value of LSH is simply that which resonates with 0.5 x CSER at the desired frequency of operation. However, this is not correct; it neglects the effect of ZSRC upon the resonance of the circuit.

The two CSER capacitors appear in series with the source resistance, i.e., the transformed impedance resulting from the TX portion of the match. Continuing the design example at 915 MHz, this was ZSRC = ZTX = ~125 + j0 Ω (refer back to Figure 2.9 Calculated TX Match for Zload = 125 Ω at 915 MHz on page 13 and Figure 2.10 Differential TX Load Impedance at 915 MHz on page 14). Prior to calculation of the value for LSH, it is first necessary to transform this series R-C network into an equivalent parallel R-C network. Mathematically,

$$Q = \frac{1}{R_{SRC}{}^{*}\omega_{RF}{}^{*}(0.5{}^{*}C_{SER})}$$

Equation 6

$$C_{SER\text{-}SH} = \frac{0.5{}^{*}C_{SER}}{1 + \left(\frac{1}{Q}\right)^{2}}$$

Equation 7

$$L_{SH} = \frac{1}{\omega_{RF}{}^{2}{}^{*}C_{SER\text{-}SH}}$$

Equation 8

Continuing the design example at 915 MHz with RSRC = 125 Ω and CSER = 1.8 pF, this results in LSH = 47.68 nH. It is then a simple matter to use Equation 4 to determine the value of LGATE = 18.51 nH.

The values shown in the table below represent one possible set of solutions for RX matching component values, assuming CLNA = 1.0 pF and RSRC = 125 Ω. The RX matching network's RLNA impedance can be calculated from the table below by the equation of RLNA=(1+Q^2)*RSRC. This load impedance is shown at the LNA side by the matching network applied on the Silicon Labs reference radio boards and is approximately (with ideal elements) from 3200 Ω (at 169 MHz) down to 450 Ω (at 915 MHz) and function of frequency. As mentioned previously, this is not a unique set of solutions. For example, if the value of CSER had been chosen instead as CSER = 1.2 pF, the calculated required value for LGATE at 915 MHz would be 20.09 nH. Both solutions easily provide acceptable performance.

Alternatively, if the assumed value of CLNA had been increased to CLNA = 1.25 pF (i.e., due to increased trace and pad parasitics), one possible solution at 915 MHz would be calculated as CSER = 0.9 pF and LGATE = 18.25 nH.

The deciding factor in choosing one solution over another is often how close the calculated component values fall near standard tolerance values (e.g., 5% tolerance parts).

Table 2.3. Example LGATE:CSER Calculations vs Frequency (RSRC=125 Ω)

Freq	C_{SER}	Q	C_{LNA}	L_{LNA}	L_{SH}	L_{GATE}
915 MHz	1.8 pF	1.546	1.0 pF	30.25 nH	47.68 nH	18.51 nH
868 MHz	1.6 pF	1.834	1.0 pF	33.62 nH	54.53 nH	20.80 nH
490 MHz	1.6 pF	3.248	1.0 pF	105.5 nH	144.4 nH	60.96 nH
434 MHz	1.6 pF	3.667	1.0 pF	134.5 nH	180.6 nH	77.08 nH
315 MHz	1.8 pF	4.491	1.0 pF	255.3 nH	297.7 nH	137.4 nH
170 MHz	3.0 pF	4.993	1.0 pF	876.5 nH	607.8 nH	358.9 nH

2.4.4 Interaction of TX and RX Signal Paths

To this point, there has been no discussion of how the TX and RX signal paths may be directly tied (as shown in Figure 2.6 Impedance Transformation Block Topology on page 10) while still “playing nicely” together. That topic is now considered.

The TX signal path and match heavily influences the RX performance, while the RX signal path and match only weakly affects the TX performance. The recommended design approach is therefore to construct the match for the TX path first, followed by the addition of the RX match.

The PA output impedance of the EFR32 family chips may be viewed as a moderate-value resistance (500 to 1000 Ω) in parallel with the integrated CTUNE tuning capacitor. The value of the PA equivalent parallel output resistance varies somewhat depending upon whether the PA circuit is enabled or disabled (i.e., TX or RX mode). However, the variation is not large, and as the PA output resistance is typically several times larger than the desired PA load impedance (e.g., 125 Ω), it may be ignored in the matching process as a first-order approximation. That is to say, the source resistance seen by the RX match (CSER and LGATE, as seen in Figure 2.15 RX Match (Including RLNA and CLNA) on page 20) is primarily determined by the TX match (CB, LMID, and CTUNE).

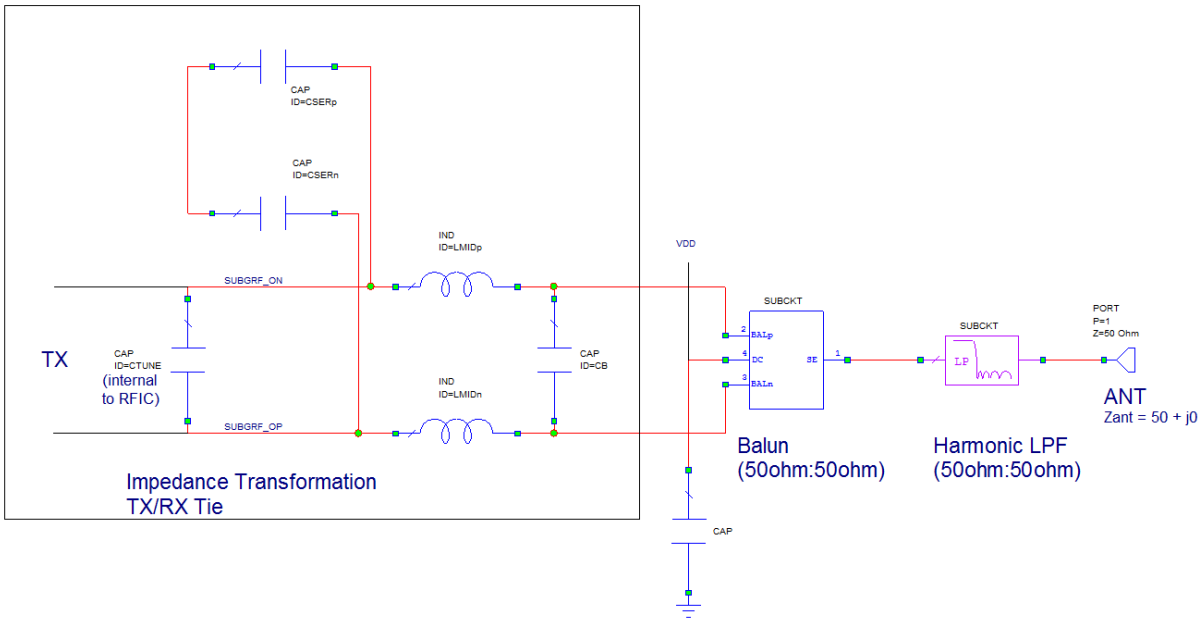


Figure 2.16. Effective Matching Network in TX Mode

The RX match, however, does provide a small additional load on the TX signal path. As shown in Figure 2.2 General Topology of sub-GHZ RF Match on page 4, a switch is integrated inside the EFR32 chip across the RX input pins. The switch is open while in RX mode but closed in TX mode, thus shorting the RX input pins together and shorting across CLNA and LGATE. This effectively places the two CSER capacitors in series with one another, and in parallel across the TX pins, as shown in Figure 2.5 Typical Performance through LPF + Balun (915 MHz, N = 5, 0900BL15C050 Balun) on page 9. In this fashion, the effective value of the CTUNE tuning capacitor is increased by approximately 0.5 x CSER while in TX mode.

This switch helps isolate the TX and RX signal paths, and attenuates the amplitude of the TX signal swing that is observed across the RX input pins.

3. Putting it All Together

The previous sections have discussed the design procedures for each of the sub-blocks (lowpass filter, balun, and impedance transformation network) of the complete match. The topology of the entire discrete matching network for an application at 868 MHz or 915 MHz is shown in Figure 2.6 Impedance Transformation Block Topology on page 10. The topology of the matching network for applications in lower frequency bands is shown in Figure 2.7 TX Impedance Transformation Network on page 12.

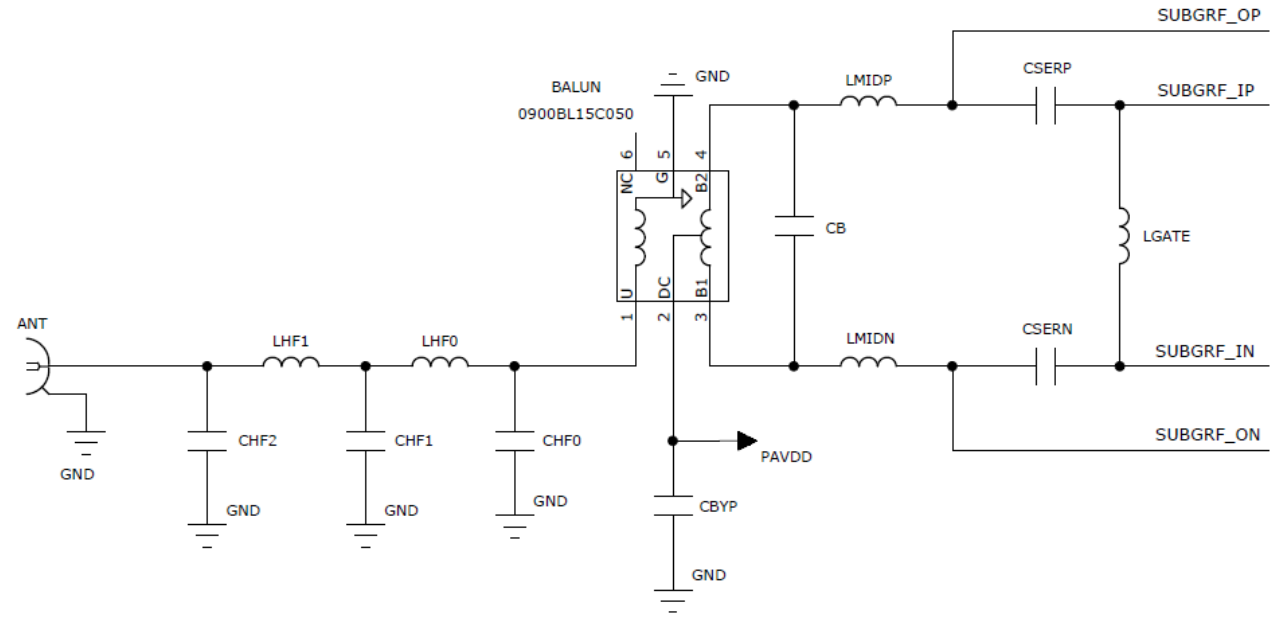


Figure 3.1. Complete Match Network Topology for 868 M/915 M

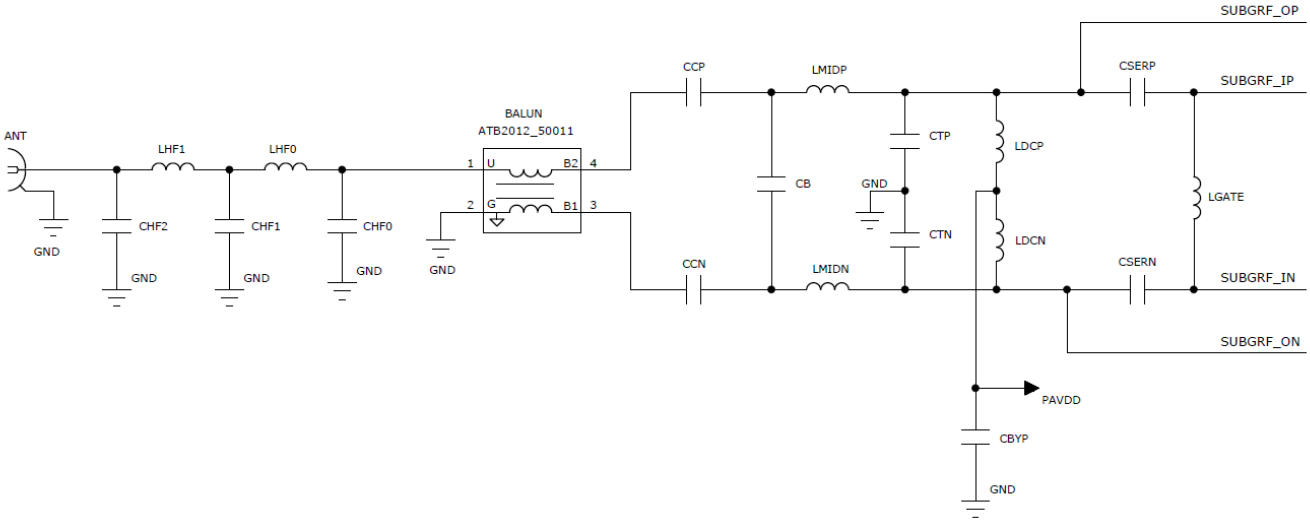


Figure 3.2. Complete Match Network Topology for 169 M/315 M/434 M/490 M

The high-band and the low-band matching topologies differ in the following respects:

- The low-band match includes pull-up inductors LDCP and LDCN, as a suitable balun with center tap (for the DC feed function) was not identified by Silicon Labs for use in low-band applications. These inductors should be high-value (e.g., 470 nH) with low DC winding resistance (e.g., Murata LQW18CNR47).
- The low-band match includes DC blocking capacitors CCP and CCN. The balun selected by Silicon Labs for use in low-band applications provides DC continuity between the primary and secondary windings, and thus DC blocking capacitors must be used else VDD will be shorted to ground through the balun. These capacitors may be removed if a balun with no DC continuity between windings is selected. The value of the capacitors should be selected to provide very low AC impedance while remaining below the series-resonant frequency of the capacitor.
- The low-band match includes provisions for additional tuning capacitors CTP and CTN. These additional capacitors will likely be needed only for applications at ≤ 315 MHz. At such low frequencies, the range of the internal PA tuning capacitor CTUNE may not be sufficient and may need to be augmented by these external discrete capacitors.
- The low-band match applies 7th-order filter at some bands.

The reader may desire to use the equations and design process discussed within this application note to construct an entirely new match. However, many other readers may simply desire a tabulated list of component values for matches and applications already developed by Silicon Labs. For these readers, the following tables are provided.

The component values required for the various lowpass filter section(s) were previously summarized in Table 2.1 Lowpass Filter Component Values vs. Frequency on page 6, and are not reproduced here in the interest of brevity. To date, Silicon Labs has used two different baluns, depending upon the frequency of the application. The 0900BL15C050 balun from Johanson Technology (JTI) has been used for high-band designs (868M/915M/950M0, while the ATB2012_50011 balun from TDK has been used in all other designs.

As discussed in 2.4.3 RX Signal Path and Match, the value of CLNA has an effect upon the component values in the RX section of the match (e.g., CSER and LGATE). The optimized layouts used by the Silicon Labs reference designs and also described in AN928.1: EFR32 Series 1 Layout Design Guide has quite low PCB parasitics between the RX pins and thus, the matching element values can be calculated assuming CLNA=1pF. The element values for this case is summarized in Table 3.1 Summary of Matching Component Values vs. Frequency (CLNA = 1.0 pF) on page 25. The last column shows, whether the match is already bench tuned and tested or not. The tested boards are fully characterized by Silicon Labs. The not tested matches can be used as a starting point for bench evaluation.

In the Silicon Labs reference design layouts the ground metallization of the inner PCB layers are eliminated beneath the RX match area to reduce the parasitic capacitance between the RX pins, as shown in the figure below. The CLNA = 1 pF value can be maintained only with this trick using Silicon Labs reference board thickness of 1.6 mm. Thinner board designs may create higher parasitic capacitance so fine-tuning of the RX matching network may be required compared to the CLNA = 1 pF reference matching circuit values.

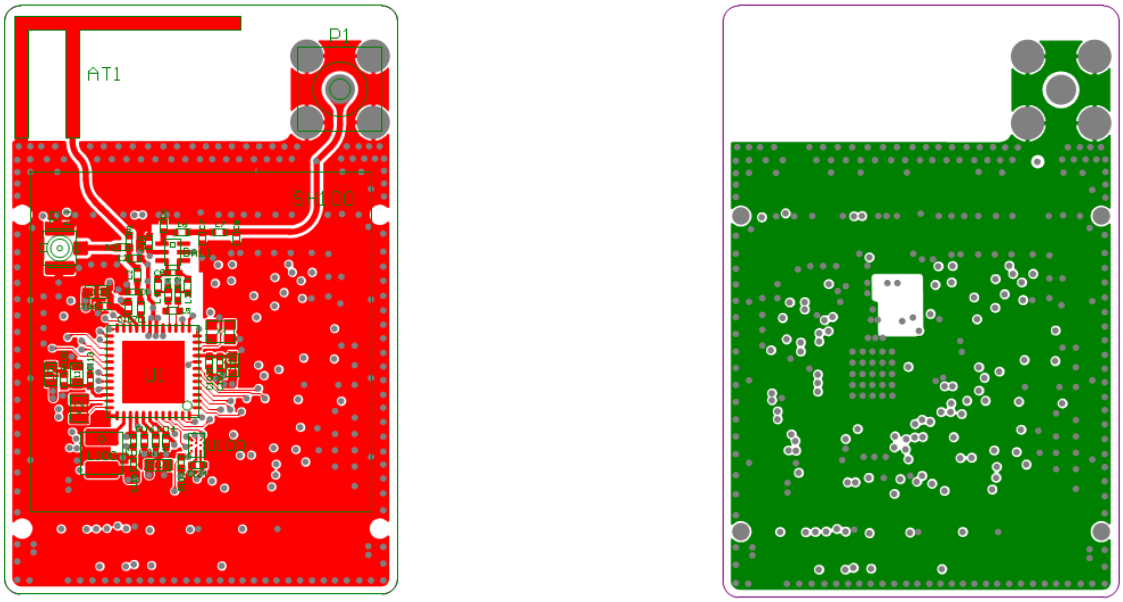


Figure 3.3. Elimination of the GND Metallization in the Inner Layers Beneath the RX Match Area

If the inner layer metallization cannot be eliminated due to any reason (or having board thickness much smaller than 1.6 mm, i.e. < 0.8 mm) the CLNA increases and will be close to 1.25 pF. The corresponding component values for CLNA=1.25pF case are summarized in Table 3.2 Summary of Matching Component Values vs. Frequency (CLNA = 1.25 pF) on page 26 below. Unfortunately, these match values were not bench tested yet. In simulations they yield slightly worse RF performances (lower TX powers, worse sensitivities, and narrower bandwidths).

As an example the final schematic of the 868 MHz/2.4 GHz and 169MHz /2.4 GHz dual band boards are given in Appendix 1. Schematics.

The measured result of the tested boards in TX mode are summarized in Table 3.3 Summary of Matching RF performance in TX mode (CLNA = 1.0 pF) on page 26. In RX mode the sensitivity data given in the datasheet are valid for all matches.

Table 3.1. Summary of Matching Component Values vs. Frequency (CLNA = 1.0 pF)

Freq Band	P_{OUT}	PAVDD	LGATE	CSER	LMID	CB	CT	LDC	BALUN	LPF	Tested
169 MHz	20 dBm	3.3 V	390 nH	3.0 pF	36 nH	10 pF	13 pF	470 nH	TDK	N = 7	Y
	10 dBm	1.7 V	390 nH	3.0 pF	51 nH	12 pF	10 pF	470 nH	TDK	N = 3	Y
230 MHz	20 dBm	3.3 V	200 nH	3.0 pF	23 nH	3.9 pF	5.6 pF	470 nH	TDK	N=7	Y
262 MHz	20 dBm	3.3 V	150 nH	3.0 pF	19 nH	3.9 pF	12 pF	470 nH	TDK	N=7	Y
315 MHz	14 dBm	1.8 V	120 nH	2.7 pF	18 nH	3.9 pF	3.3 pF	470 nH	TDK	N = 7	Y
345 MHz	20 dBm	3.3 V	120 nH	1.8 pF	18 nH	2.0 pF	5.6 pF	470 nH	TDK	N=7	N
	10 dBm	1.8 V	120 nH	1.8 pF	22 nH	2.0 pF	5.6 pF	470 nH	TDK	N=5	N
434 MHz	14 dBm	1.8 V	75 nH	1.8 pF	13 nH	2.7 pF	N/A	470 nH	TDK	N = 5	Y
	10 dBm	1.7 V	75 nH	1.6 pF	18 nH	4.7 pF	N/A	470 nH	TDK	N = 5	Y
490 MHz	20 dBm	3.3 V	62 nH	1.6 pF	9.1 nH	3.3pF	N/A	470 nH	TDK	N = 5	Y
868 MHz	20 dBm	3.3 V	18 nH	1.9 pF	3.3 nH	3.9 pF	N/A	N/A	JTI	N = 5	Y
	14 dBm	1.8 V	18 nH	1.9 pF	3.3 nH	3.9 pF	N/A	N/A	JTI	N = 5	Y
915 MHz	20 dBm	3.3 V	18 nH	1.8 pF	3.3 nH	3.9 pF	N/A	N/A	JTI	N = 5	Y
	13 dBm	1.7 V	18 nH	1.8 pF	3.3 nH	3.9 pF	N/A	N/A	JTI	N = 3	N
950 MHz	13 dBm	1.7 V	TBD	TBD	TBD	TBD	N/A	N/A	JTI	N = 3	N

Table 3.2. Summary of Matching Component Values vs. Frequency (CLNA = 1.25 pF)

Freq Band	P_{OUT}	PAVDD	LGATE	CSER	LMID	CB	CT	LDC	BALUN	LPF	Tested
169 MHz	20 dBm	3.3 V	330 nH	3.0 pF	36 nH	10 pF	13 pF	470 nH	TDK	N = 7	N
	10 dBm	1.7 V	330 nH	3.0 pF	43 nH	12 pF	11 pF	470 nH	TDK	N = 3	N
315 MHz	14 dBm	1.8 V	120 nH	1.8 pF	22 nH	5.1 pF	2.7 pF	470 nH	TDK	N = 5	N
434 MHz	14 dBm	1.8 V	75 nH	1.0 pF	15 nH	2.7 pF	N/A	470 nH	TDK	N = 5	N
	10 dBm	1.7 V	75 nH	1.0 pF	18 nH	3.0 pF	N/A	470 nH	TDK	N = 3	N
490 MHz	20 dBm	3.3 V	62 nH	1.0 pF	9.1 nH	3.3 pF	N/A	470 nH	TDK	N = 5	N
868 MHz	20 dBm	3.3 V	20 nH	0.9 pF	4.3 nH	4.7 pF	N/A	N/A	JTI	N = 5	N
	14 dBm	1.8 V	20 nH	0.9 pF	4.7 nH	4.7 pF	N/A	N/A	JTI	N = 5	N
915 MHz	20 dBm	3.3 V	18 nH	0.9 pF	3.9 nH	4.3 pF	N/A	N/A	JTI	N = 5	N
	13 dBm	1.7 V	18 nH	0.9 pF	3.9 nH	4.3 pF	N/A	N/A	JTI	N = 3	N
950 MHz	13 dBm	1.7 V	TBD	TBD	TBD	TBD	N/A	N/A	JTI	TBD	N

Table 3.3. Summary of Matching RF performance in TX mode (CLNA = 1.0 pF)

Freq Band	P_{OUT_GOAL}	P_{AVDD}	Pfund	$P2^{nd}$	$P3^{rd}$	Ipa
169 MHz	20 dBm	3.3 V	19.9 dBm	–58 dBm	–62 dBm	76 mA
	10 dBm	1.7 V	10 dBm	–59 dBm	–47 dBm	14 mA
230 MHz	20 dBm	3.3 V	20.7 dBm	-47.9 dBm	-56.4 dBm	87.7 mA
262 MHz	20 dBm	3.3 V	20.0 dBm	-55.4 dBm	-59.1 dBm	87.8 mA
315 MHz	14 dBm	1.8 V	14 dBm	–59 dBm	–66 dBm	39.6 mA
434 MHz	14 dBm	1.8 V	14.1 dBm	–55 dBm	–60 dBm	37.3 mA
	10 dBm	1.7 V	10 dBm	–62 dBm	–66 dBm	14.7 mA
490 MHz	20 dBm	3.3 V	19.9 dBm	–57 dBm	–62 dBm	77 mA
868 MHz	20 dBm	3.3 V	19.9 dBm	–32 dBm	–64 dBm	85 mA
	14 dBm	1.8 V	14 dBm	–45 dBm	–70 dBm	40.5 mA
915 MHz	20 dBm	3.3 V	20.1 dBm	–34 dBm	–51 dBm	86 mA
	13 dBm	1.7 V	TBD	TBD	TBD	TBD
950 MHz	13 dBm	1.7 V	TBD	TBD	TBD	TBD

Appendix 1. Schematics

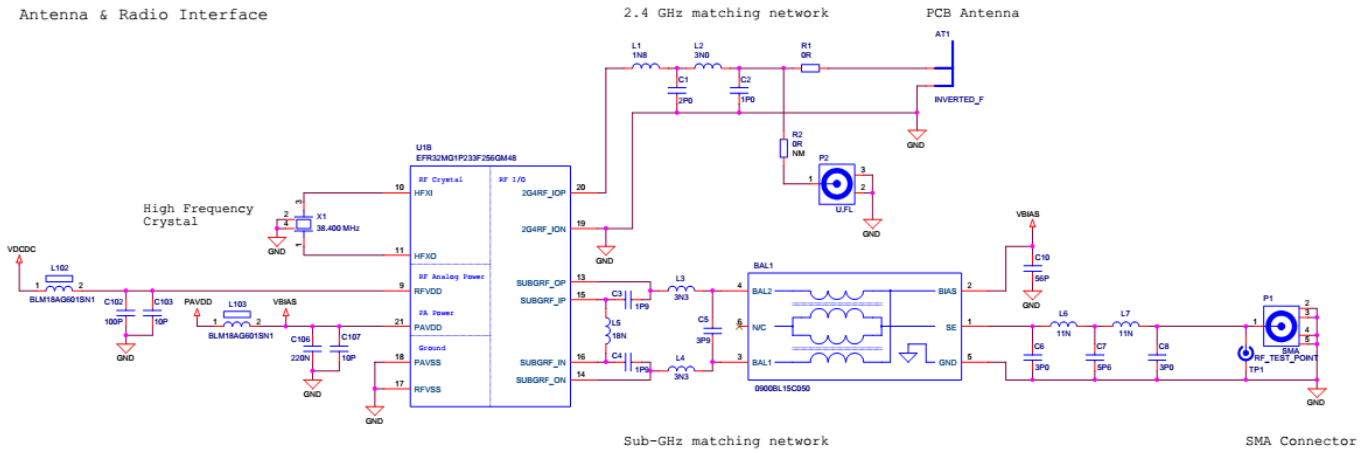


Figure 1.1. 868 MHz / 2.4 GHz Dual Band Board Schematic

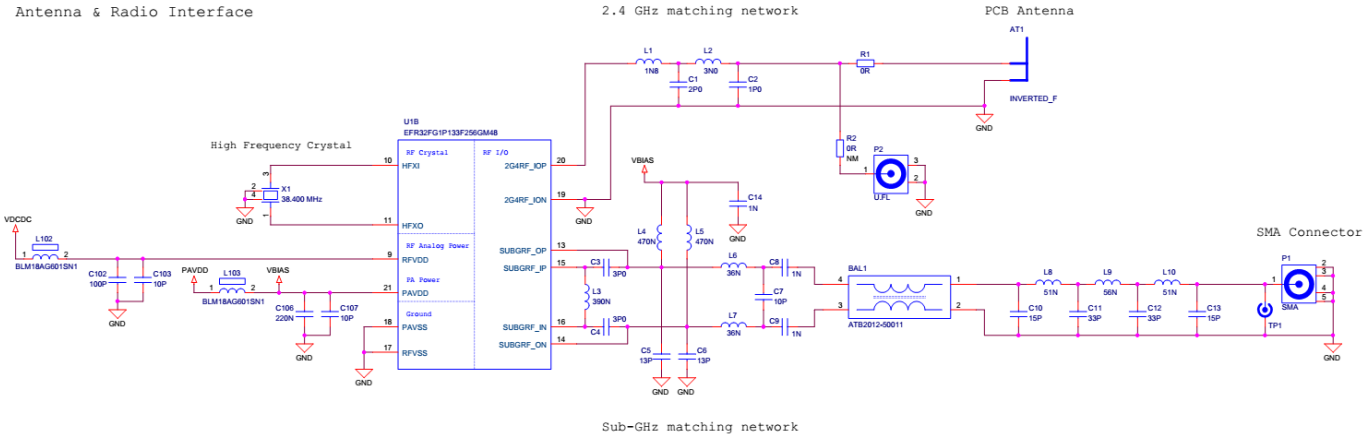


Figure 1.2. 169 MHz / 2.4 GHz Dual Band Board Schematic

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