AN928.3: Series 3 Layout Design Guide

The purpose of this application note is to help users design PCBs for the Series 3 devices using design practices that allow for good RF performance.

The matching principles for the 2.4 GHz Series 3 wireless MCUs are described in the application note, AN930.3: Series 3 2.4 GHz Matching Guide.

The Silicon Labs MCU and Wireless Starter Kits and Simplicity Studio provide a powerful development and debug environment. To take advantage of the capabilities and features on custom hardware, Silicon Labs recommends including debugging and programming interface connector(s) in custom hardware designs. The details and benefits of including these connector interfaces are detailed in AN958: Debugging and Programming Interfaces for Custom Designs.

The power supply configurations of Series 3 are described in AN0002.3: Series 3 Hardware Design Considerations. The RF performance strongly depends on the PCB layout, as well as the design of the matching networks. For optimal performance, Silicon Labs recommends using the PCB layout design guidelines described in the following sections.

KEY POINTS

- Provides a reference schematic and PCB layout
- Lists and describes all main design principles

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1. Device Compatibility

This application note supports the following devices:

- Series 3:
  - SiMG301
  - SiBG301

2. Design Recommendations When Using Series 3 Wireless MCUs

Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended that designers use the reference designs as-is since they minimize detuning effects caused by parasitics or generated by poor component placement and PCB routing. Series 3 reference design files are available in Simplicity Studio under the Kit Documentation tab. The compact RF part of the designs (excluding the 50 Ω single-ended antenna) is highlighted by a blue frame, and it is strongly recommended to use the same framed RF layout in order to avoid any possibility of detuning effects. The figure below shows the framed compact RF part of the designs.

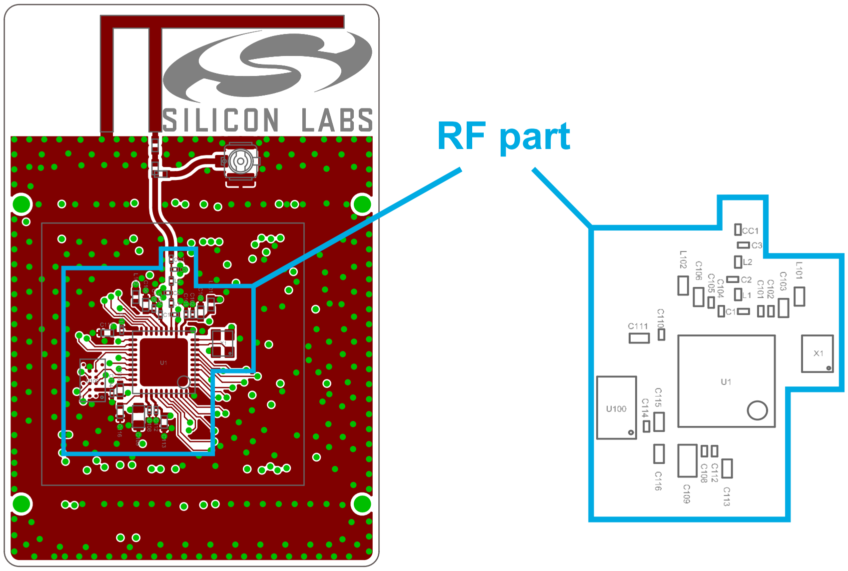

Figure 2.1. Top Layer of BRD4408A (SiXG301) Radio Board (Left Side) and Assembly Drawing of the RF Part (Right Side)

The layout of the MCU VDD filtering capacitors should also be copied from the reference design as much as possible. When layouts cannot be followed as shown by the reference designs (due to PCB size and shape limitations), the layout design rules described in the following sections are recommended.

2.1 Matching Network for the SiXG301 Wireless MCU

This section provides matching networks recommended for use with SiXG301. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.2 Additional Layout Design Guidelines for the SiXG301 Matching Network.
The SiXG301 wireless MCU comes in a single package and can provide maximum +10 dBm power. All SiXG301 reference designs use a 4-element parallel-C series-L ladder structured matching network, which is optimal for both the +10 dBm and the +0 dBm PA of the SoC. The antenna and radio interface schematic for the +10/+0 dBm BRD4408A Radio Board is shown in the following figure.

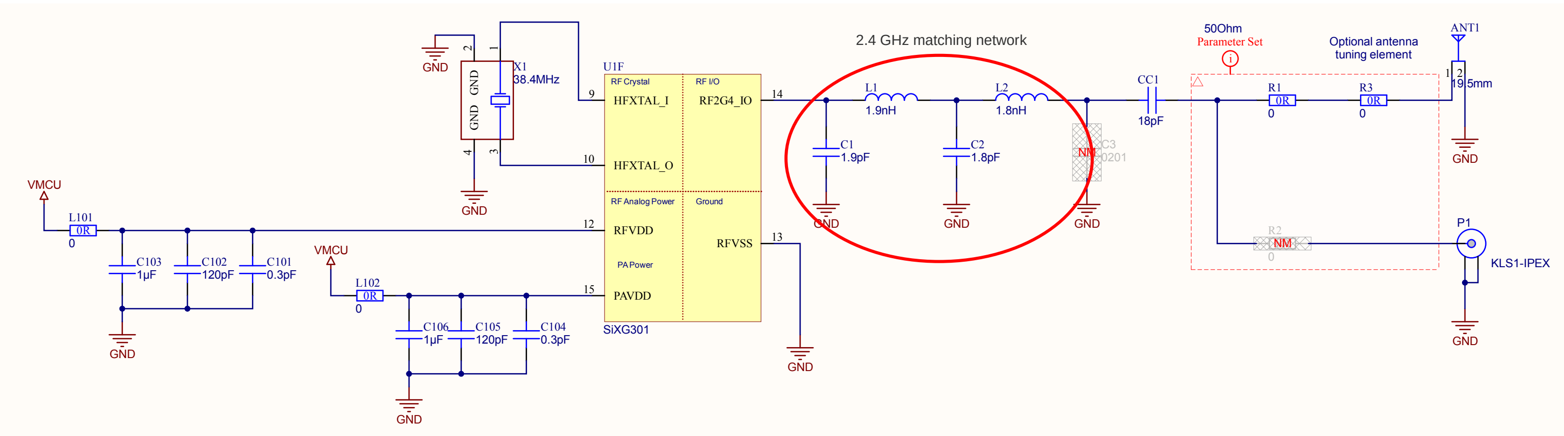

Figure 2.2. RF Section Schematic for the +10/+0 dBm BRD4408A Radio Board (Matching Network is Highlighted)

All Radio Boards for SiXG301 comprise a 50 Ω IFA (Inverted-F Antenna) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these Radio Boards through an u.FL. connector.

In the figure above, there is an additional component (R3) close to the antenna, which is basically not part of the matching network. For a custom design, it is recommended to leave option for this series element for additional harmonic suppression, and its default value should be 0 Ω.The IFA PCB antenna on these Radio Boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, it is recommended to leave option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

3. Guidelines for Layout Design When Using Series 3 Wireless MCUs

3.1 General Layout Design Guidelines for Series 3 Wireless MCUs

Some general guidelines for designing RF-related layouts for good RF performance are as follows:

- For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design, because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required.
- Avoid the separation of the ground plane metallization. It is recommended to create a unified ground plane on the PCB as much as possible which is not separated by traces. Also, the ground path between the matching network and the Series 3 IC exposed pad ground should be clear and unhindered on at least one of the PCB layers. The only exceptions for ground plane separation are the Series 3 matching network and HFXO areas, where the ground pins should NOT be connected to the Top layer ground. More details on these exceptions are provided in 3.1 General Layout Design Guidelines for Series 3 Wireless MCUs.
- Use as many grounding vias (especially near the GND pins) as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.
- Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10^{th} harmonic (the typical distance between vias on reference radio boards is 40–50 mil). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
- For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers.
- Avoid using long and/or thin transmission lines to connect the RF related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.
- Use tapered line between transmission lines with different width (i.e., different impedance) to reduce internal reflections.
- Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.
- Always ensure good VDD filtering by using some bypass capacitors (especially at the range of the operating frequency). The series self-resonance of the capacitor should be close to the filtered frequency. The bypass capacitor which filters the highest frequency should be placed closest to the VDD pins of the Series 3. In addition to the fundamental frequency, the crystal/clock frequency and its harmonics (up to the 3^{rd}) should be filtered to avoid up-converted spurs.
- Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may be an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace.
- Place the RF-related parts (especially the antenna) far away from the dc-dc converter output and the related dc-dc components.
- Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slewn rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.
- Use as short VDD traces as possible. The VDD trace can be a hidden, unwanted radiator so it is important to simplify the VDD routing as much as possible and use large, continuous GND pours with many stitching vias. To achieve the simplified VDD routing, try to avoid star topology of VDD traces (i.e., avoid connecting all VDD traces in one common point).
- Using silkscreen near the antenna could slightly affect the dielectric environment of the antenna. Although this effect is usually negligible, if possible, try to avoid using silkscreen on the antenna or on the antenna copper pour keep out areas.
- Always verify the customer PCB stack-up with the Silicon Labs stack-up (for that SoC) for the proposed matching network values to be applicable. Silicon Labs might use different stack-ups for different SoCs for easier manufacturability (QFN vs WLCSP).

3.2 Layout for the Series 3 Wireless MCUs

Examples shown in this section are based on the layout of the following designs.

- **BRD4408A (SiXG301)**

  The common layout design concepts are shown with the BRD4408A Radio Board layout to demonstrate the basic principles. Later on, separate sections will provide additional layout design guidelines to the matching network of the specific Series 3 families. The layout structure for the RF part of the previously listed designs are shown in the figures below.

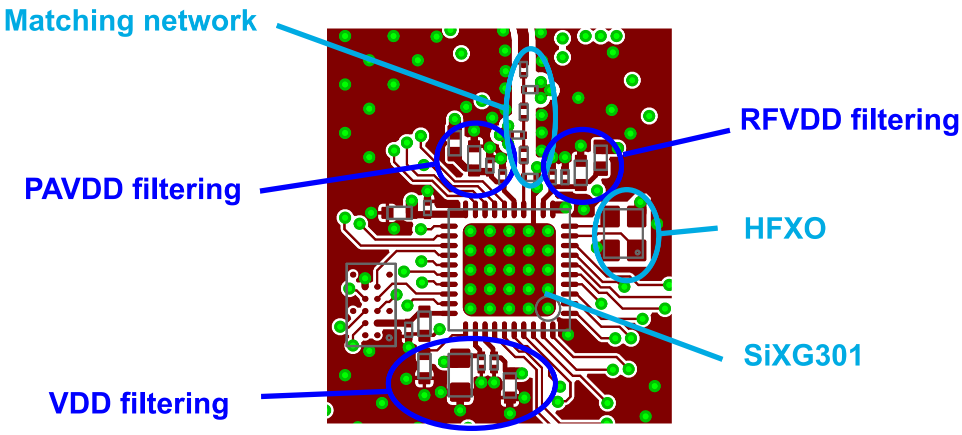

Figure 3.1. Layout of the RF Section for the BRD4408A Radio Board (Top Layer)

3.2.1 Layout Design Guidelines for Series 3 Wireless MCUs

- The lower-value VDD bypass capacitors (the ones with ~pF values) should be kept as close as possible to the VDD pins (RFVDD, PAVDD, AVDD, DVDD, IOVDD).
- To ensure good ground connection, all VDD filtering capacitors should use vias close to their ground pins. It is also recommended that the GND return path between the GND vias of the VDD filtering capacitors and the GND vias of the RFIC paddle should not be blocked in any way; return currents should have a clear and unhindered pathway through the GND plane to the back of the RFIC.
- The exposed pad footprint for the paddle of the Series 3 IC should use as many vias as possible to ensure good grounding and heat sink capability.
- The RF crystal should be placed as close as possible to the HFXTAL_I and HFXTAL_O pins of the Series 3 IC to minimize wire parasitic capacitances and any frequency offsets.
- The ground pins of RF crystal should be connected directly to the first inner layer ground plane using ground vias. Connecting the ground pins to the common ground metal on the Top Layer should be avoided.
- The series matching/filtering inductors should be placed one after another or perpendicular to each other to reduce coupling between stages.
- Traces near the GND pins of the capacitors should be thickened to improve the grounding effect in the thermal straps. This minimizes series parasitic inductances between the ground pour and the GND pins. The figure below demonstrates the above listed layout design recommendations on the BRD4408A Radio Board.

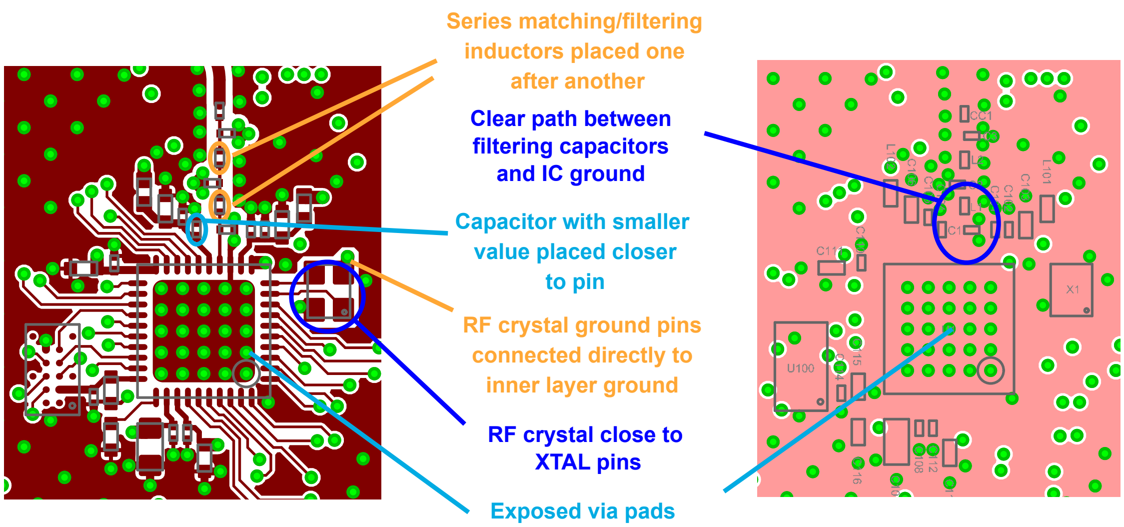

Figure 3.2. VDD Filtering, RF Crystal and Exposed Pad Ground Layout Guidelines on BRD4408A (Top Layer, Inner Layer 1)

- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering. Gaps should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to the restrictions of the actual radio board design. These restrictions include traces routed on other layers or components on the bottom side, which are not shown in the figure above.
- The area beneath the RF chip and the matching network (on the first inner layer) should be filled with continuous ground metal as it will show good ground reference for the matching network and will ensure a good, low impedance return path to the RF chip's ground as well. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX/RX matching network and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear, unhindered pathway through the GND plane to the back of the RFIC.

- Use an isolating ground metal between the crystal and RFVDD traces to avoid any detuning effects on the crystal caused by the nearby power supply and to avoid the leakage of the crystal/clk signal and its harmonics to the supply lines.

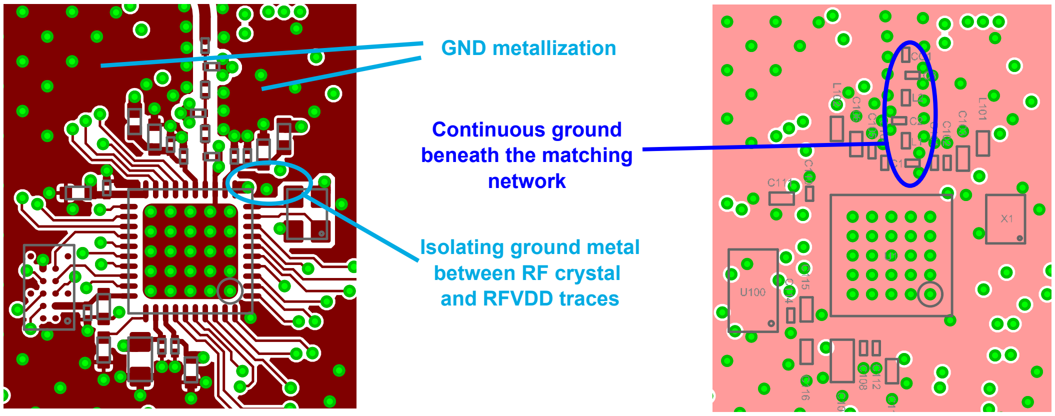

Figure 3.3. Ground Connection Layout Guidelines on BRD4408A (Top Layer, Inner Layer 1)

- Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VDD trace, to reduce their harmonic radiation caused by the fringing field.

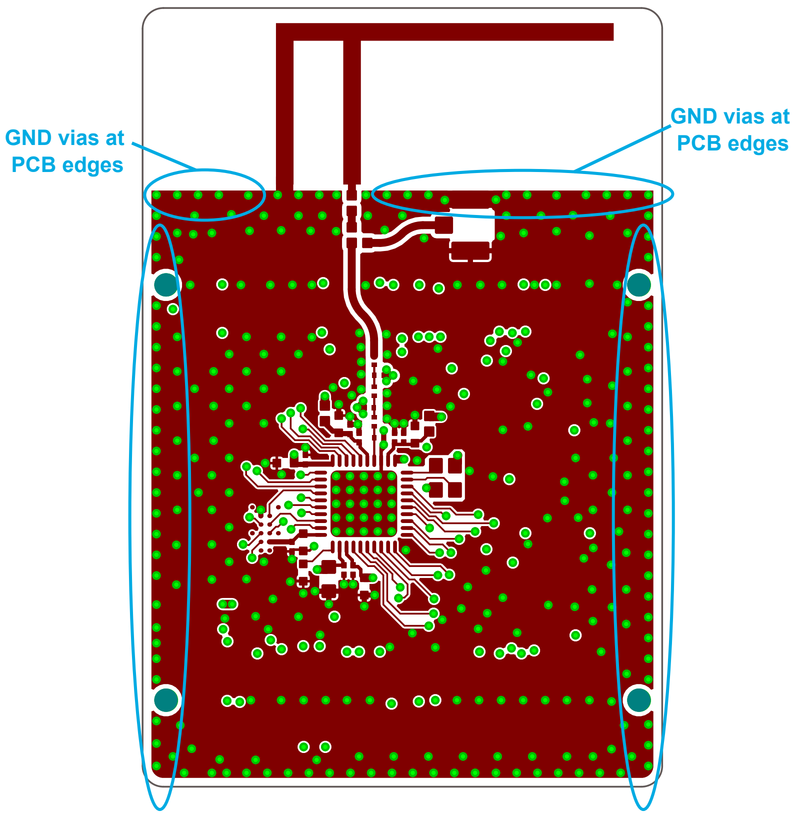

Figure 3.4. GND Vias at PCB Edges on BRD4408A Radio Board (Top Layer)

- If necessary, a shielding can be used to shield the harmonic radiation of the PCB; in that case, the shielding can should cover all of the RF-related components (excluding the antenna).

- The ideal layer consistency for PCBs with more than two layers is as follows:
  - *Top layer:* Use as much continuous solid GND metallization as possible with many vias.
  - *First inner layer:* Use continuous, unified GND metallization beneath the RF part; wires can be routed beneath the non- RF parts if necessary.
  - *All other inner layers:* Route as many (supply and digital) traces on these layers as possible.
  - *Bottom layer:* This layer should be unified GND metal; route traces on this layer only if necessary.

  The following figure illustrates layer consistency on the layout of BRD4408A Radio Board.

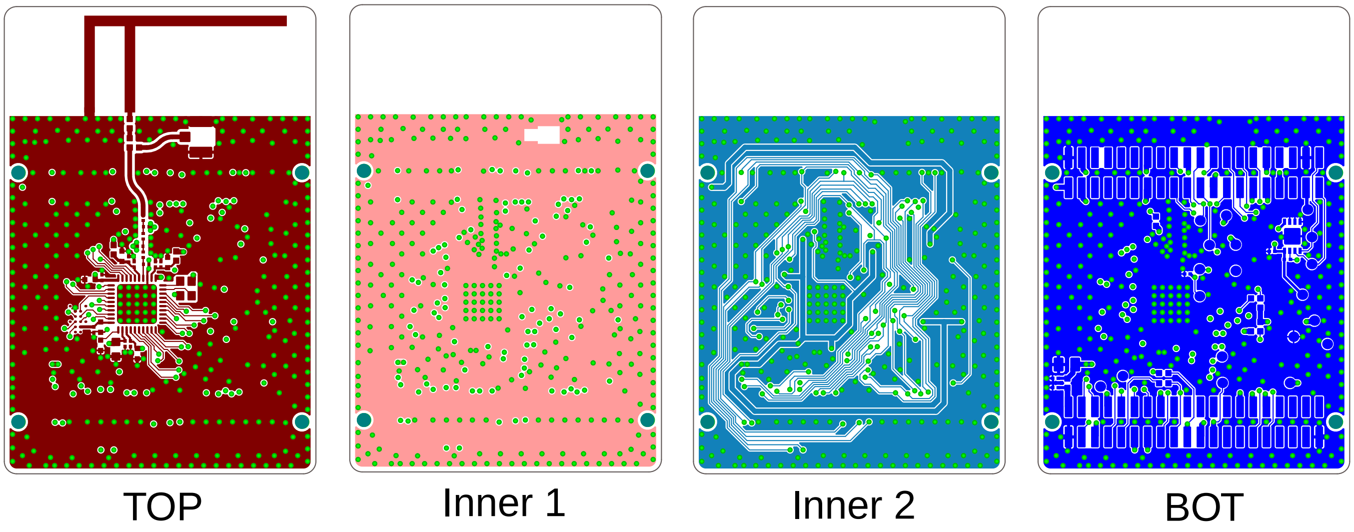

Figure 3.5. Layer Consistency on BRD4408A Radio Board

- Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.
- Avoid placing the supply lines close to the PCB edge.
- To reduce sensitivity to PCB thickness variations, use 50 Ω grounded coplanar lines where possible for connecting the antenna or the u.FL connector to the matching network. This also reduces radiation and coupling effects. A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency.
- The interconnections between elements are not considered transmission lines since their lengths are much shorter than the wavelength, and, thus, their impedances are not critical. As a result, their recommended width is equal to the width of the pad of the applied components. In this way, reflections at pad-trace transitions can be prevented, and parasitic capacitances to ground can be minimized. Examples for the trace dimensions are shown in the table below.
- Use many vias near the coplanar lines in order to minimize radiation.

The following figure demonstrates the 50 Ω grounded coplanar lines on the layout of the BRD4408A Radio Board.

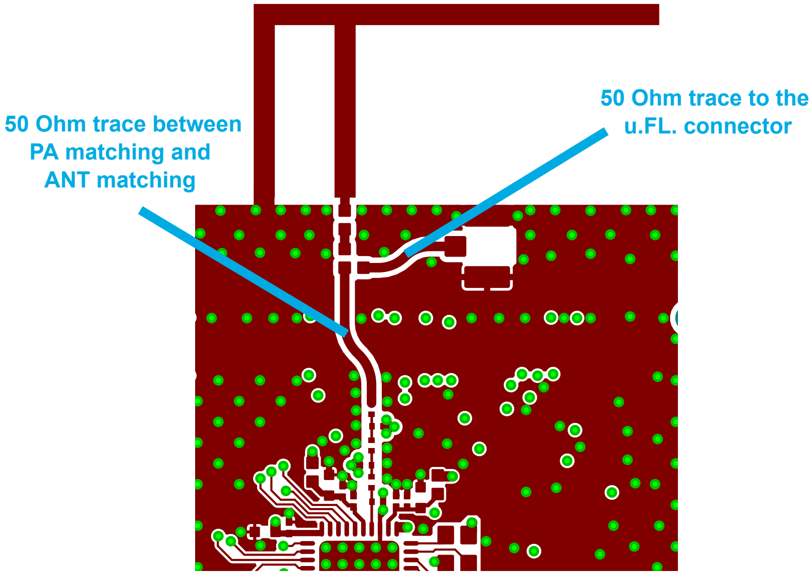

Figure 3.6. 50 Ω Grounded Coplanar Lines on BRD4408A Radio Board (Top Layer)

Table 3.1. Parameters for 50 Ω Grounded Coplanar Lines

Lines	Parameters
f	2.4 GHz
T	0.018-0.035 mm
Dk	4.6
H	0.3 mm
G	0.25 mm
W	0.45 mm

Note:

- For PCBs with more than 2 layers, 'H' is the distance between the top and the first inner layer. For 2-layer PCBs, 'H' is the distance between the top and the bottom layer.
- The example in the table above is based on the parameters for the 4-layer BRD4408A Radio Board. Other radio boards may have a different PCB layer stack-up. Refer to the PCB specification file for the particular radio board PCB stack-up details.
- A 2-layer PCB requires different parameters for a 50 Ω transmission line than shown in this table due to the different value of "H".
- Characteristic impedance is not particularly “sensitive” to the gap value. It should be between 0.25 and 0.4 mm to have 47 to 53 Ω impedance.
- Different impedance calculators may yield slightly different results.

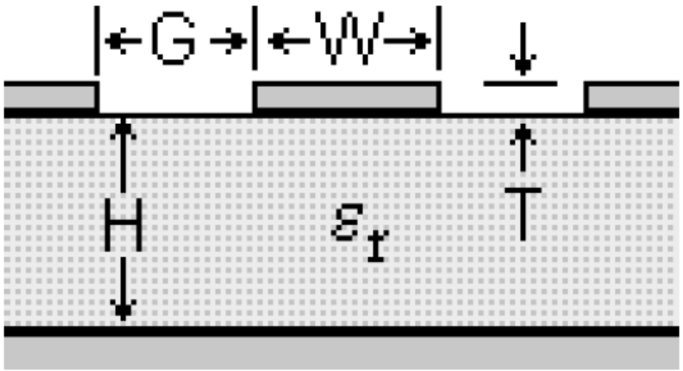

Figure 3.7. Grounded Coplanar Line Parameters

3.2.2 Additional Layout Design Guidelines for the SiXG301 Matching Network

As discussed in 2.1 Matching Network for the SiXG301 Wireless MCU, the SiXG301 matching network is equally optimized for the 0 dBm and +10 dBm high-power PA.

- It is strongly recommended to keep a close distance between the C1 capacitor and the RF2G4_IO TX/RX pin of the SiXG301 IC.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components. The reference design uses 5 mil (0.127mm) wide interconnection traces which have high impedance (~90 Ω), but due to their short length, wide, lower impedance traces could also be used with no detuning effects.
- Connect the nearby shunt capacitors in the matching network to the opposite side of the transmission line for SiXG301 device.
- Connect the 1st shunt capacitor directly to Inner layer ground with multiple vias, and also to the exposed GND pad under the IC. All other capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pins of the rest of the capacitors to the common ground metal on the Top Layer should also be avoided in order to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect RFVSS directly to the exposed pad ground and not to connect it to the common top layer ground.
- Route the PAVDD trace as closeto the RF trace as possible. Consequently, the PAVDD filtering network should also be close to both the RF trace and the PAVDD pin, and it should comprise of three shunt capacitors (0.3 pF + 120pF + 1uF) and a series ferrite.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 39 mils.

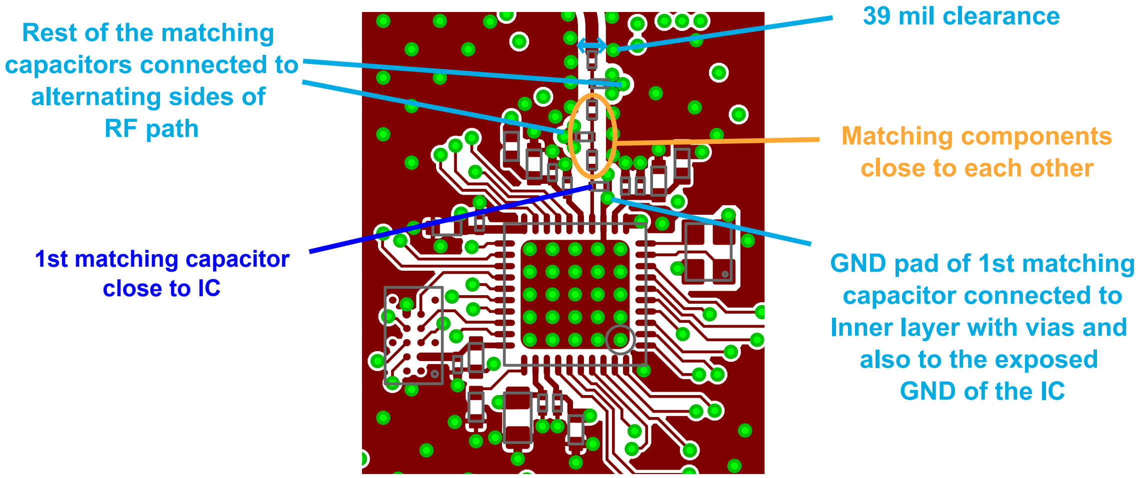

Figure 3.8. Matching Network Layout Guidelines on BRD4408A Radio Board (Top Layer)

4. Revision History

Revision 0.1

September, 2025

- Initial release including SiXG301 recommendations

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