AN928.2: EFR32 Series 2 Layout Design Guide

The purpose of this application note is to help users design PCBs for the EFR32 Series 2 Wireless Gecko Portfolio using design practices that allow for good RF performance.

The matching principles for the 2.4 GHz EFR32 Series 2 wireless MCUs are described in the application note, AN930.2: EFR32 Series 2 2.4 GHz Matching Guide, while the matching process for the sub-GHz EFR32 Series 2 devices are discussed in AN923.2: EFR32 Series 2 sub-GHz Matching Guide. The MCU-related subjects are detailed in the following application notes: AN0918.2: Series 1 to Wireless Gecko Series 2 Compatibility and Migration Guide, AN0948.2: EFR32 Series 2 Power Configurations and DC-DC, and AN0955: CRYPTO.

The Silicon Labs MCU and Wireless Starter Kits and Simplicity Studio provide a powerful development and debug environment. To take advantage of the capabilities and features on custom hardware, Silicon Labs recommends including debugging and programming interface connector(s) in custom hardware designs. The details and benefits of including these connector interfaces are detailed in AN958: Debugging and Programming Interfaces for Custom Designs.

The power supply configurations of EFR32 Series 2 are described in AN0002.2: EFR32 Wireless Gecko Series 2 Hardware Design Considerations. The RF performance strongly depends on the PCB layout, as well as the design of the matching networks. For optimal performance, Silicon Labs recommends using the PCB layout design guidelines described in the following sections.

KEY POINTS

- Provides a reference schematic and PCB layout
- Lists and describes all main design principles
- Provides a summary checklist of all design principles

1. Device Compatibility

This application note supports the following devices:

EFR32 Gecko Series 2:

- EFR32MG21, EFR32MG22, EFR32MG24, EFR32MG26, EFR32MG27
- EFR32BG21, EFR32BG22, EFR32BG24, EFR32BG27
- EFR32FG22, EFR32FG23, EFR32FG25, EFR32FG28
- EFR32ZG23, EFR32ZG28

Note: The part number EFR32xG21 includes EFR32xG21-B and EFR32xG21-C, which are different revisions of the SoC.

2. Design Recommendations When Using EFR32 Series 2 Wireless MCUs

Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended that designers use the reference designs as-is since they minimize detuning effects caused by parasitics or generated by poor component placement and PCB routing. EFR32 reference design files are available in Simplicity Studio under the Kit Documentation tab.

The compact RF part of the designs (excluding the 50 Ω single-ended antenna) is highlighted by a blue frame, and it is strongly recommended to use the same framed RF layout in order to avoid any possibility of detuning effects. The figure below shows the framed compact RF part of the designs.

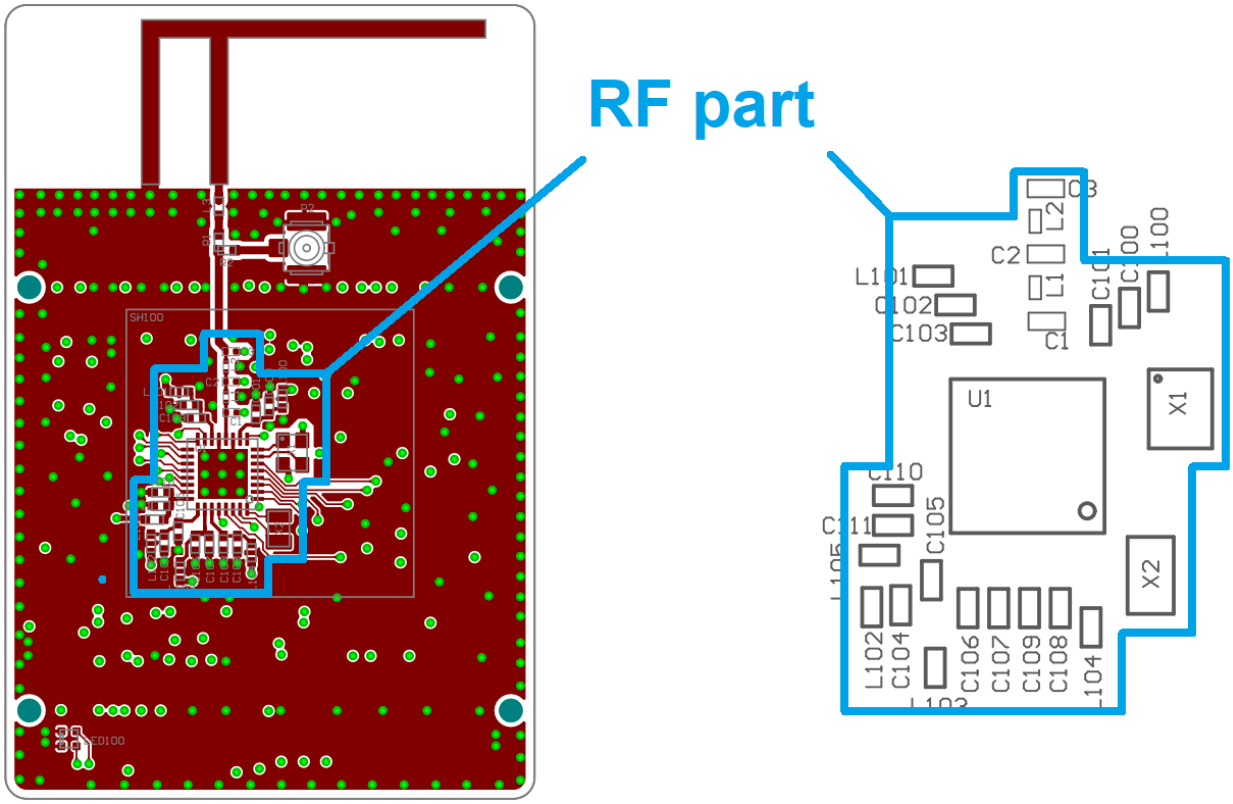


Figure 2.1. Top Layer of the BRD4180A (EFR32xG21) Radio Board (Left Side) and Assembly Drawing of the RF Part (Right Side)

The layout of the MCU VDD filtering capacitors should also be copied from the reference design as much as possible. When layouts cannot be followed as shown by the reference designs (due to PCB size and shape limitations), the layout design rules described in the following sections are recommended.

2.1 Matching Network Types for the EFR32xG21 Wireless MCU

This section provides matching networks recommended for use with EFR32xG21. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.2 Additional Layout Design Guidelines for the EFR32xG21 Matching Networks.

The part number EFR32xG21 includes EFR32xG21-B and EFR32xG21-C, which are different revisions of the SoC.

The EFR32xG21 wireless MCU can provide maximum +20 dBm power. All EFR32xG21 reference designs use a parallel-C series-L ladder structured matching network. For low power applications (≤10 dBm) a 3-element C-L-C network is sufficient, while high power solutions (>10 dBm) require a 5-element match. For 0 dBm output power the recommended matching network is shown in Figure 2.4 Recommended Matching Network for EFR32xG21 for 0 dBm Output Power on page 5.

The antenna and radio interface schematic for the 10 dBm BRD4181A Radio Board is shown in the figure below.

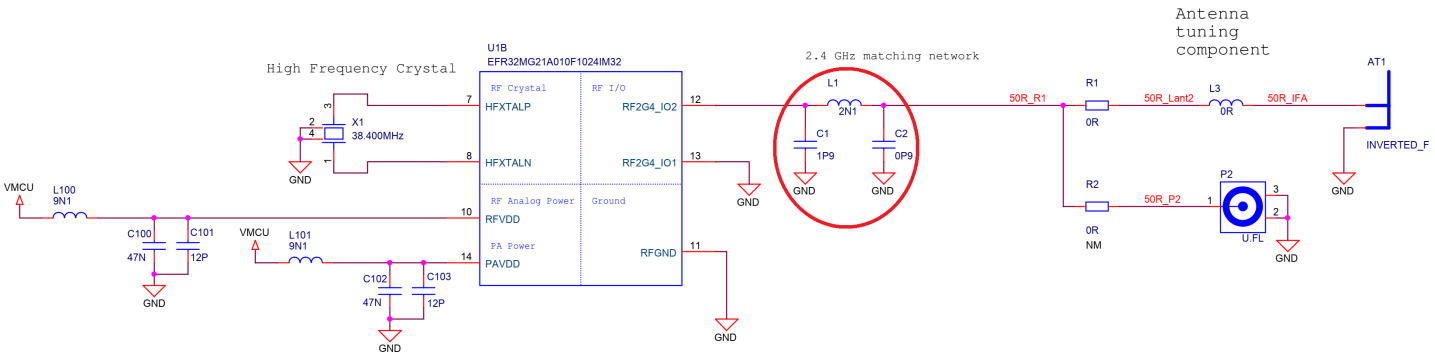


Figure 2.2. RF Section Schematic for the 10 dBm BRD4181A Radio Board (Matching Network is Highlighted)

The antenna and radio interface schematic for the 20 dBm BRD4180A Radio Board is shown in the figure below.

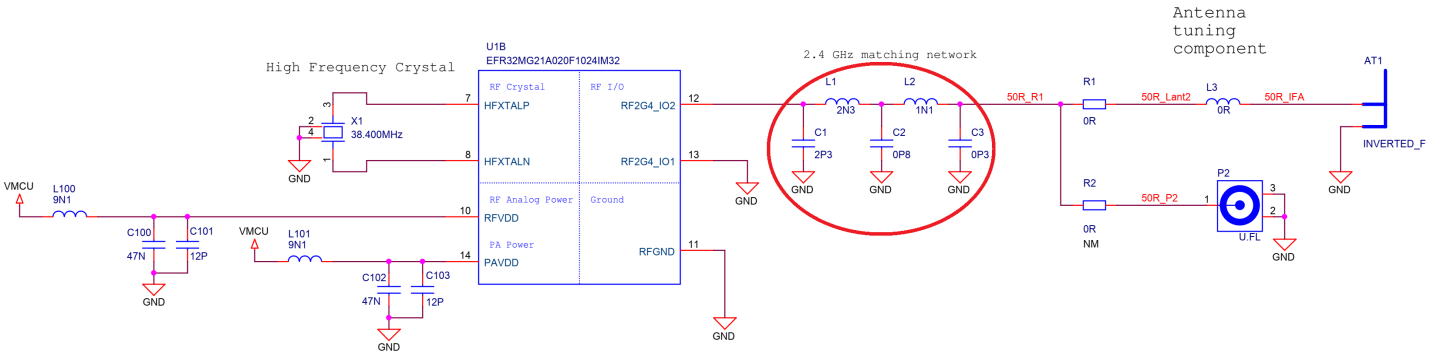


Figure 2.3. RF Section Schematic for the 20 dBm BRD4180A Radio Board (Matching Network is Highlighted)

It is not surprising that the increased TX output power of the EFR32 devices is accompanied by a corresponding increase in the absolute level of harmonic signals. Since most regulatory standards (e.g., FCC, ETSI, ARIB etc.) require the harmonic signals to be attenuated below some absolute power level (in watts or dBm), the amount of low-pass filtering required is generally greater on an RF Radio Board using an EFR32 that was designed for higher output power.

All Radio Boards for EFR32xG21 comprise a 50 Ω IFA (Inverted-F Antenna) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these Radio Boards through an U.FL connector.

In the figure above, there is an additional component (L3) close to the antenna, which is basically not part of the matching network. For a custom design, it is recommended to leave option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

The IFA PCB antenna on these Radio Boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, it is recommended to leave option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

Note: If both RF pins (RF2G4_IO1 and RF2G4_IO2) are used, the matches can couple and detune each other, so the ideal match is for only one populated.

The recommended matching network for 0 dBm output power for EFR32xG21 is shown below:

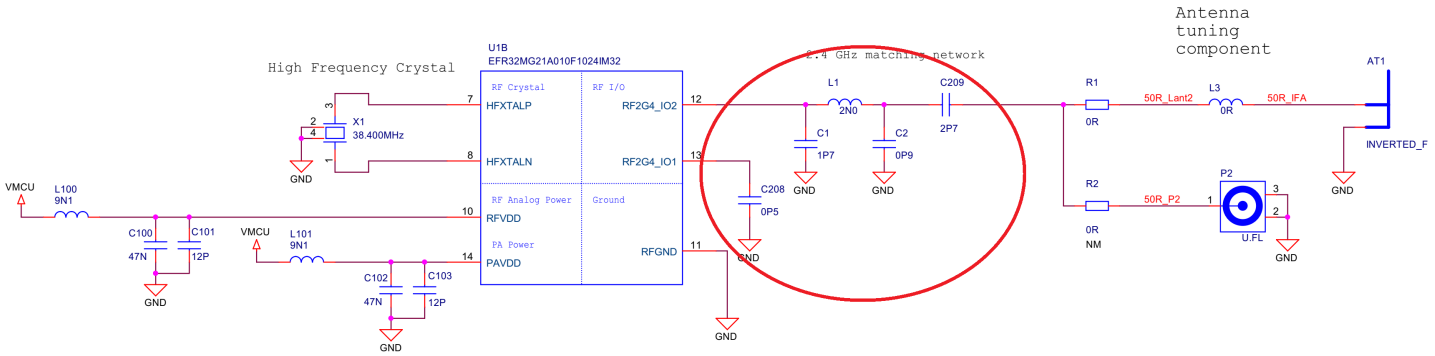


Figure 2.4. Recommended Matching Network for EFR32xG21 for 0 dBm Output Power

Note: the 0 dBm matching network requires 2 additional capacitors as well as component value changes compared to the 10 dBm matching network. The current Radio Boards (BRD4180A, BRD4181A) do not have an option for the 0.5 pF capacitor at the RF2G4_IO1 pin. Therefore, the 0 dBm PA cannot be used on these devices. To use the 0 dBm PA, PCB layout change is necessary.

If using the 0 dBm and the 10 dBm PA with the same BOM, the matching network recommendation is as follows:

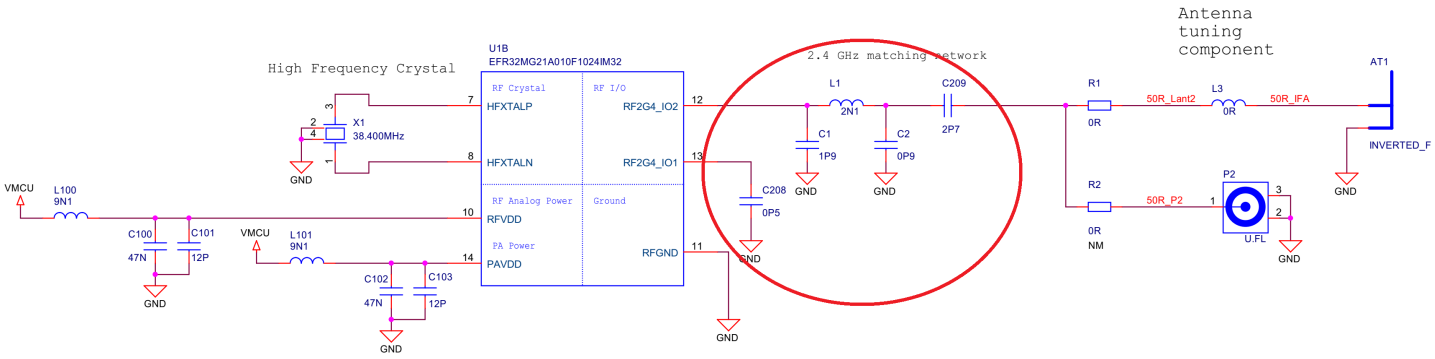


Figure 2.5. Recommended Matching Network for EFR32xG21 for 0 / 10 dBm Output Power

Note: The placement and connection of C208 has slight effect on radiated harmonic performance in case of the 10 dBm power setting. For recommendations on how to connect this component on the PCB layout, refer to 3.2.2 Additional Layout Design Guidelines for the EFR32xG21 Matching Networks.

Further details on the EFR32xG21 matching network principles can be found in the application note, AN930.2: EFR32 Series 2 2.4GHz Matching.

2.2 Matching Network Types for the EFR32xG22 Wireless MCU

This section provides matching networks recommended for use with EFR32xG22 with different layout approaches. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.3 Additional Layout Design Guidelines for the EFR32xG22 Matching Networks.

There are two different layout and matching concepts designed for EFR32xG22, as follows:

Layout concepts:

1. Existing concept: This layout approach utilizes a short GND trace connection between the first shunt matching capacitor and RFVSS ground pin of the chip, and that capacitor is not connected to any via or component-layer GND pour (except for the chip exposed pad through RFVSS). The second shunt matching capacitor is grounded through a single via to an inner layer's GND plane. Also, there is about 70 mils of total copper keep-out on the component-layer GND pour around the RF matching circuit.
2. Generic concept: This layout concept follows more generic RF layout guidelines and no special or unique approach is applied. The shunt matching capacitors are connected to the component-layer GND pour with multiple stitching vias and there is about 37 mils of total copper keep-out on the component-layer GND pour around the RF matching circuit.

Matching concepts:

1. Pi-matching concept: This matching concept utilizes three SMD components in a Pi-structure with two shunt capacitors and one series inductor between the two capacitors. Historically, this type of matching concept was initially designed for the EFR32xG22 parts and radio boards are available with this Pi-matching configuration (on the existing layout concept). This Pi-matching network on the generic layout concept provides good radiated harmonic margins on PCB stack-up configurations when the gap between the top and first inner GND layer is small, i.e., < 150 µm.
2. T-matching concept: This matching concept utilizes three SMD components in a T-structure with two series inductors and one shunt capacitor between the two inductors. This is the most recent matching network designed for the EFR32xG22 parts. Because the first component in the match from the chip is a series inductor, the match provides a high impedance load at the harmonics, and thus good harmonic suppression is achieved. However, there is no issue with the GND coupling between matching elements since there is only one shunt capacitor in the match. It is recommended to connect this single shunt capacitor in the match to the PAVDD side of the GND plane on the top layer. T-match is less sensitive to the layout variants, but tested when following the generic layout concept on PCB stack-up configurations when the gap between the top and first inner GND layer is equal with or smaller than 0.8 mm. The best radiated harmonic margin was achieved when utilizing the T-match on Silicon Labs 2- and 4-layer reference boards.

EFR32xG22 data sheet provides a suggested matching network with the layout concept number one above. All data sheet parameters are captured with this configuration. This solution provides excellent conducted RF performance but the radiated 5th harmonic can be marginal in FCC certifications. To ensure margins on the radiated 5th harmonic, it is especially important to place the first shunt matching capacitor very close to the chip pins and follow the reference radio board's PCB stack-up. Also, Silicon Labs reference radio boards are available with the existing layout concept.

However, Silicon Labs recommends to follow the generic layout concept number two above. This solution is more robust and does have bigger margins on the radiated harmonics. The RF performance when following this layout approach is not that sensitive to the PCB stack-up, component spreading and layout parasitics as the existing layout concept is. Additionally, the T-match appears to have better harmonic margins (both conducted and radiated) when using standard PCB stack-up configurations (top and GND layer distance is between 0.15 and 0.8 mm), and also appears to be more robust against different layout concepts.

The EFR32xG22 part is capable of transmitting at the output power level up to +8 dBm. However, higher than +6 dBm TX power output will result in higher current consumption and harmonic levels, and the +8 dBm TXP is not guaranteed over temperature and process variations. Please work with your local Silicon Labs Sales contact to request AN1353-NDA EFR32xG22 8 dBm Use Case Recommendations for more details.

2.2.1 Data Sheet Pi-Matching Network with Existing Layout Concept #1

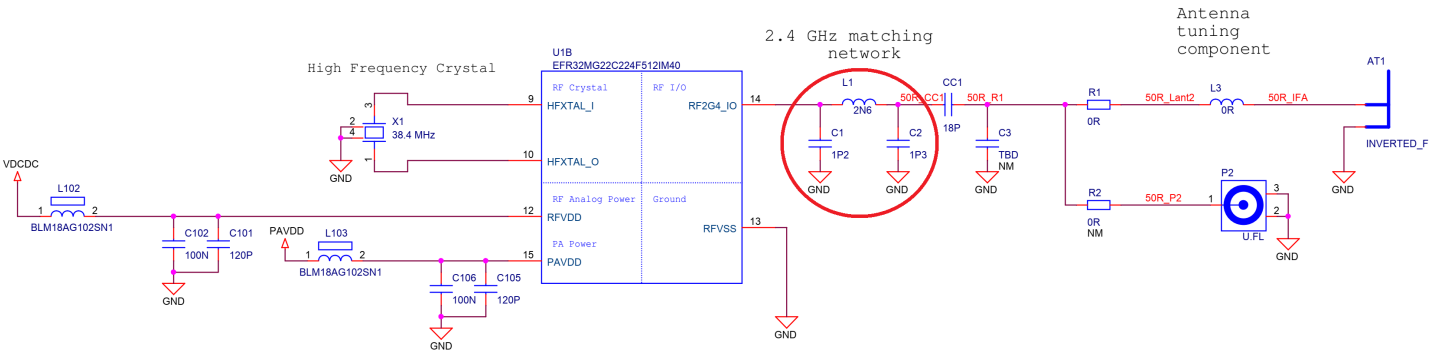


Figure 2.6. Pi-Matching Network Schematic with the Existing Layout Concept #1

Use the matching network shown above with EFR32xG22 for any achievable power level when following the existing layout concept #1 discussed above. The series dc-blocking capacitor (CC1) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm, i.e., simultaneously optimized with the 0 and +6 dBm PA as well.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

All Radio Boards for EFR32xG22 comprise a 50 Ω IFA (Inverted-F Antenna) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these Radio Boards through an U.FL connector.

In the figure above, there is an additional component (L3) close to the antenna, which is basically not part of the matching network. For a custom design, it is recommended to leave option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

The IFA PCB antenna on these Radio Boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, it is recommended to leave option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

2.2.2 Pi-Matching Network with Generic Layout Concept #2

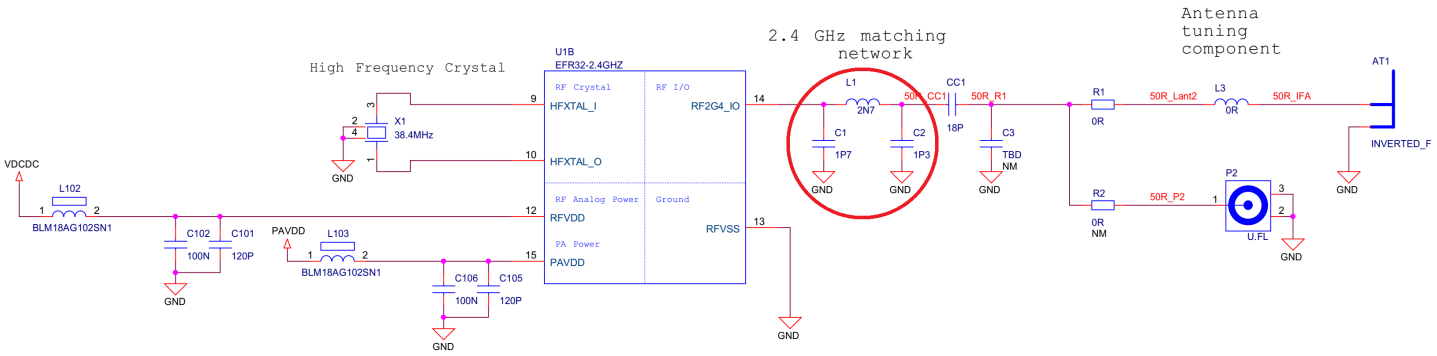


Figure 2.7. Pi-Matching Network Schematic with the Generic Layout Concept #2

Use the matching network shown above with EFR32xG22 for any achievable power level on a 2- or more-layer PCB where the gap between the top and first inner (or bottom - for a 2-layer PCB) layer is maximum 800 µm when following the generic layout concept #2 discussed above. The series dc-blocking capacitor (CC1) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm. The matching network is simultaneously optimized for both the 0 and +6 dBm PA.

The matching network component values are optimized for PCB stack-up configurations with a separation of maximum 800 µm (32mils) between the top and first inner layer (or bottom layer for a 2-layer PCB). Tested with the standard radio board stack-up with a 0.3mm gap between the top and first inner layer, with a 4-layer PCB with 0.07 mm gap between the top and first inner layer, and with a 2-layer 32 mils (0.8 mm) thick PCB.

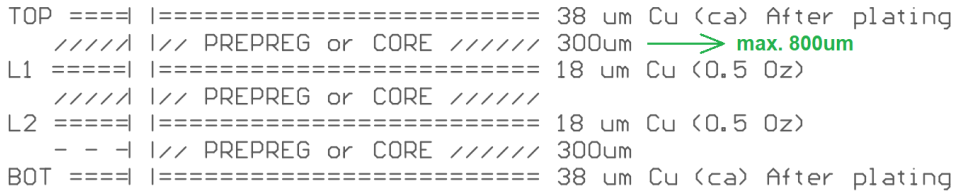


Figure 2.8. Stack-up for the Pi-match with a 4-layer PCB

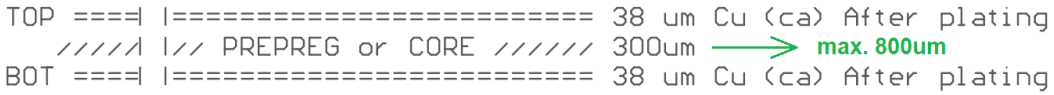


Figure 2.9. Stack-up for the Pi-match with a 2-layer PCB

All Radio Boards for EFR32xG22 comprise a 50 Ω IFA (Inverted-F Antenna) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these Radio Boards through an U.FL connector.

In the figure above, an additional component (L3), close to the antenna, is not part of the matching network. For a custom design, leave option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

The IFA PCB antenna on these Radio Boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, leave option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

2.2.3 T-Matching Network Schematic

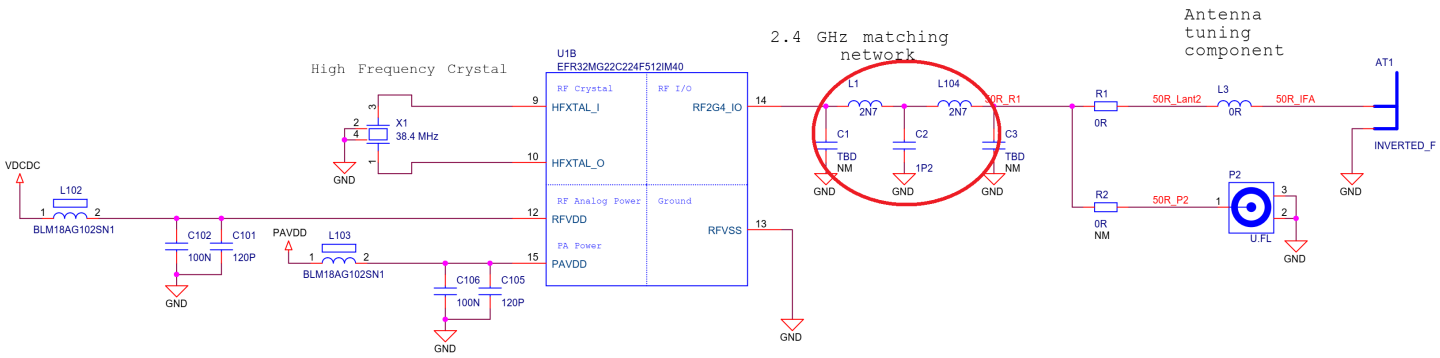


Figure 2.10. T-Matching Network Schematic

Use the matching network shown above with EFR32xG22 for any achievable power level on a 2- or more layer PCB where the gap between the top and first inner layer (or bottom layer for 2-layer PCB) is a maximum of 800 µm while following the generic or existing layout concepts discussed above. (Silicon Labs provides performance data when following the generic layout concept). An additional series dc-blocking capacitor is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm. The matching network is simultaneously optimized for both the 0 and +6 dBm PA.

The matching network component values are optimized for PCB stack-up configurations with a separation maximum of 800 µm (32 mils) between the top and first inner layer (or bottom layer for 2-layer PCB). The matching network is tested with the standard radio board stack-up with a 0.3 mm gap between the top and first inner layer and with a 2-layer 32 mils (0.8 mm) thick PCB.

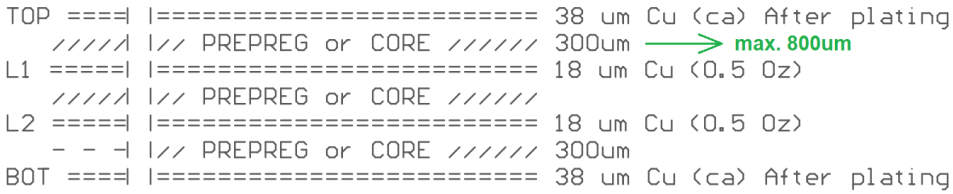


Figure 2.11. Stack-up for the T-match with a 4-layer PCB

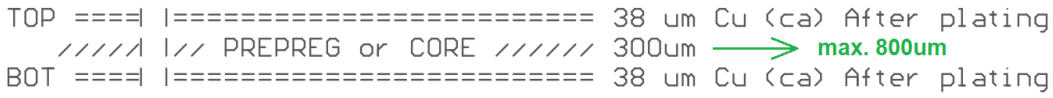


Figure 2.12. Stack-up for the T-match with a 2-layer PCB

All radio boards for EFR32xG22 comprise a 50 Ω Inverted-F Antenna (IFA) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these radio boards through a U.FL connector.

In the figure above, an additional component (L3), close to the antenna, is not part of the matching network. For a custom design, leave the option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

The IFA PCB antenna on these radio boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, leave the option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

2.3 Matching Network Types for the EFR32xG23 Wireless MCU

This section provides matching networks recommended for use with EFR32xG23. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.4 Additional Layout Design Guidelines for the EFR32xG23 Matching Networks.

The typical RF matching circuit for EFR32xG23 is shown below:

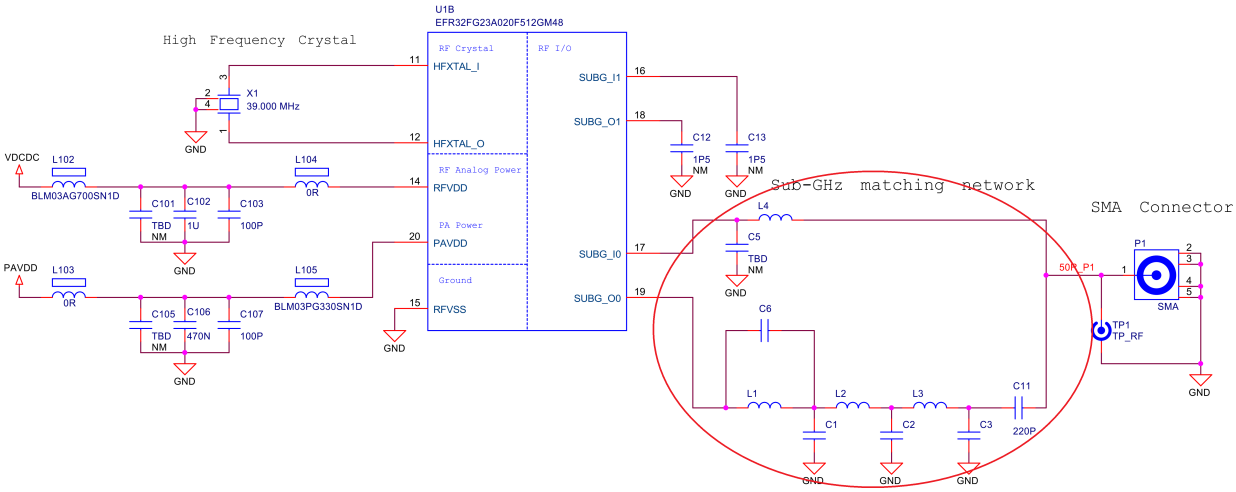


Figure 2.13. Typical RF Matching Circuit for EFR32xG23

Note: Matching network component values should be chosen based on the frequency band and output power target. Matching network structure can be slightly different for different frequency bands/output power targets. For the correct matching network information, refer to AN923.2: EFR32 Series 2 sub-GHz Matching Guide and the EFR32xG23 radio board reference designs.

All radio boards for EFR32xG23 comprise an SMA connector, which can be used for conducted measurements or to connect an external antenna for radiated test purposes.

2.4 Matching Network Types for the EFR32xG24/26 Wireless MCU

This section provides matching networks recommended for use with EFR32xG24 and EFR32xG26, which have similar RF front-end designs. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.5 Additional Layout Design Guidelines for the EFR32xG24/26 Matching Networks.

The EFR32xG24 is available in both QFN (QFN40/QFN48) and WLCSP (WLCSP42) packages, while the EFR3xG26 is available in QFN (QFN48/QFN68) and BGA (BGA136) packages. The recommended matching network for QFN packages is a parallel-C series-L ladder structured matching network, while the WLCSP package requires a T-match (L-C-L).

For the QFN package devices, there are notable differences on the RF front-ends schematic and PCB layout designs of the low-power (≤10 dBm) and high-power (>10 dBm) applications:

- The 10 dBm PA requires a 4 element C-L-C-L matching network, while the 20 dBm PA requires a 5 element C-L-C-L-C matching network (the extra capacitor is necessary for ideal harmonic suppression)
- Different matching network component values
- Different PCB layout around the matching network
- The 10 dBm PA requires a dc-blocking capacitor at the matching network output
- Different PAVDD filtering network is required for low and high power cases

Silicon Labs also provides a 5-element C-L-C-L-C matching network recommendation for high power (>10 dBm) antenna diversity applications for the QFN package types where a dc-blocking capacitor is required at all 3 ports of the external diversity switch.

The recommended matching network for EFR32xG24/26 QFN package types optimized for 10 dBm TX power (based on BRD4186C, BRD4116A, and BRD4120A) is shown in the figure below:

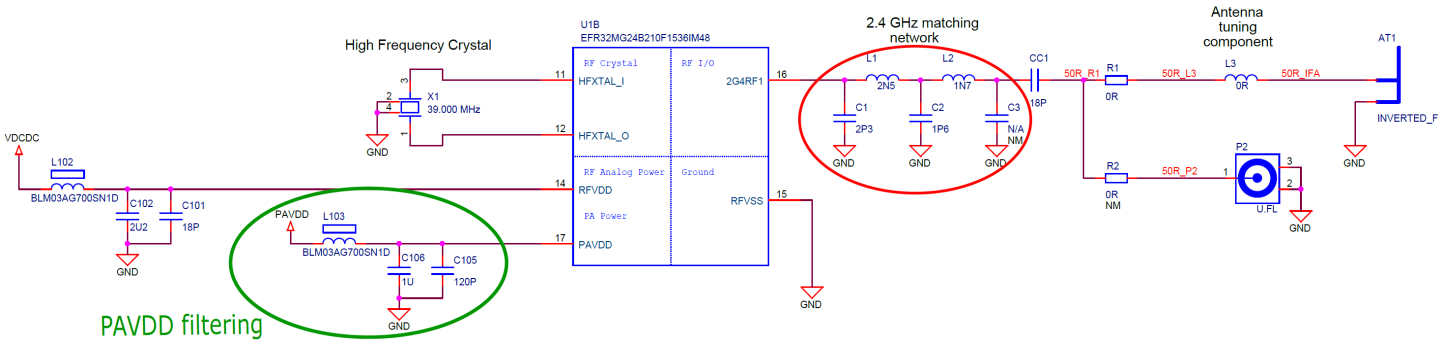


Figure 2.14. 10 dBm Matching Network for the EFR32xG24/26 QFN Package Type (Matching Network and PAVDD Filtering are Highlighted)

The recommended matching network for EFR32xG24/26 QFN package types optimized for 20 dBm TX power (based on BRD4187C, BRD4117A, and BRD4121A) is shown in the figure below:

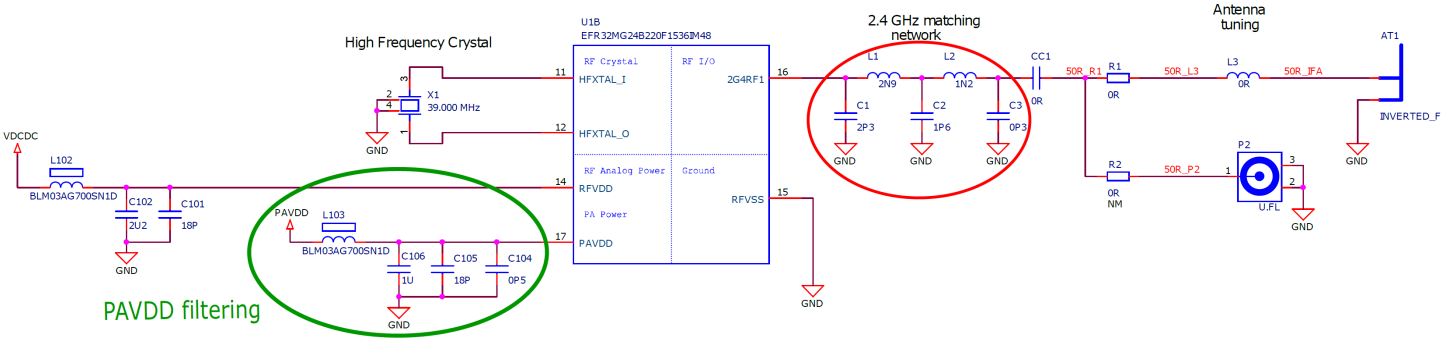


Figure 2.15. 20 dBm Matching Network for the EFR32xG24/26 QFN Package Type (Matching Network and PAVDD Filtering are Highlighted)

The recommended matching network for EFR32xG24 QFN package types optimized for 20 dBm TX power for antenna diversity operation (based on BRD4188C) is shown in the figure below:

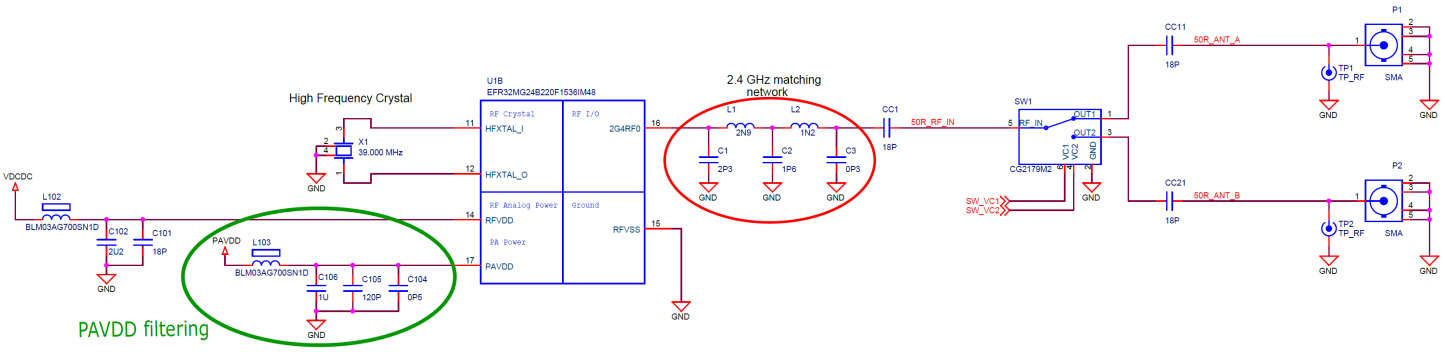


Figure 2.16. 20 dBm Matching Network for the EFR32xG24 QFN Package Type for Antenna Diversity (Matching Network and PAVDD Filtering are Highlighted)

The BRD4188B comprises two SMA connectors, which can be used for conducted measurements or to connect external antennas for radiated test purposes.

The recommended matching network for EFR32xG24 WLCSP package type optimized for 4 dBm TX power (based on BRD4115B) is shown in the figure below:

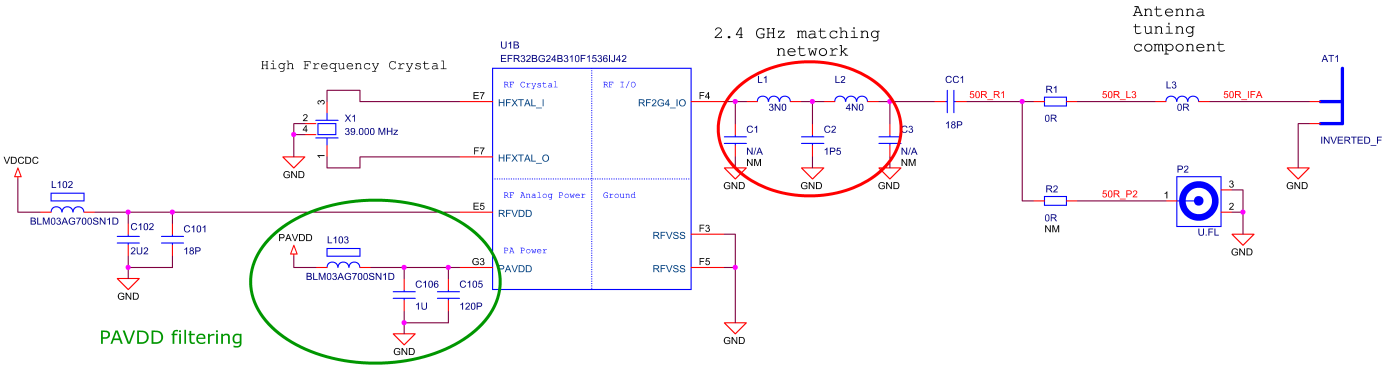


Figure 2.17. 4 dBm Matching Network for the EFR32xG24 WLCSP Package Type (Matching Network and PAVDD Filtering are Highlighted)

The recommended matching network for EFR32xG26 BGA package type optimized for 10 dBm TX power (based on BRD4118A) is shown in the figure below:

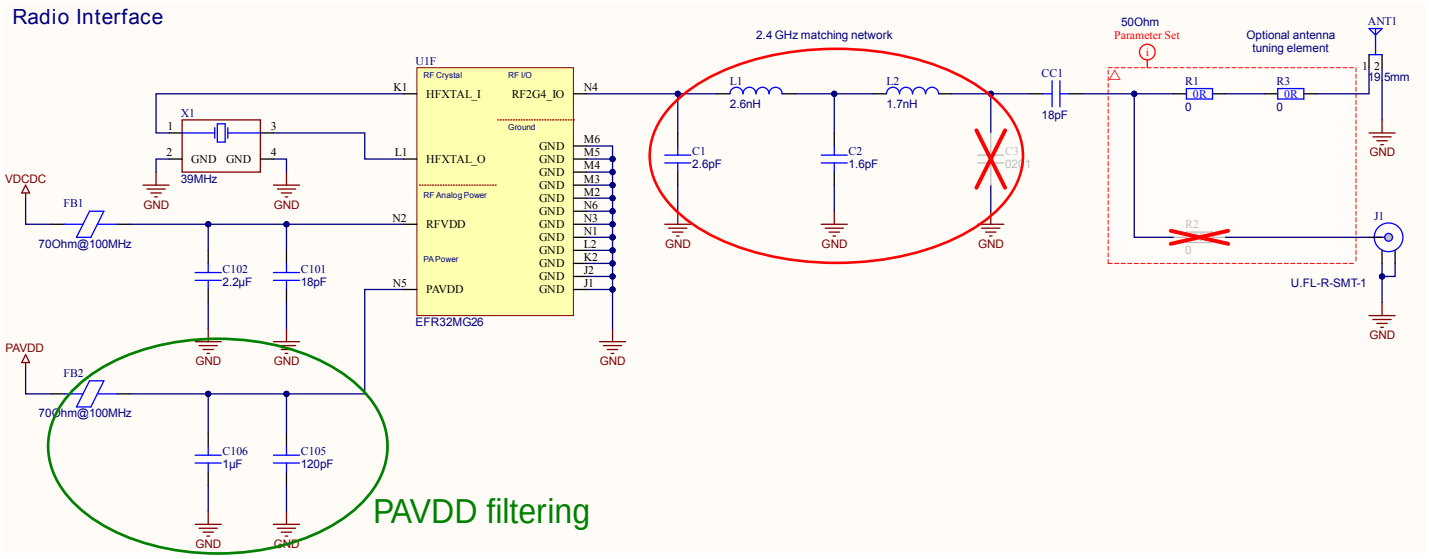


Figure 2.18. 10 dBm Matching Network for the EFR32xG26 BGA Package Type (Matching Network and PAVDD Filtering are Highlighted)

All radio boards comprise a 50 Ω Inverted-F Antenna (IFA) connected to the 50 Ω output of the matching network to be able to measure radiated performance. Optional conducted measurements are possible on these radio boards through a U.FL connector.

In the figure above, an additional component (L3), close to the antenna, is not part of the matching network. For a custom design, leave the option for this series element for additional harmonic suppression. Its default value should be 0 Ω.

The IFA PCB antenna on these radio boards is optimized for 50 Ω impedance without any external discrete antenna matching network. For maximum flexibility, leave the option for a 3-element pi-structure antenna matching network between L3 and the antenna on a custom design.

2.5 Matching Network Types for the EFR32xG25 Wireless MCU

This section provides matching networks recommended for use with EFR32xG25. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in section 3.2.6 Additional Layout Design Guidelines for the EFR32xG25 Matching Networks .

The EFR32xG25 Wireless MCU is comprised of two PAs (FSK and OFDM) that can provide up to 16 dBm power. Regardless of which PA is utilized (only one of them can be selected), the matching network and layout guidelines presented in this application note are similarly applicable.

Silicon Labs recommends two types of matching network structures:

1. With an external ceramic balun: This matching structure consists of an impedance transforming circuit, a differential to single-ended transformer balun, and a low pass filter. Silicon Labs provides reference designs with this structure for the 868, 915, and 920 MHz bands with the same schematic and layout designs.
2. With full discrete match: This matching structure only consists of discrete passive components that provide the function of the impedance and differential to single-ended transformations, as well as the the low pass filtering. Silicon Labs provides a reference design with this structure for the 470 MHz band. The matching networks for the 868, 915, and 920 MHz bands were tested on a prototype radio board that is not an available reference design.

2.5.1 Matching Network Structure with an External Ceramic Balun

The typical RF matching circuit for EFR32xG25 with the use of an external ceramic balun is shown below.

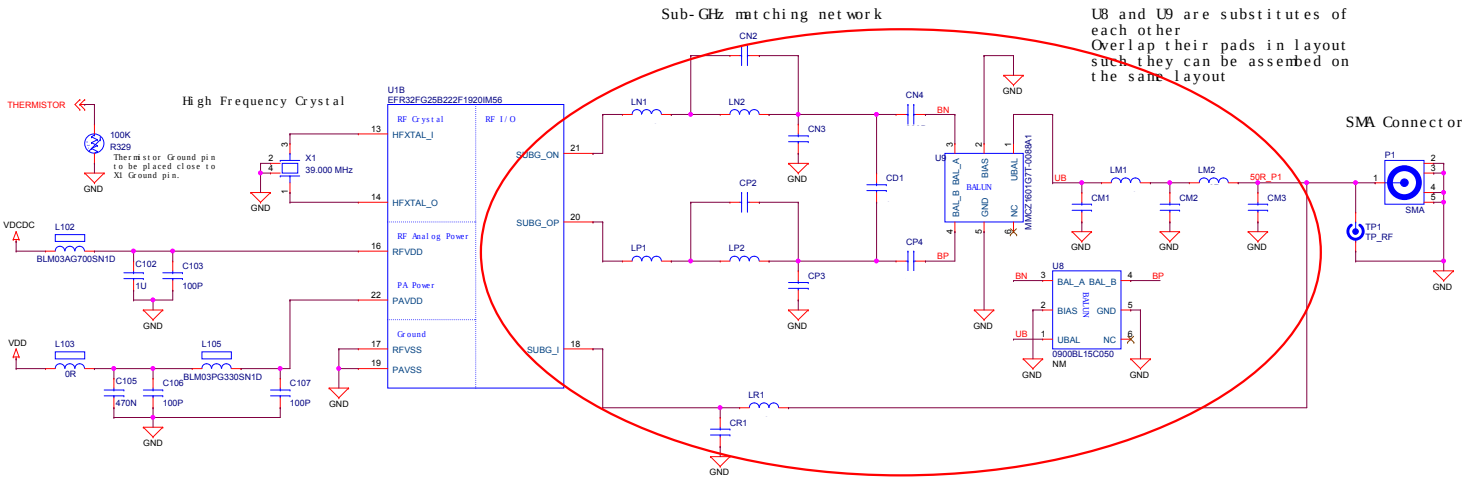


Figure 2.19. RF Section Schematic for the 16 dBm BRD4270B Radio Board (Matching Network is Highlighted)

Note: Matching network component values should be chosen based on the frequency band. However, the matching structures are similar for the 868, 915, and 920 MHz bands. For the correct matching network information, refer to AN923.2: EFR32 Series 2 sub-GHz Matching Guide and the EFR32xG25 radio board reference designs.

All radio boards for EFR32xG25 comprise an SMA connector, which can be used for conducted measurements or to connect an external antenna for radiated test purposes.

2.5.2 Full Discrete Matching Network Structure

The typical full discrete RF matching circuit for EFR32xG25 for the 868, 915, and 920 MHz bands is shown below. This structure can be further simplified to a minimum BOM version with a fewer number of components. For the minimum BOM schematic, refer to AN923.2: EFR32 Series 2 sub-GHz Matching Guide.

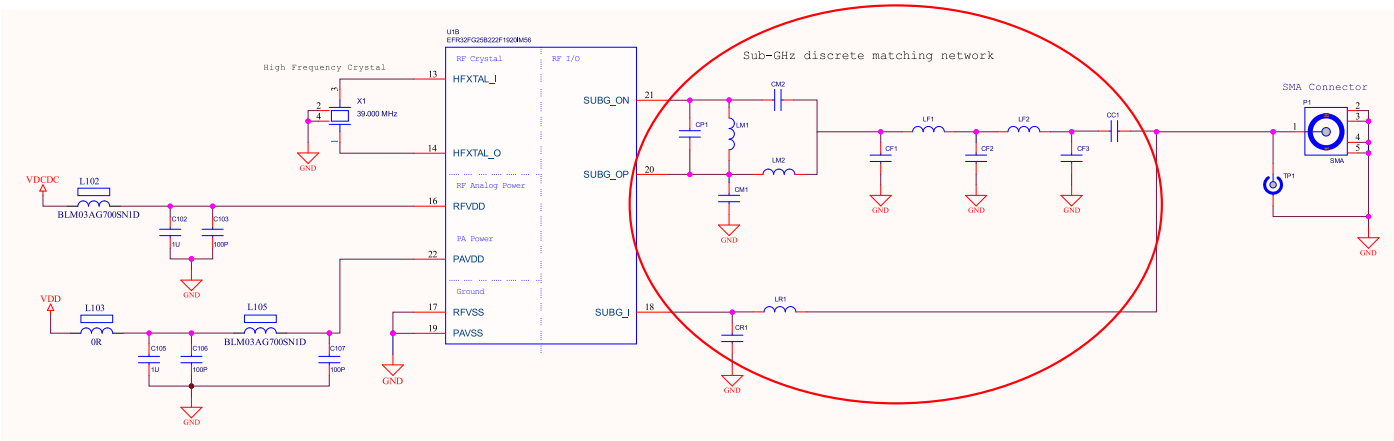


Figure 2.20. RF Section Schematic for the 868, 915, and 920 MHz Band Full Discrete Match Prototype Radio Board (Matching Network is Highlighted)

The typical full discrete RF matching circuit for EFR32xG25 for the 470 MHz band is shown below.

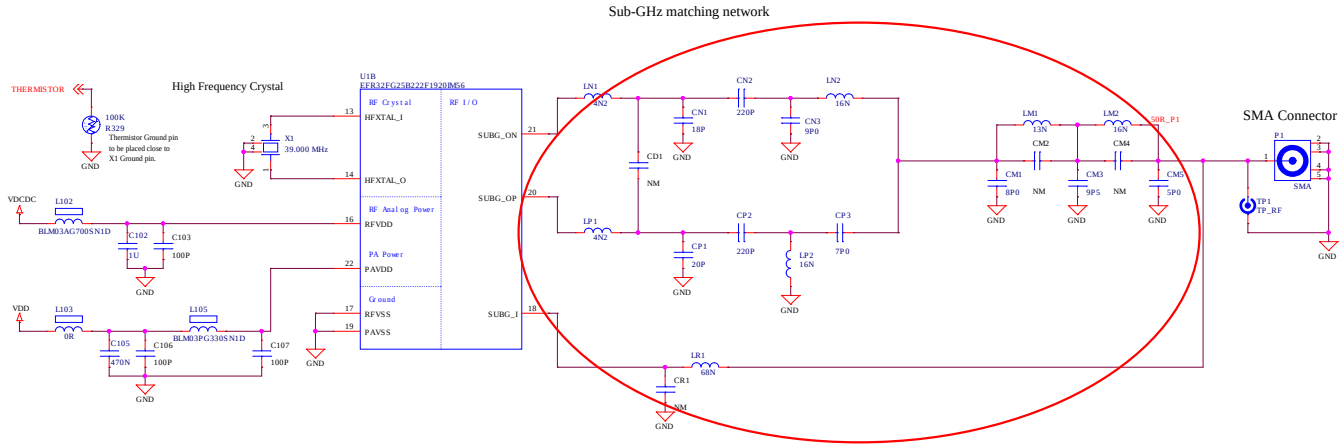


Figure 2.21. RF Section Schematic for the 470 MHz Band Full Discrete Match BRD4272A Radio Board (Matching Network is Highlighted)

Note: Matching network component values should be chosen based on the frequency band. However, while the matching structure is similar for the 868, 915, and 920 MHz bands, it is slightly different for the 470 MHz band as shown in the schematics above. Additionally, although the thermistor is not present on the full discrete match prototype radio board, it could be added to the design using the same layout considerations as for the 868, 915, and 920 MHz band external ceramic balun radio boards (BRD4270B and BRD4271A) or the 470 MHz band full discrete match radio board (BRD4272A) that comprises a thermistor, which can be used to obtain a stable XO crystal frequency. Thermistors change their resistance based on the temperature in their proximity; therefore, they can be used as a temperature sensor, which allows for the compensation of the temperature dependent frequency error of the XO crystal.

All radio boards for EFR32xG25 comprise an SMA connector, which can be used for conducted measurements or to connect an external antenna for radiated test purposes.

2.6 Matching Network Types for the EFR32xG27/29 Wireless MCU

This section provides matching networks recommended for use with EFR32xG27/29. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in 3.2.7 Additional Layout Design Guidelines for the EFR32xG27/29 Matching Networks.

EFR32xG27/29 is available in both QFN (QFN32/QFN40) and WLCSP (WLCSP39 for the xG27 and WLCSP45 for the xG29) packages. For both QFN and WLCSP packages, the recommended matching network is a T match (L-C-L) with a series dc blocking capacitor; however, the optimal matching network component values depend on the package type. The maximum achievable power is +8 dBm with the QFN buck, +6 dBm with the QFN boost dc-dc converter variant, and +6 dBm with the WLCSP package type (buck and boost mode).

The recommended matching network for EFR32xG27/29 QFN package types optimized for 0 / +8 dBm TX power (based on BRD4194A) is shown in the figure below:

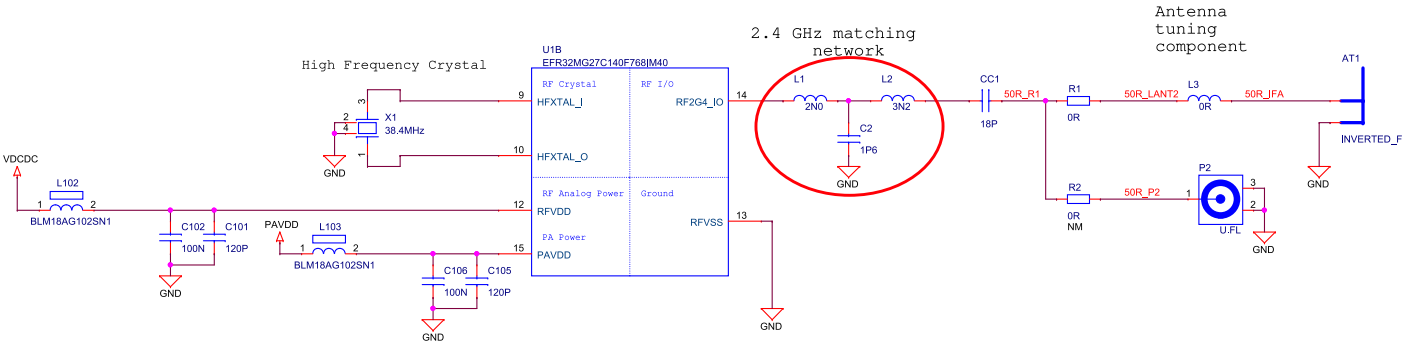


Figure 2.22. Matching Network for EFR32xG27/29 QFN Package Type

Note: The matching network above can be used for both the QFN buck and boost dc-dc converter variants. The series dc blocking capacitor (CC1) is mandatory when utilizing the 0 dBm PA and can be eliminated if only the high-power PA is used in the application.

The recommended matching network for EFR32xG27/29 WLCSP type optimized for 0 / +6 dBm TX power (based on BRD4110B / BRD4111B) is shown on the figure below:

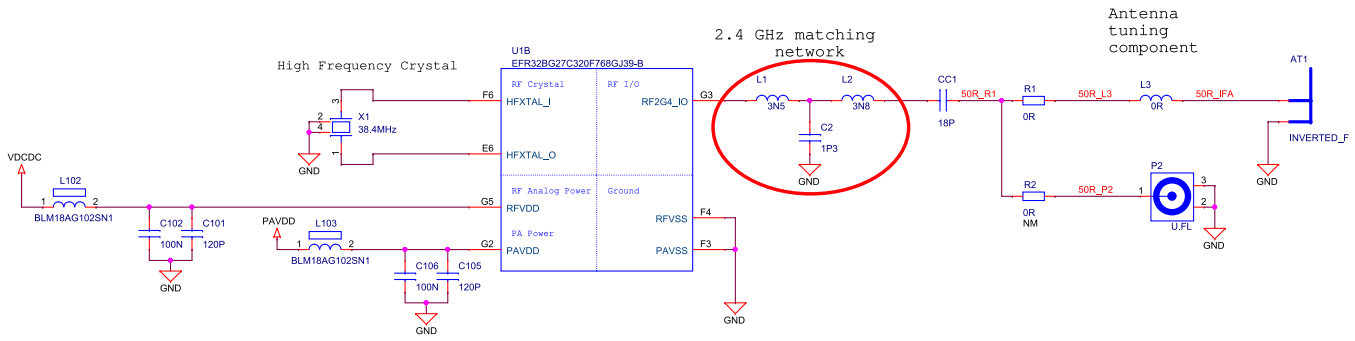


Figure 2.23. Matching Network for EFR32xG27/29 WLCSP Package Type

Note: The matching network above can be used regardless of the dc-dc operation mode (buck/boost). The series dc blocking capacitor (CC1) is mandatory when utilizing the 0 dBm PA and can be eliminated if only the high-power PA is used in the application.

Note: The RF validation of the WLCSP packages for xG27/29 was performed up to +4 dBm output power of the high power PA. However, +6 dBm capability has been thoroughly tested and deemed applicable up to 125 °C and will be referred to as the highest power level in this application note.

In the figures above, there is an additional component (L3) close to the antenna, which is basically not part of the matching network. For a custom design, it is recommended to leave the option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

2.7 Matching Network Types for the EFR32xG28 Wireless MCU

This section provides matching networks recommended for use with EFR32xG28. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing, and so it is recommended to follow the layout guidelines as documented in 3.2.8 Additional Layout Design Guidelines for the EFR32xG28 Matching Networks.

The EFR32xG28 wireless MCU is a dual-band device targeting applications that utilize both the Sub-GHz and 2.4 GHz bands. The RF front-end therefore consists of two separate matching networks leading to their respective antenna ports.

The recommended matching network for EFR32xG28 for the 868/915 MHz and 2.4 GHz band optimized for 14 dBm and 10 dBm TX power (based on BRD4400C) is shown in the figure below:

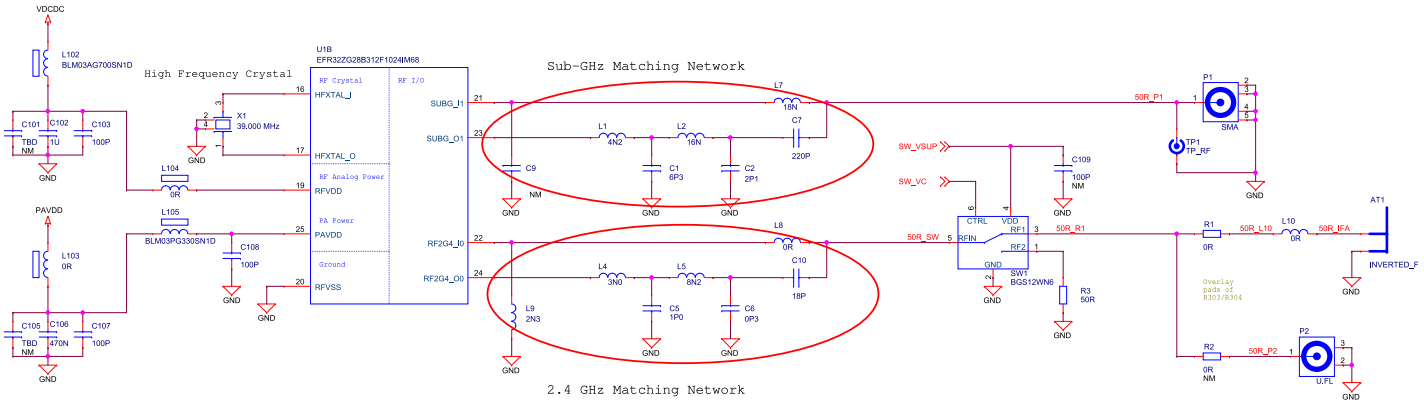


Figure 2.24. RF Section Schematic for the 868/915 MHz +14 dBm and 2.4 GHz +10 dBm BRD4400C Dual-band Radio Board (matching networks are highlighted)

The recommended matching network for EFR32xG28 for the 868/915 MHz and 2.4 GHz band optimized for 20 dBm and 10 dBm TX power (based on BRD4401C) is shown in the figure below:

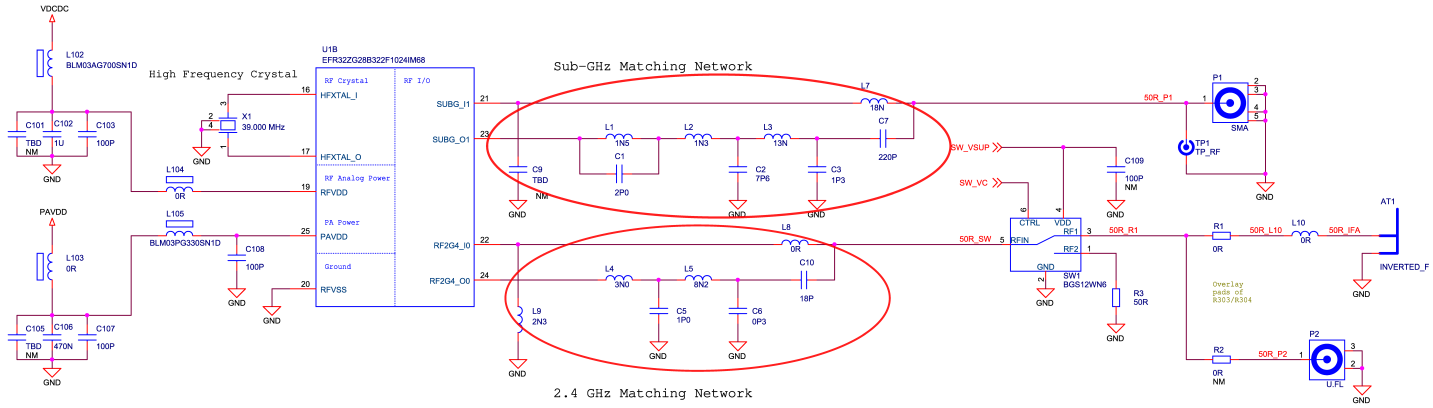


Figure 2.25. RF Section Schematic for the 868/915 MHz +20 dBm and 2.4 GHz +10 dBm BRD4401C Dual-band Radio Board (matching networks are highlighted)

EFR32xG28 is available in both QFN68 and QFN40 packages. Additionally, there are Sub-GHz/2.4 GHz and Sub-GHz/Sub-GHz versions of the device. The layout guidelines in this application note apply to all four package variants.

The RF switch at the output of the 2.4 GHz matching network is a crucial part of the design at 868 MHz Sub-GHz operation. Its purpose is to detach the 2.4 GHz antenna, preventing it from being a radiator for the 3rd harmonic (2604 MHz) that can couple onto the 2.4 GHz path.

Note: Refer to the device data sheets for the different sub-GHz matching network component vaues for the different frequencies and output power levels.

All radio boards for EFR32xG28 comprise an SMA and a U.FL connector, which can be used for conducted measurements or to connect an external antenna for radiated test purposes.

In the figures above, there is an additional component (L10) close to the antenna, which is basically not part of the matching network. For a custom design, it is recommended to leave the option for this series element for additional harmonic suppression, and its default value should be 0 Ω.

3. Guidelines for Layout Design When Using EFR32 Series 2 Wireless MCUs

3.1 General Layout Design Guidelines for EFR32 Series 2 Wireless MCUs

Some general guidelines for designing RF-related layouts for good RF performance are as follows:

- For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design, because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required.
- Avoid the separation of the ground plane metallization. It is recommended to create a unified ground plane on the PCB as much as possible which is not separated by traces. Also, the ground path between the matching network and the EFR32 IC exposed pad ground should be clear and unhindered on at least one of the PCB layers. The only exceptions for ground plane separation are the EFR32 matching network and HFXO areas, where the ground pins should NOT be connected to the Top layer ground. More details on these exceptions are provided in 3.2 Layout for the EFR32 Series 2 Wireless MCUs.
- Use as many grounding vias (especially near the GND pins) as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.
- Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic (the typical distance between vias on reference radio boards is 40–50 mil). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
- For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers.
- Avoid using long and/or thin transmission lines to connect the RF related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.
- Use tapered line between transmission lines with different width (i.e., different impedance) to reduce internal reflections.
- Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.
- Always ensure good VDD filtering by using some bypass capacitors (especially at the range of the operating frequency). The series self-resonance of the capacitor should be close to the filtered frequency. The bypass capacitor which filters the highest frequency should be placed closest to the VDD pins of the EFR32. In addition to the fundamental frequency, the crystal/clock frequency and its harmonics (up to the 3rd) should be filtered to avoid up-converted spurs.
- Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may be an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace.
- Place the RF-related parts (especially the antenna) far away from the dc-dc converter output and the related dc-dc components.
- Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.
- Use as short VDD traces as possible. The VDD trace can be a hidden, unwanted radiator so it is important to simplify the VDD routing as much as possible and use large, continuous GND pours with many stitching vias. To achieve the simplified VDD routing, try to avoid star topology of VDD traces (i.e., avoid connecting all VDD traces in one common point).
- Using silkscreen near the antenna could slightly affect the dielectric environment of the antenna. Although this effect is usually negligible, if possible, try to avoid using silkscreen on the antenna or on the antenna copper pour keep out areas.

3.2 Layout for the EFR32 Series 2 Wireless MCUs

Examples shown in this section are based on the layout of the following designs.

- BRD4180A (EFR32xG21)
- BRD4182A (EFR32xG22) with existing layout concept #1
- BRD4182A (EFR32xG22) with generic layout concept #2
- BRD4210A (EFR32xG23)
- BRD4186C (EFR32xG24)
- BRD4270B (EFR32xG25) with an external ceramic balun
- Full discrete match hardware design example (EFR32xG25)
- BRD4194A (EFR32xG27) or BRD4412A (EFR32xG29)
- BRD4400C (EFR32xG28)

The common layout design concepts are shown with the BRD4180A Radio Board layout to demonstrate the basic principles. Later on, separate sections will provide additional layout design guidelines to the matching network of the specific EFR32 families.

The layout structure for the RF part of the previously listed designs are shown in the figures below.

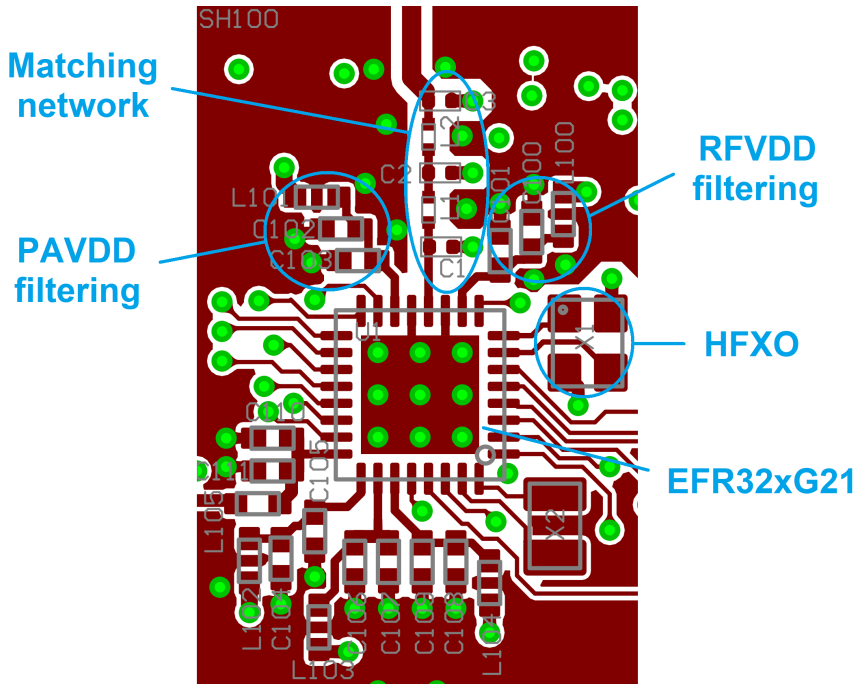


Figure 3.1. Layout of the RF Section for the BRD4180A Radio Board (Top Layer)

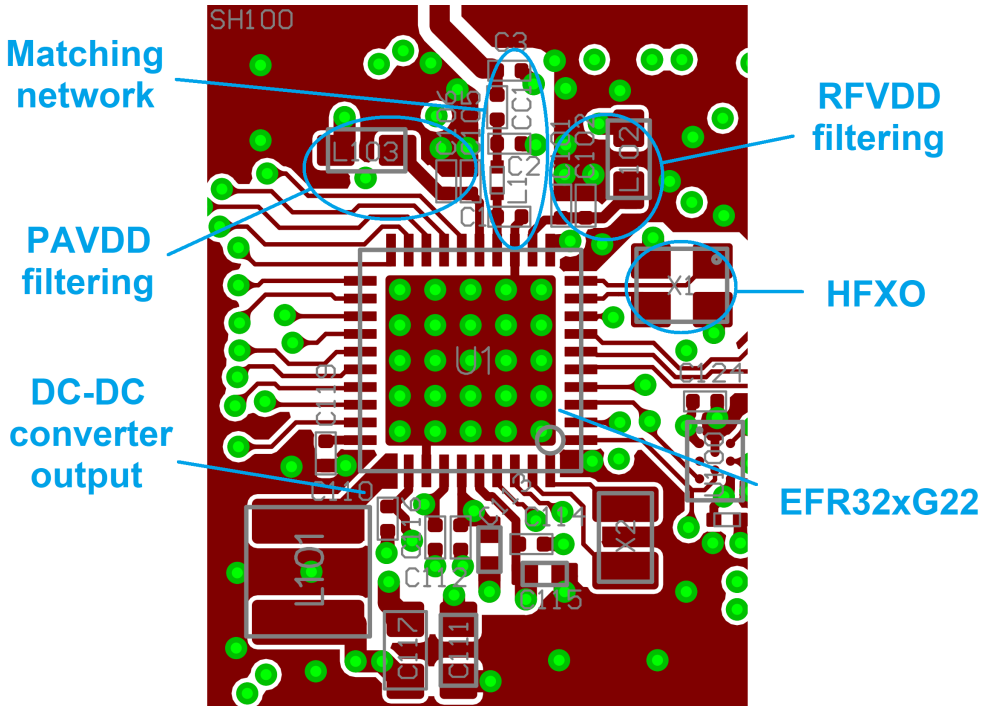


Figure 3.2. Layout of the RF Section for the BRD4182A (Rev B05) Radio Board with Existing Layout Concept #1 (Top Layer)

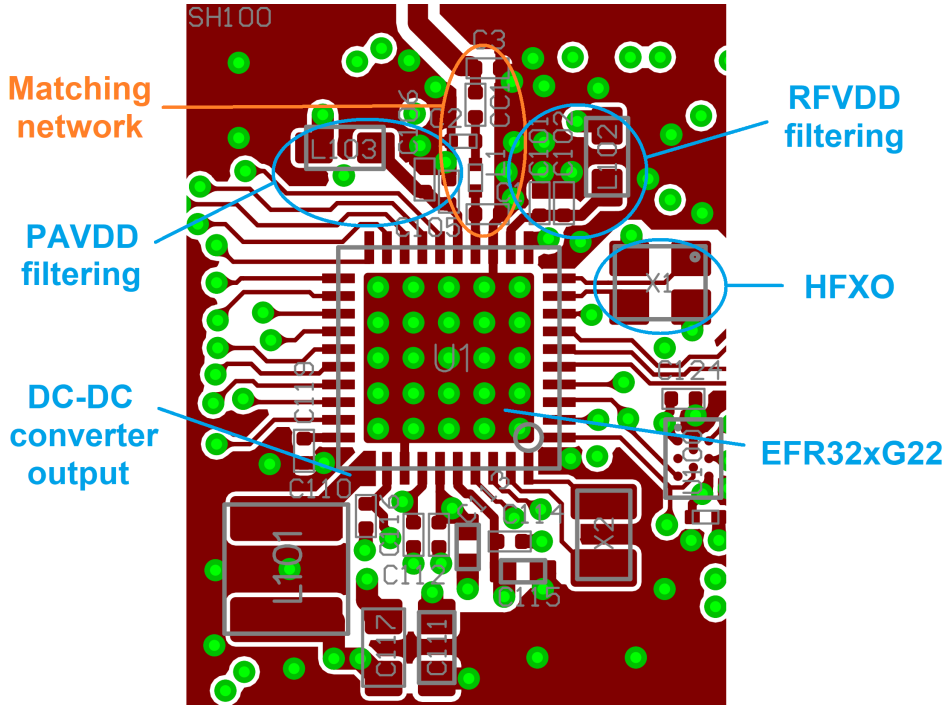


Figure 3.3. Layout of the RF Section for the BRD4182A (Prototype) Radio Board with Generic Layout Concept #2 (Top Layer)

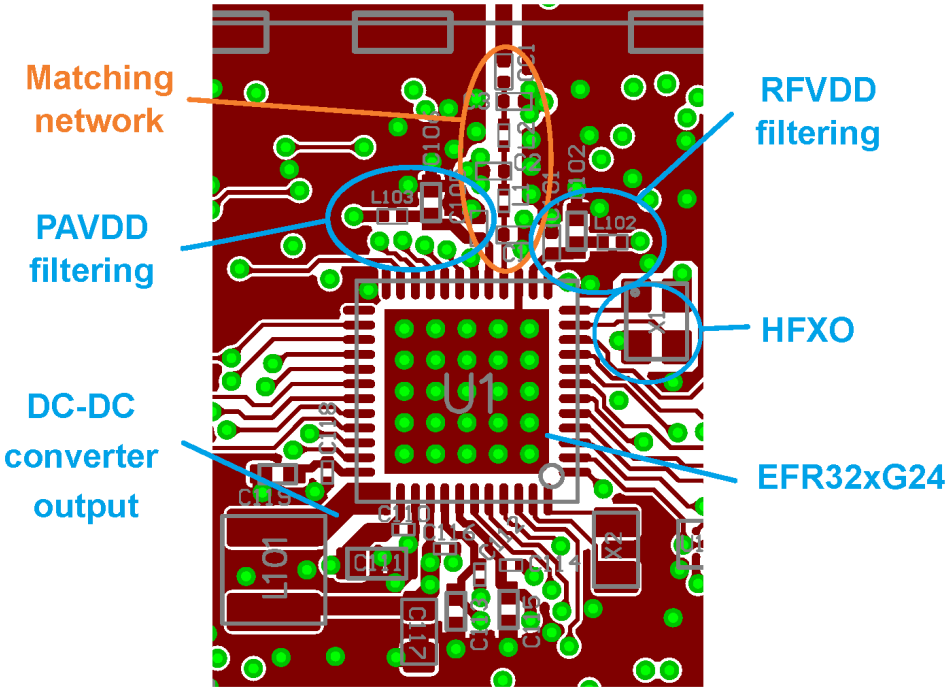


Figure 3.4. Layout of the RF Section for the BRD4210A Radio Board (Top Layer)

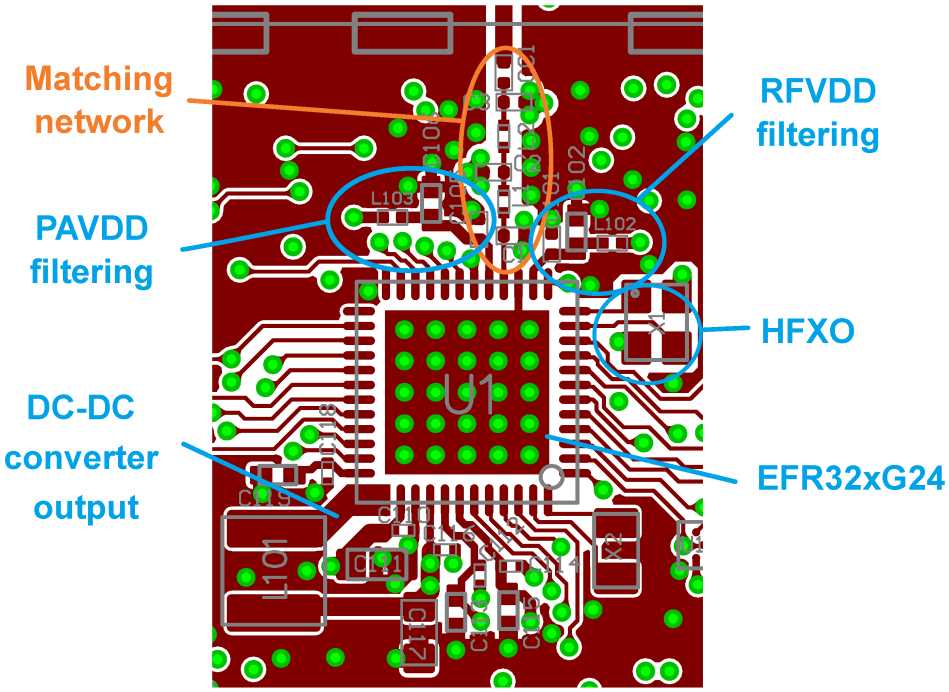


Figure 3.5. Layout of the RF Section for the BRD4186C Radio Board (Top Layer)

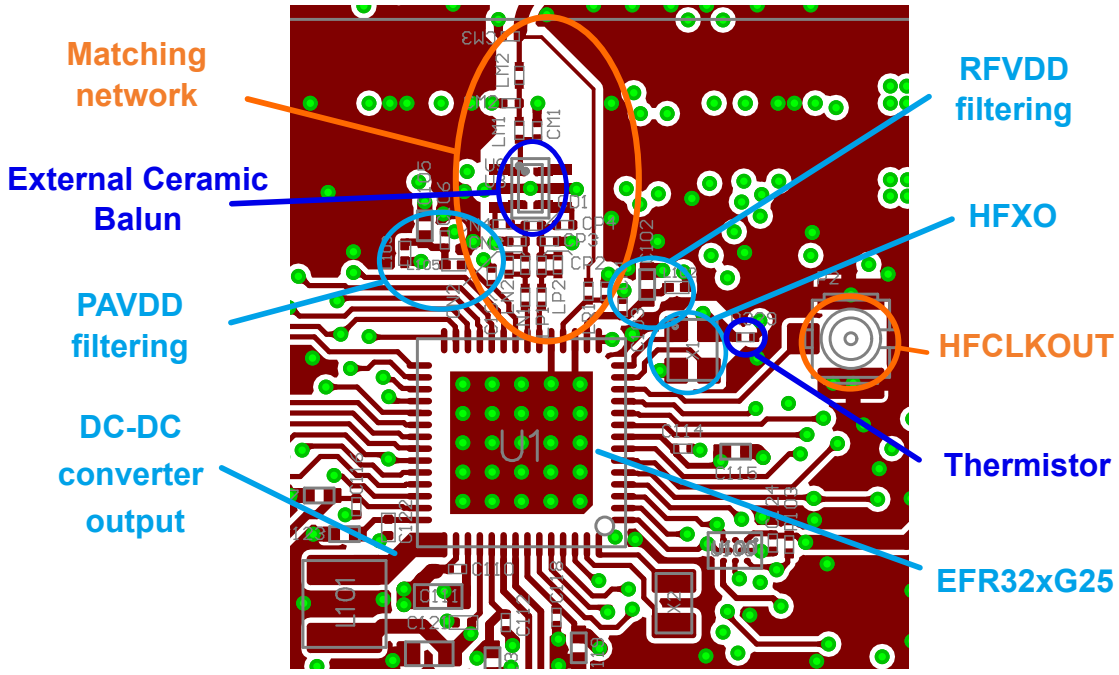


Figure 3.6. Layout of the RF Section for the BRD4270B Radio Board with an External Ceramic Balun (Top Layer)

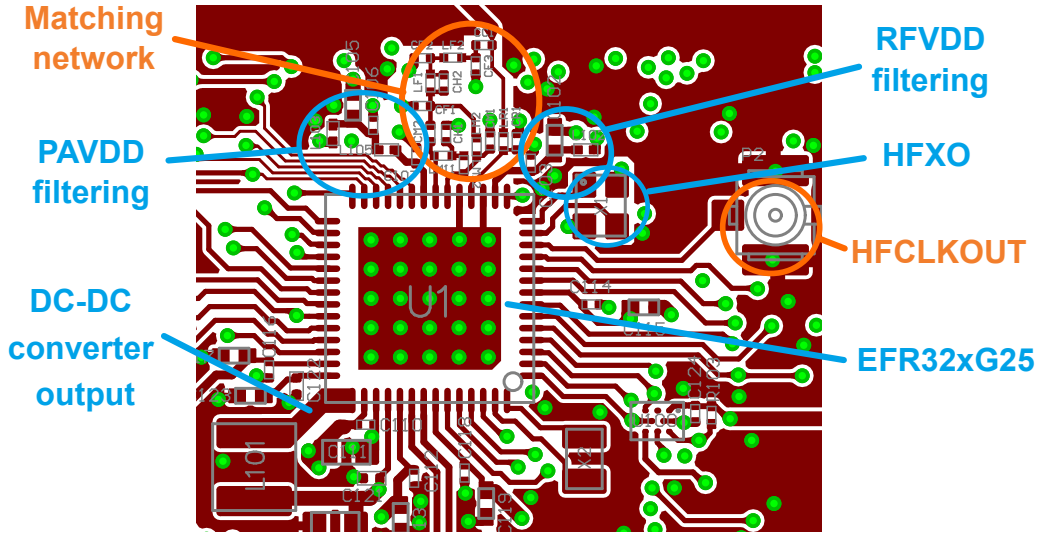


Figure 3.7. Layout of the RF Section for the 868, 915, and 920 MHz Band Full Discrete Match Prototype Radio Board (Top Layer)

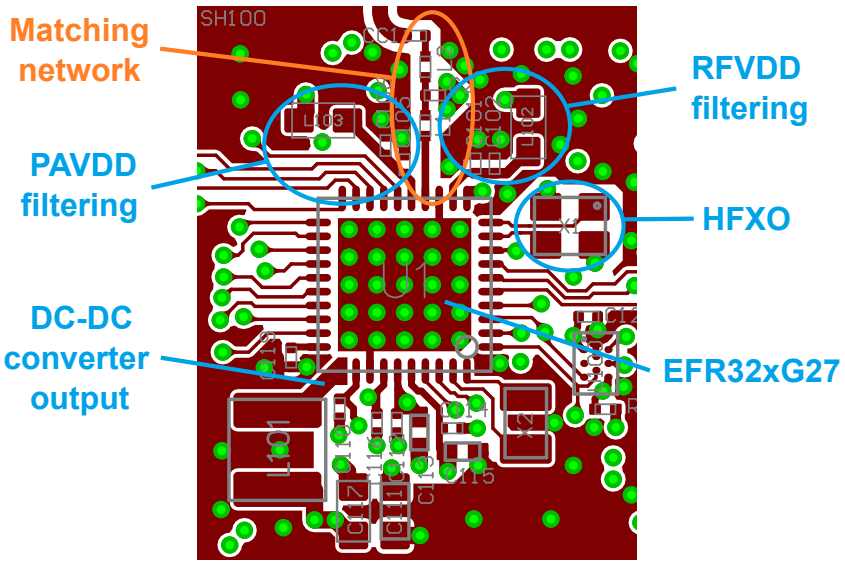


Figure 3.8. Layout of the RF Section for the BRD4194A or BRD4412A Radio Board (Top Layer)

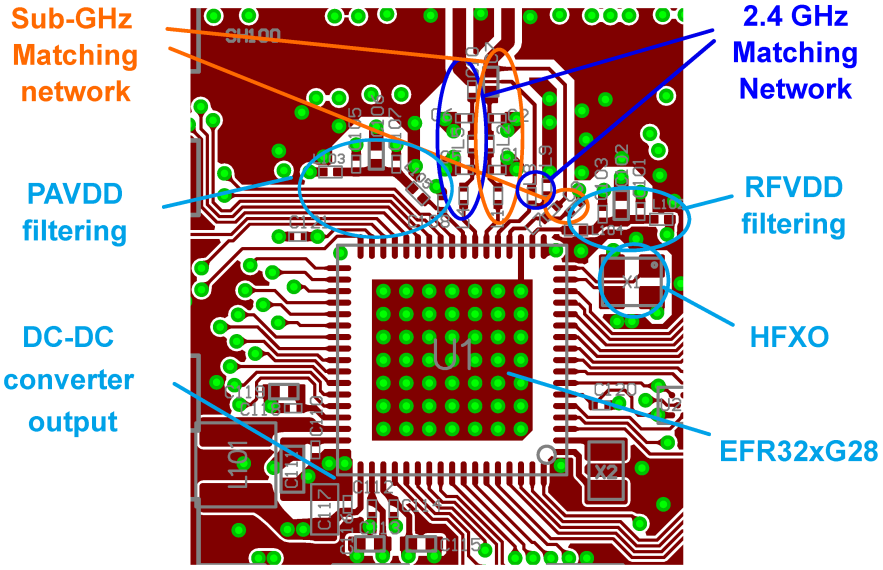


Figure 3.9. Layout of the RF Section for the 868/915 MHz +14 dBm and 2.4 GHz +10 dBm BRD4400C Dual-band Radio Board

3.2.1 Layout Design Guidelines for EFR32 Series 2 Wireless MCUs

- The lower-value VDD bypass capacitors (the ones with ~pF values) should be kept as close as possible to the VDD pins (RFVDD, PAVDD, AVDD, DVDD, IOVDD).
- To ensure good ground connection, all VDD filtering capacitors should use vias close to their ground pins. It is also recommended that the GND return path between the GND vias of the VDD filtering capacitors and the GND vias of the RFIC paddle should not be blocked in any way; return currents should have a clear and unhindered pathway through the GND plane to the back of the RFIC.
- The exposed pad footprint for the paddle of the EFR32 should use as many vias as possible to ensure good grounding and heat sink capability.
- The RF crystal should be placed as close as possible to the HFXTAL_I and HFXTAL_O pins of the EFR32 IC to minimize wire parasitic capacitances and any frequency offsets.
- The ground pins of RF crystal should be connected directly to the first inner layer ground plane using ground vias. Connecting the ground pins to the common ground metal on the Top Layer should be avoided.
- The series matching/filtering inductors should be placed one after another or perpendicular to each other to reduce coupling between stages.
- Traces near the GND pins of the capacitors should be thickened to improve the grounding effect in the thermal straps. This minimizes series parasitic inductances between the ground pour and the GND pins.

The figure below demonstrates the above listed layout design recommendations on the BRD4180A Radio Board.

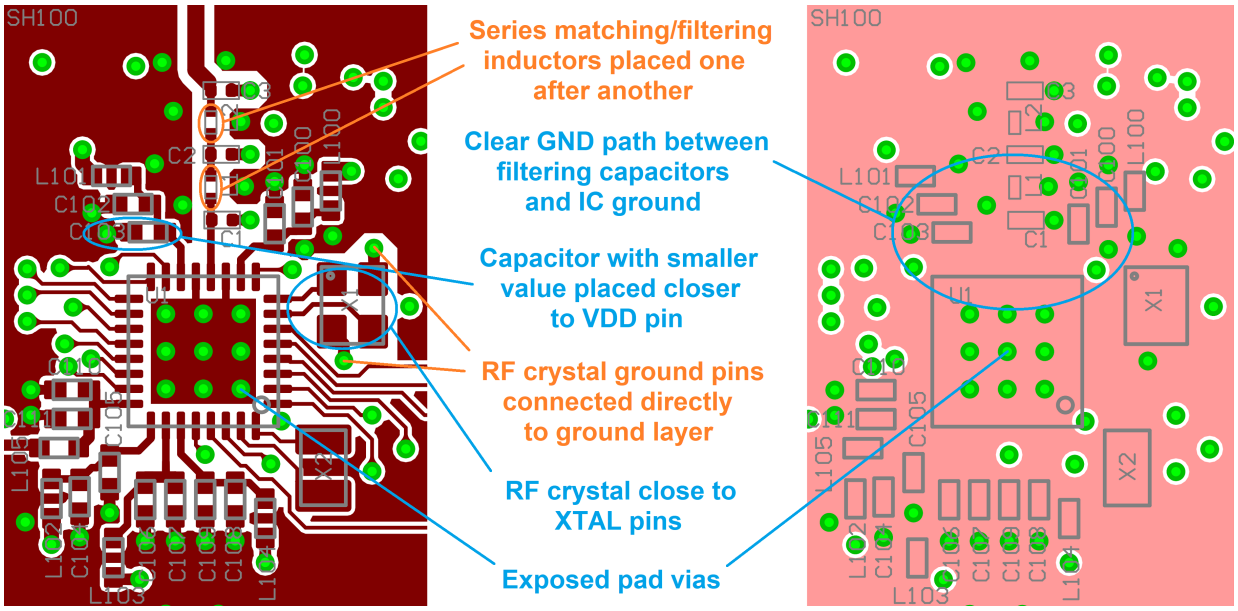


Figure 3.10. VDD Filtering, RF Crystal and Exposed Pad Ground Layout Guidelines on BRD4180A (Top Layer, Inner Layer 1)

- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering. Gaps should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to the restrictions of the actual radio board design. These restrictions include traces routed on other layers or components on the bottom side, which are not shown in the figure above.
- The area beneath the RF chip and the matching network (on the first inner layer) should be filled with continuous ground metal as it will show good ground reference for the matching network and will ensure a good, low impedance return path to the RF chip's ground as well. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX/RX matching network and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear, unhindered pathway through the GND plane to the back of the RFIC.
- Use an isolating ground metal between the crystal and RFVDD traces to avoid any detuning effects on the crystal caused by the nearby power supply and to avoid the leakage of the crystal/clk signal and its harmonics to the supply lines.

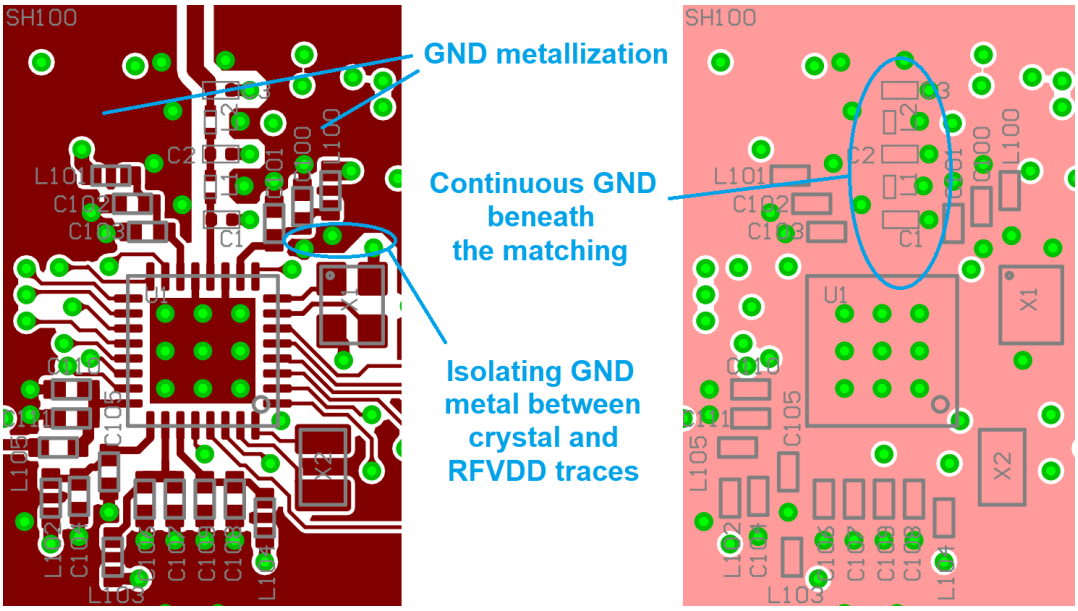


Figure 3.11. Ground Connection Layout Guidelines on BRD4180A (Top Layer, Inner Layer 1)

- Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VDD trace, to reduce their harmonic radiation caused by the fringing field.

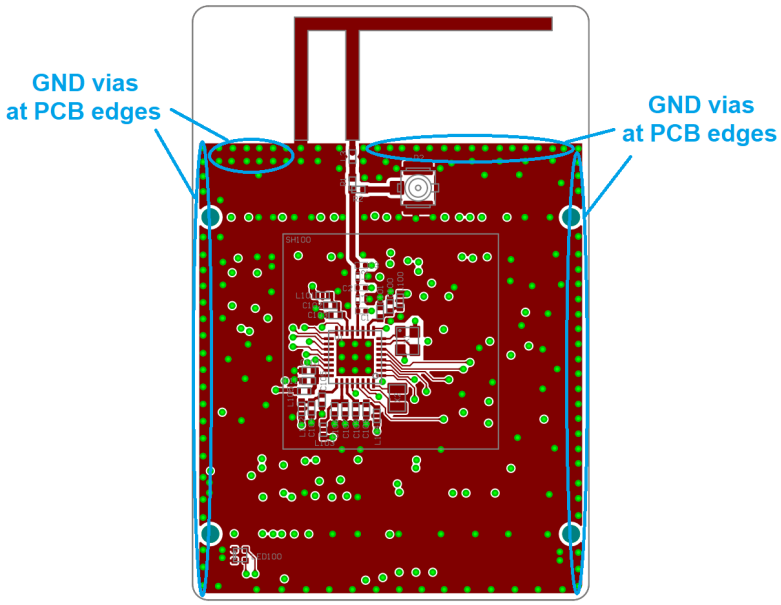


Figure 3.12. GND Vias at PCB Edges on BRD4180A Radio Board (Top Layer)

- If necessary, a shielding cap can be used to shield the harmonic radiations of the PCB; in that case, the shielding cap should cover all of the RF-related components (excluding the antenna).
- The ideal layer consistency for PCBs with more than two layers is as follows:

Top layer:	Use as much continuous solid GND metallization as possible with many vias.
First inner layer:	Use continuous, unified GND metallization beneath the RF part; wires can be routed beneath the non- RF parts if necessary.
All other inner layers:	Route as many (supply and digital) traces on these layers as possible.
Bottom layer:	This layer should be unified GND metal; route traces on this layer only if necessary.

The following figure illustrates layer consistency on the layout of BRD4180A Radio Board.

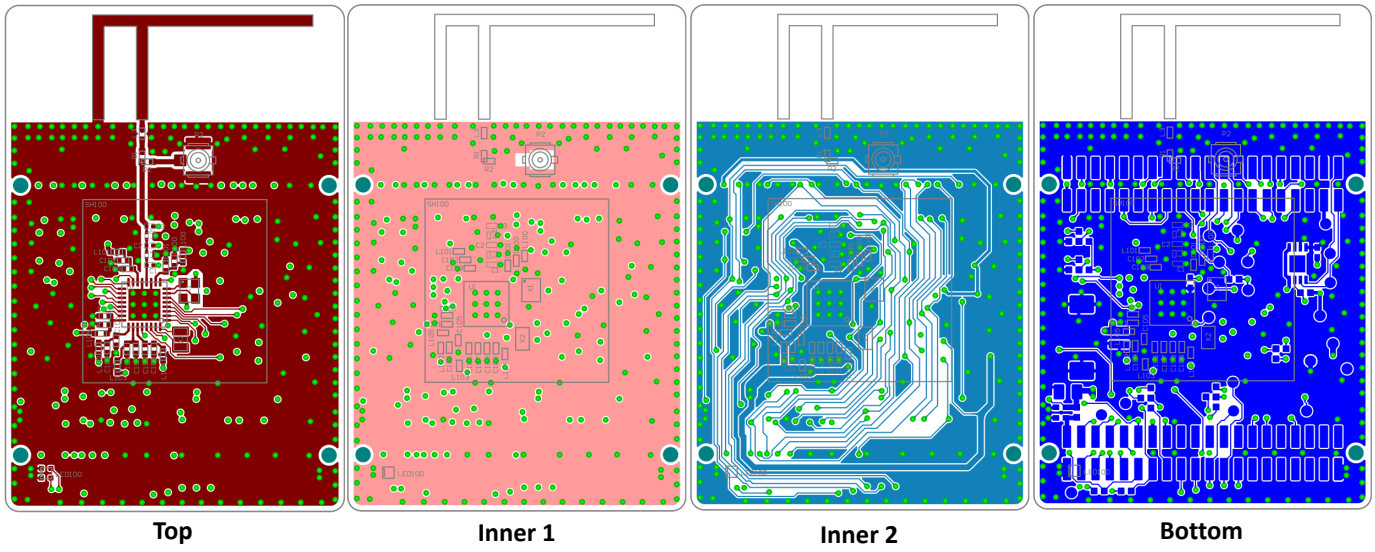


Figure 3.13. Layer Consistency on BRD4180A Radio Board

- Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.
- Avoid placing the supply lines close to the PCB edge.
- To reduce sensitivity to PCB thickness variations, use 50 Ω grounded coplanar lines where possible for connecting the antenna or the U.FL connector to the matching network. This also reduces radiation and coupling effects. A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency.
- The interconnections between elements are not considered transmission lines since their lengths are much shorter than the wavelength, and, thus, their impedances are not critical. As a result, their recommended width is equal to the width of the pad of the applied components. In this way, reflections at pad-trace transitions can be prevented, and parasitic capacitances to ground can be minimized. Examples for the trace dimensions are shown in the table below.
- Use many vias near the coplanar lines in order to minimize radiation.

The following figure demonstrates the 50 Ω grounded coplanar lines on the layout of the BRD4180A Radio Board.

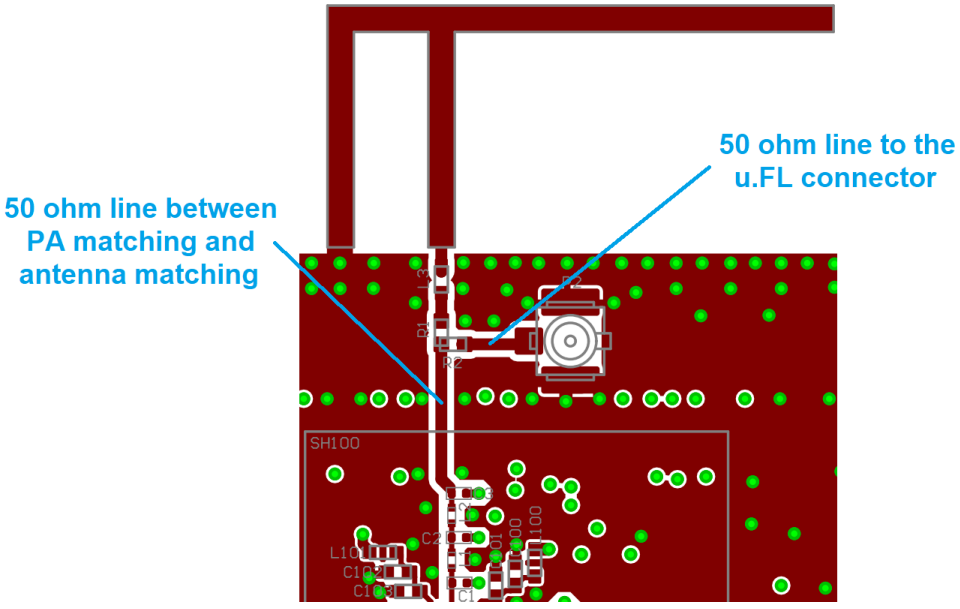


Figure 3.14. 50 Ω Grounded Coplanar Lines on BRD4180A Radio Board (Top Layer)

Table 3.1. Parameters for 50 Ω Grounded Coplanar Lines

Lines	Parameters
f	2.4 GHz
T	0.018-0.035 mm
εr	4.6
H	0.3 mm
G	0.25 mm
W	0.45 mm

Note:

- For PCBs with more than 2 layers, 'H' is the distance between the top and the first inner layer. For 2-layer PCBs, 'H' is the distance between the top and the bottom layer.
- The example in the table above is based on the parameters for the 4-layer BRD4180A Radio Board. Other radio boards may have a different PCB layer stack-up. Refer to the PCB specification file for the particular radio board PCB stack-up details.
- A 2-layer PCB requires different parameters for a 50 Ω transmission line than shown in this table due to the different value of "H".
- Characteristic impedance is not “super sensitive” to the gap value. It should be between 0.25 and 0.4 mm to have 47 through 53 Ω impedance.
- Different impedance calculators may yield slightly different results.

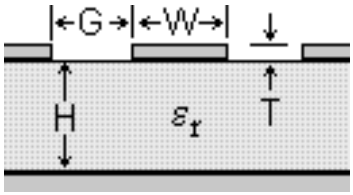


Figure 3.15. Grounded Coplanar Line Parameters

3.2.2 Additional Layout Design Guidelines for the EFR32xG21 Matching Networks

- It is strongly recommended to keep ~1 mm distance between the C1 capacitor and the corresponding TX/RX pin (RF2G4_IO1 or RF2G4_IO2) of the EFR32xG21 IC (on the BRD4180A Radio Board, the actual distance between C1 capacitor and the TX/RX pins is 0.95 mm). The additional parasitic inductance of this short trace is part of the matching network, increased harmonic levels can be expected if not kept precisely.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- In most of the cases, better harmonic performance can be obtained when the consecutive harmonic filtering capacitors in the matching network are rotated to the opposite sides of the transmission line. However, validation results of the EFR32xG21 chip showed that applying such a positioning for the matching network components increases harmonic levels. Therefore, it is recommended to connect the nearby shunt capacitors in the matching network to the **same side of the transmission line** for the EFR32xG21 device.
- Shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using ground vias. Connecting the ground pins to the common ground metal on the Top Layer should be avoided in order to get optimal harmonic performance.
- The EFR32xG21 chip has 2 equivalent single-ended TX outputs / RX inputs. If only one of these outputs / inputs are used with the 10 dBm or the 20 dBm PA matching network, the other one should be connected directly to the exposed pad ground. Make sure not to connect the unused TX / RX pin to the common top layer ground of the PCB as it may increase harmonic levels.
- To achieve better harmonic performance, it is also recommended to connect pin 11 (RFVSS) to the exposed pad ground directly and not to connect it to the common top layer ground.
- Use at least 0.3 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

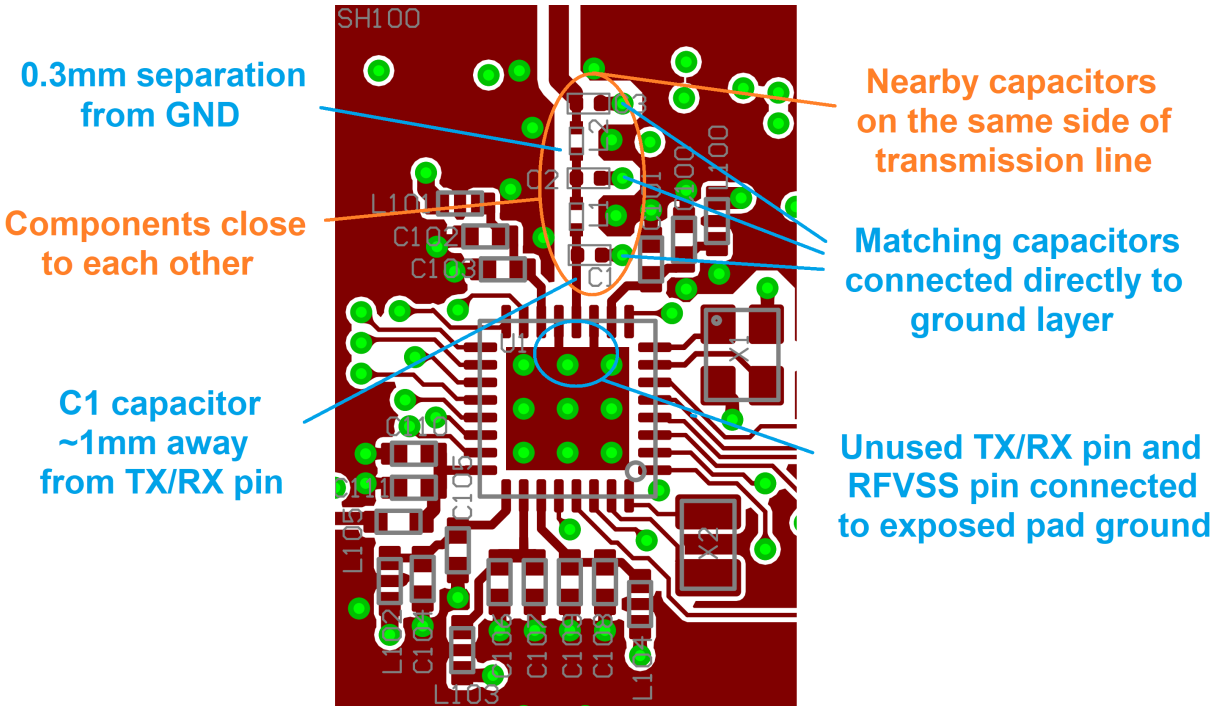


Figure 3.16. Matching Network Layout Guidelines on BRD4180A (Top Layer)

The recommended matching networks for 0 dBm and 0 / 10 dBm output power levels are shown in Figure 2.4 Recommended Matching Network for EFR32xG21 for 0 dBm Output Power on page 5 and Figure 2.5 Recommended Matching Network for EFR32xG21 for 0 / 10 dBm Output Power on page 5.

For the 0 dBm matching network the harmonics are well below the FCC limits, therefore the connection of the 0.5 pF capacitor at the unused RF port (C208) does not affect regulatory compliance. The default and recommended connection is to connect the ground pin of this capacitor directly to the inner layer ground without connecting it to the common TOP layer ground or BOTTOM layer ground as shown in the Figure 3.17 Capacitor at Unused RF Pin Placed on TOP Layer on page 30.

When using the 0 dBm PA with the 0 / 10 dBm matching network, similarly as in the 0 dBm matching network case, the connection of the 0.5 pF capacitor at the unused RF port (C208) does not affect regulatory compliance. However, for the 10 dBm PA with the 0 /10 dBm matching network the placement of the 0.5 pF capacitor might have effect on harmonic compliance. Therefore, two recommended configurations of this capacitor are possible:

- Default Configuration: Placed on TOP layer, direct connection to inner layer ground, no connection to common TOP layer ground or BOTTOM layer ground. See in Figure 3.17 Capacitor at Unused RF Pin Placed on TOP Layer on page 30.
- Alternative Configuration: Placed on BOTTOM layer, no ground connection to inner layer ground, direct connection to BOTTOM layer ground. See in Figure 3.18 Capacitor at Unused RF Pin Placed on BOTTOM Layer on page 30.

Note: Both capacitor configurations meet the FCC limits for EFR32xG21, however 2 dB improvement can be achieved at the radiated 5th harmonic when placing the 0.5 pF capacitor on the BOTTOM side compared to the TOP side placement. For simplicity of the matching network structure on the PCB layout, the default and recommended placement of this capacitor is on the TOP layer. Alternatively, the BOTTOM side placement can be applied to further improve radiated 5th harmonic suppression.

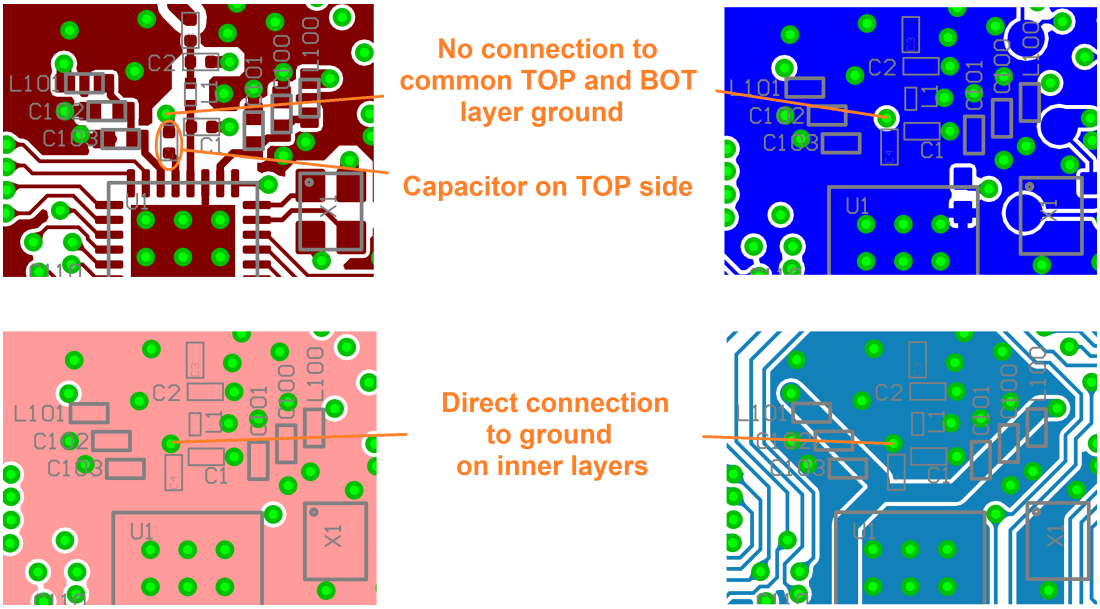


Figure 3.17. Capacitor at Unused RF Pin Placed on TOP Layer

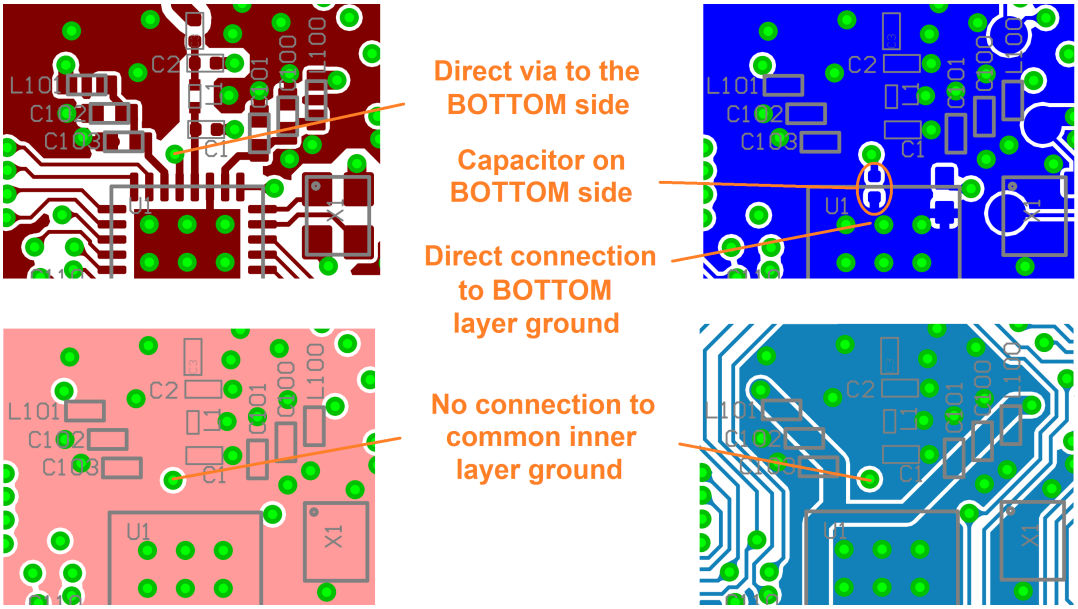


Figure 3.18. Capacitor at Unused RF Pin Placed on BOTTOM Layer

3.2.3 Additional Layout Design Guidelines for the EFR32xG22 Matching Networks

As discussed in 2.2 Matching Network Types for the EFR32xG22 Wireless MCU, two different approaches are available when designing matching network for EFR32xG22, as follows:

- Existing concept
- Generic concept

Silicon Labs recommends following the generic layout concept number two due to robustness, better margin on radiated harmonics and higher output power capability. The following sections will show the specific layout design guidelines for the above mentioned 2 layout concepts.

3.2.3.1 Layout Design Guidelines for the Pi-Matching Network with the Existing Layout Concept #1

- It is strongly recommended to place the C1 capacitor as close to the RF2G4_IO pin of the EFR32xG22 IC as possible. Also, the ground pin of this capacitor should be connected directly to the exposed pad ground through pin 13 (RFVSS), while connecting that pin to the Inner layer ground or to the common Top layer ground should be avoided.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Connect the nearby shunt capacitors in the matching network to the **same side of the transmission line** for the EFR32xG22 device.
- Shunt capacitors in the matching network (except for C1) should be connected directly to PCB Layer 2 ground plane using ground vias. Connecting the ground pins to the common ground metal on the Top Layer should be avoided in order to get optimal harmonic performance.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 70 mils.

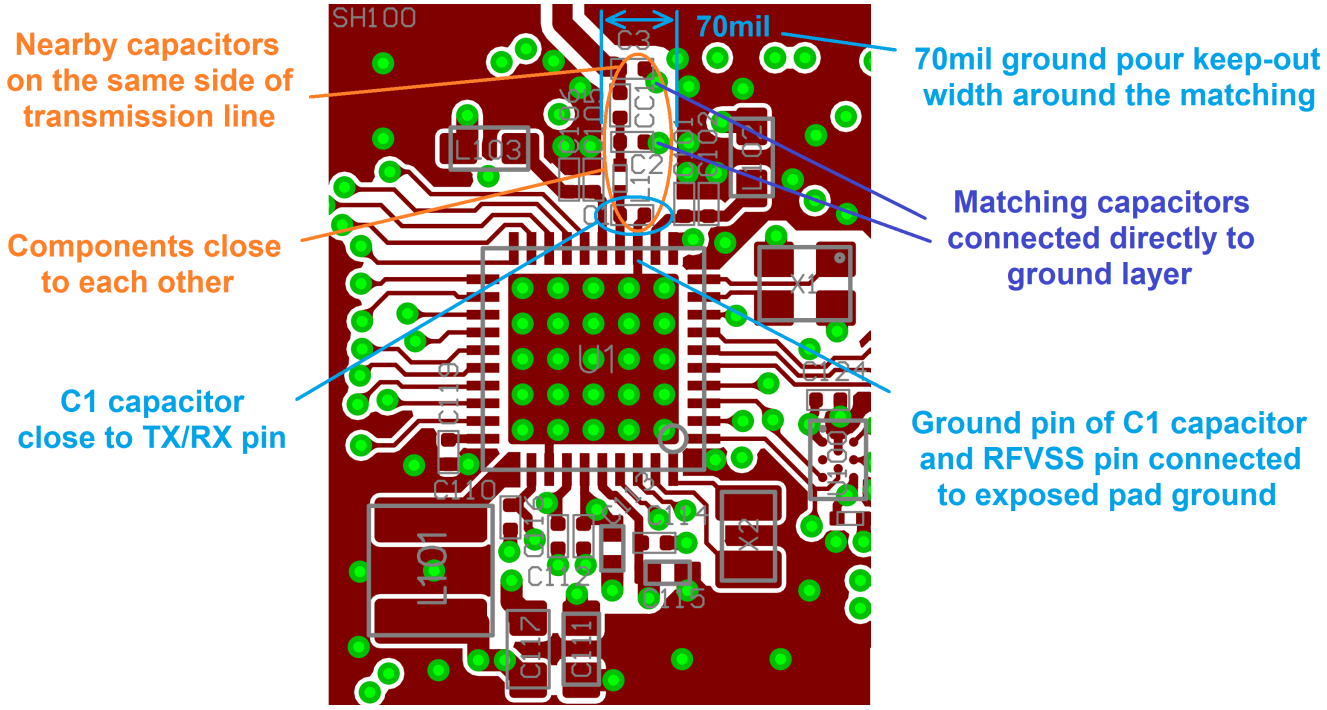


Figure 3.19. Pi-Matching Network Layout Guidelines on BRD4182A (Rev B05) with Existing Layout Concept #1 (Top Layer)

3.2.3.2 Layout Design Guidelines for the Pi-Matching Network with the Generic Layout Concept #2

- Place the C1 capacitor as close to the RF2G4_IO pin of the EFR32xG22 IC as possible. Also, the ground pin of this capacitor should be connected both to the exposed pad ground through pin 13 (RFVSS) and to the common Top layer ground pour.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Connect the nearby shunt capacitors in the matching network to the **opposite side of the transmission line** for the EFR32xG22 device.
- The shunt matching capacitors should be connected to the component-layer GND pour with multiple stitching vias.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 37 mils.

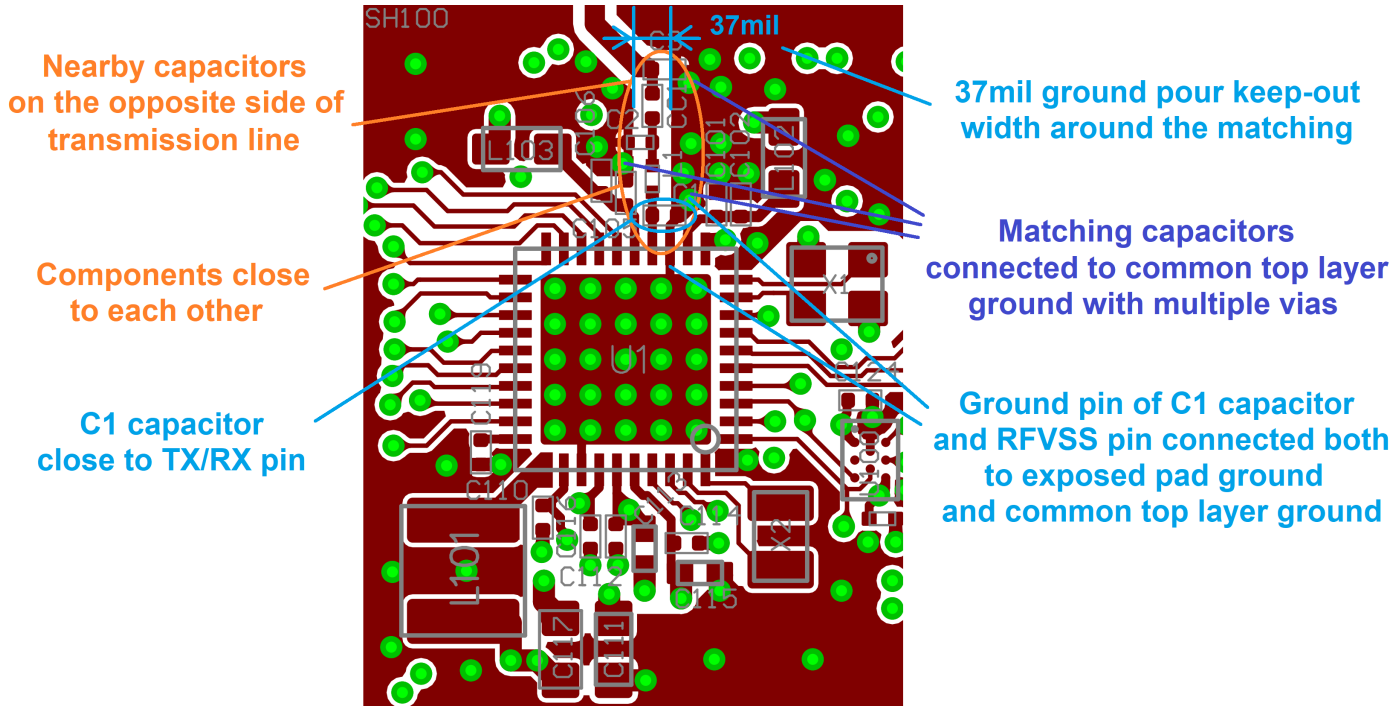


Figure 3.20. Pi-Matching Network Layout Guidelines on BRD4182A (Prototype) with Generic Layout Concept #2 (Top Layer)

3.2.3.3 Layout Design Guidelines for the T-Match with Generic Layout Concept #2

- Place the L1 inductor as close to the RF2G4_IO pin of the EFR32xG22 IC as possible. Note that Silicon Labs test results are based on a PCB design where both the Pi-match and the T-match can be mounted. If such flexible PCB design is desired, place the C1 capacitor closest to the RF2G4_IO pin.
- RFVSS pin (next to the RF2G4_IO pin) should be connected to the Top Layer ground with additional ground vias to internal ground layers.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Rotate the shunt capacitor of the T-matching network to the PAVDD side of the transmission line.
- The shunt matching capacitor should be connected to the component-layer GND pour with multiple stitching vias.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 37 mils.

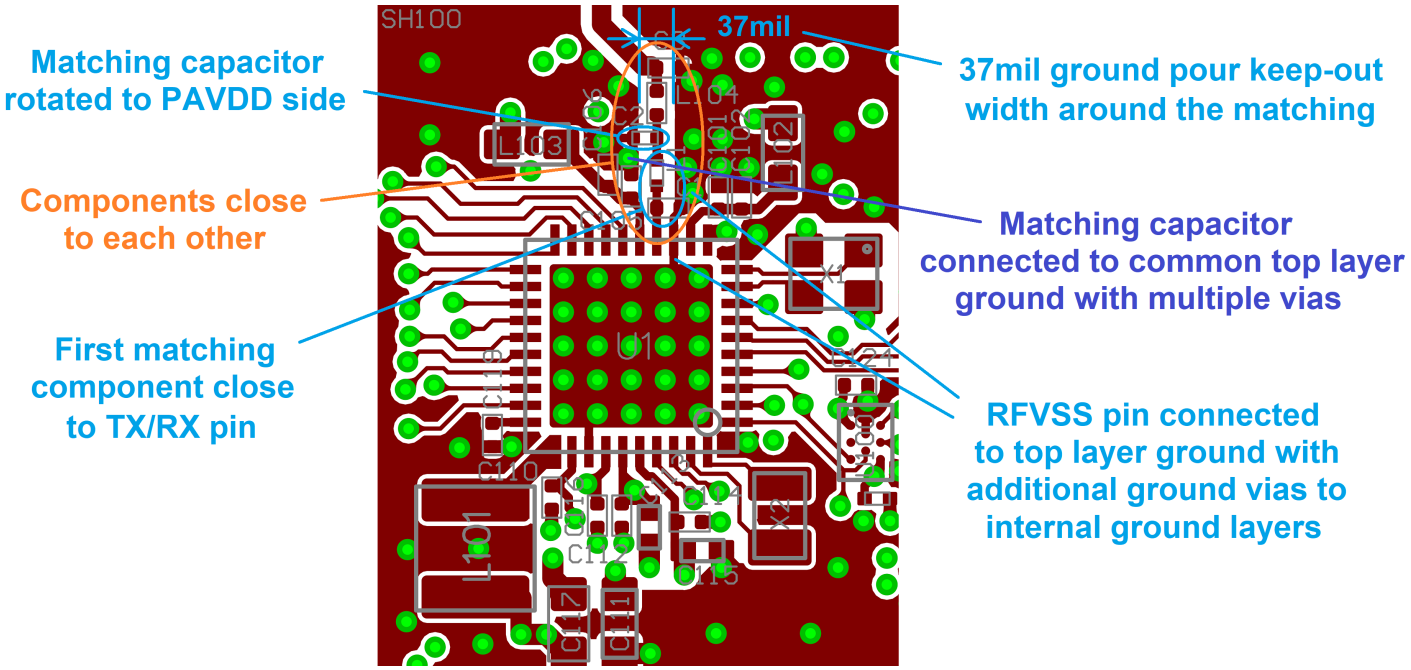


Figure 3.21. T-Matching Network Layout Guidelines on BRD4182A (Prototype) with Generic Layout Concept #2 (Top Layer)

3.2.4 Additional Layout Design Guidelines for the EFR32xG23 Matching Networks

- It is recommended to keep ~1 mm distance between the first element of the TX matching network and the SUBG_O0 or SUBG_O1 pins of the EFR32xG23 IC (on the BRD4210A Radio Board, the actual distance between C1 capacitor and the TX/RX pins is 0.93 mm). The additional parasitic inductance of this short trace is part of the matching network; increased harmonic levels can be expected if not kept precisely. This effect is more significant in high-band sub-GHz frequencies (868/915 MHz), while the effect is negligible below 500 MHz.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Connect the nearby shunt capacitors in the matching network to the same side of the transmission line for the EFR32xG23 device.
- Shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using ground vias. Connecting the ground pins to the common ground metal on the top layer should be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect pin 15 (RFVSS) to the exposed pad ground directly and not to connect it to the common top layer ground.
- Use at least 0.5 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

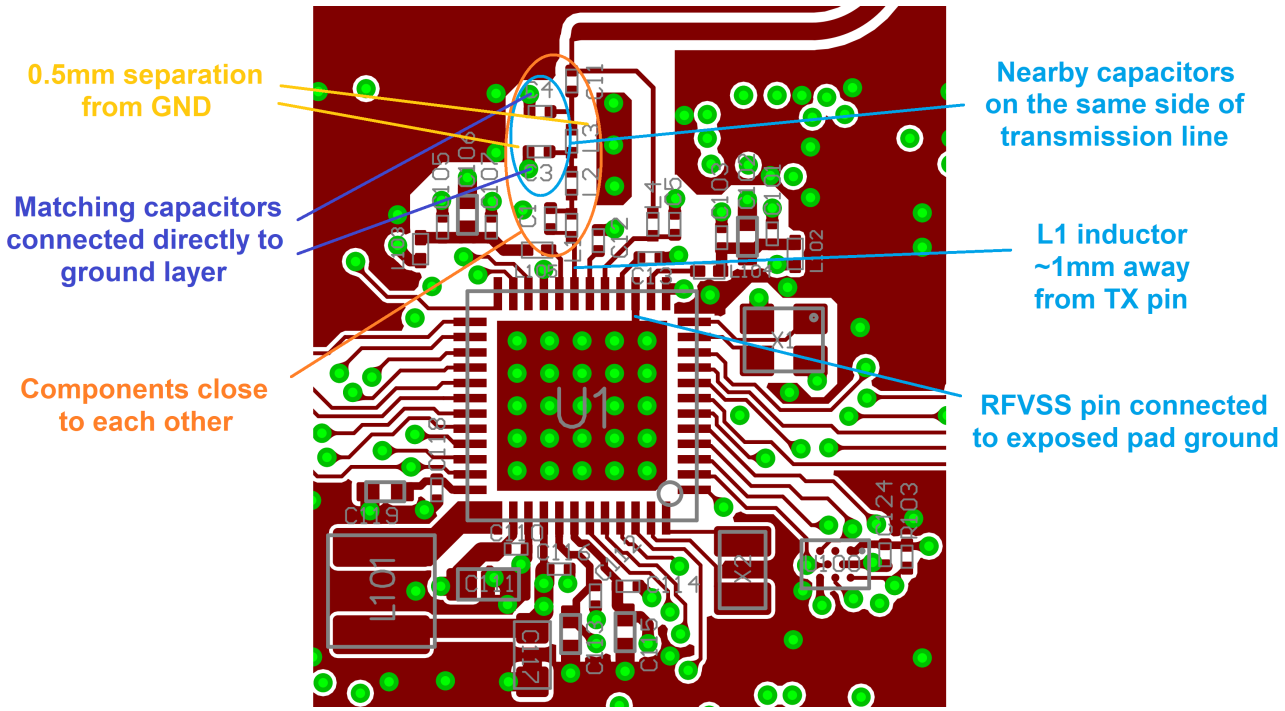


Figure 3.22. Matching Network Layout Guidelines on BRD4210A (Top Layer, part 1)

- Add a ground copper isolation between TX and RX matches to reduce coupling between TX and RX stages.
- Copy the RX matching structure as is: the additional traces that connect the RX matching inductor to the SUBG_I0 pin and to the common direct-tie point of the matching network can be considered as parasitic inductance and these traces are playing part in the matching network. These additional traces should also be applied when using a matching network type other than direct-tie type (e.g., matching network with RF switch or FEM). If different trace lengths are used, the RX matching network can be detuned from its optimal form and additional tuning might be required. The effect of these traces is significant in high-band sub-GHz frequencies (868/915 MHz), while the effect is less remarkable below 500 MHz.
- PAVDD and RFVDD filtering capacitors should be connected directly to PCB Layer 2 ground plane using ground vias. Connecting the ground pins of these capacitors to the common ground metal on the top layer should be avoided.

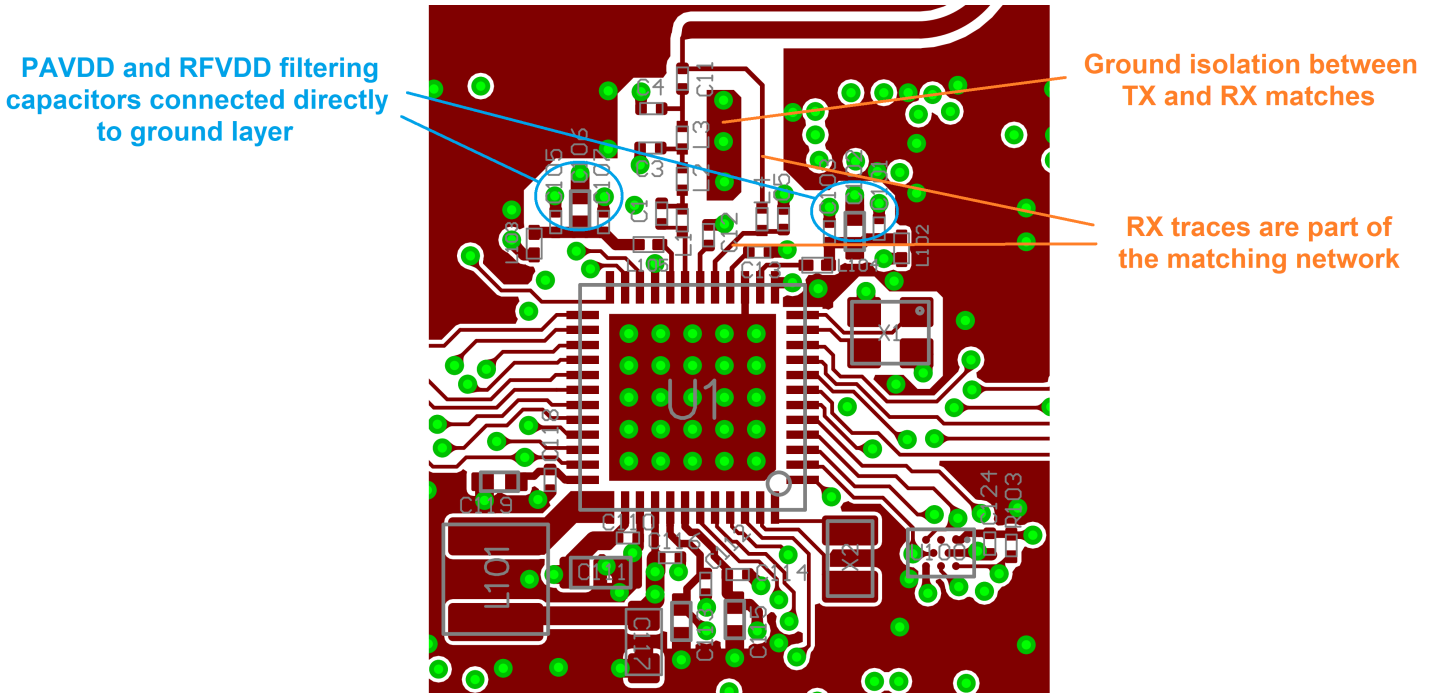


Figure 3.23. Matching Network Layout Guidelines on BRD4210A (Top Layer, part 2)

3.2.4.1 Specific Layout Design Guidelines for the QFN40 RFIC with HFCLKOUT Pin

Specific EFR32xG23 parts are available with a HFCLKOUT pin. The function of this pin is to provide the high frequency clock signal generated by the crystal oscillator (HFXO) to other EFR32 devices when connected in cascade. That way it is sufficient to use a single crystal on the PCB. The layout design guidelines regarding this pin are as follows:

- The HFCLKOUT trace should be as short as possible to avoid any signal delays between the EFR32 devices.
- The width of the trace should be equal to width of the pins it is connecting to at their connection points.
- Surround the HFCLKOUT trace with GND pour to avoid crosstalk between other traces.

Alternatively, routing the HFCKLOUT trace on an inner layer is also a solution as long as there is a GND plane between the top and that inner layer.

Note: Using the HFCLKOUT version of the 40 pin EFR32xG23 requires an additional GPIO pin assignment to enable/disable the HFCLKOUT signal between the cascaded EFR32 devices.

3.2.4.2 Specific Layout Design Guidelines for 2 RF Front-End Use

As you can see in the figure below, the EFR32xG23 RF front-end consists of two pairs of RX-TX paths. This diversity allows for the possibility of using the RFIC for dual-band applications by using both of these paths, with their separate dedicated antennas and matching networks. Note, that it would be possible to use a single antenna for dual-band applications, but that would require a dual-band matching network which is more challenging to construct.

The additional layout guidelines when all four RF pins are used are as follows:

- The trace of the SUBG_I0 RX pin should cross trace of the SUBG_O1 TX trace under the dc-blocking capacitor. It is recommended to choose the size of the capacitor larger than the rest of the components of the matching network (0201 size SMDs) to allow the trace to properly pass under it.
- The length of RX traces should be chosen to a similar value as in our design. The inductance of wires with this length are not negligible and are part of the matching network design.
- It is possible to root the RX traces on an inner layer, if there is a ground plane between that layer and the top layer. However, there are not any validated designs of this sort available, so it is recommended to root the RX traces on the top layer.

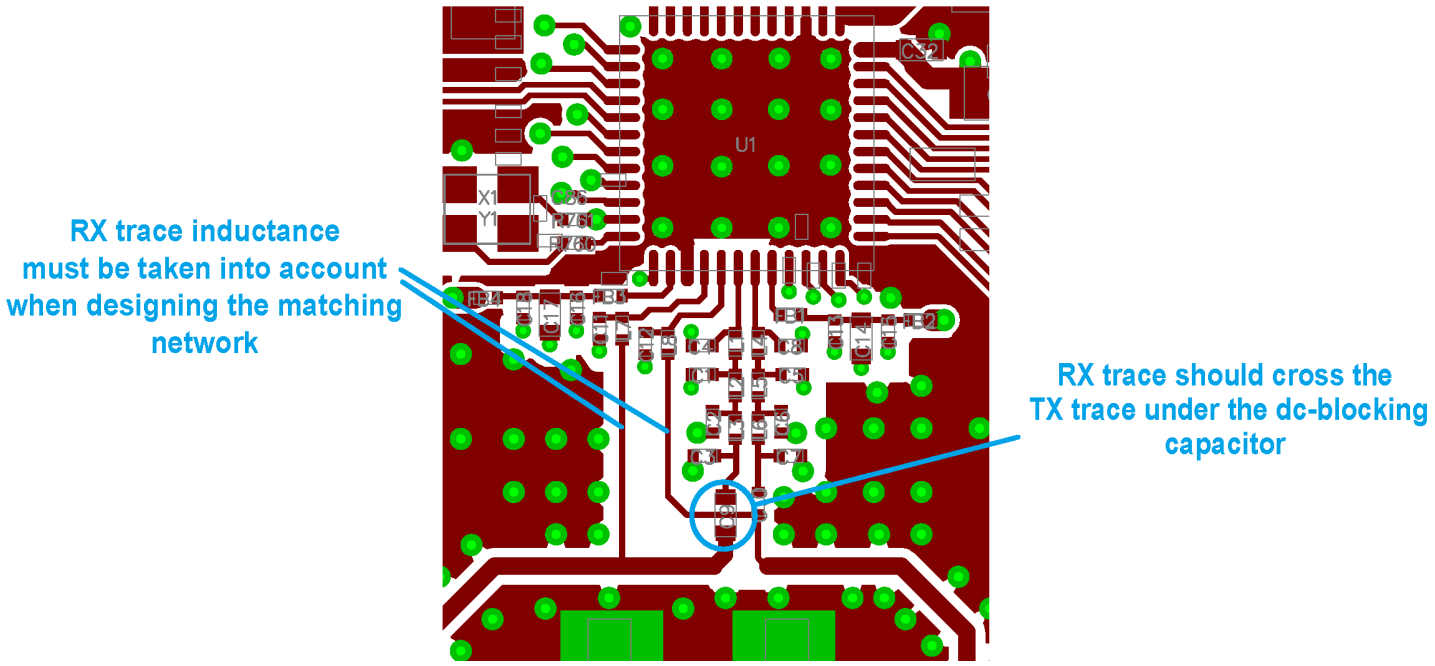


Figure 3.24. Matching Network Layout Guidelines for 2 RF Front-End Use (Top Layer)

3.2.5 Additional Layout Design Guidelines for the EFR32xG24/26 Matching Networks

As discussed in 2.4 Matching Network Types for the EFR32xG24 Wireless MCU, QFN, WLCSP (xG24), and BGA (xG26) packages require different matching network topologies. Also, for QFN packages, two different approaches are available when designing matching network for EFR32xG24, as follows:

- Layout for low power applications (≤10 dBm)
- Layout for high power applications (>10 dBm)

This section will show the specific layout design guidelines for these applications. Additionally, a few layout practices will be provided in a separate section when targeting antenna diversity applications.

3.2.5.1 Layout Design Guidelines for QFN Packages for Low-Power Applications (≤10 dBm)

- It is strongly recommended to keep a close distance between the C1 capacitor and the RF2G4_IO TX/RX pin of the EFR32xG24/26 IC.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Connect the nearby shunt capacitors in the matching network to the opposite side of the transmission line for the EFR32xG24/26 device.
- All shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pins to the common ground metal on the Top Layer should also be avoided in order to get optimal harmonic performance.
- **Do not** connect the ground pin of the first matching capacitor to the RFVSS ground pin of the chip.
- To achieve better harmonic performance, it is also recommended to connect RFVSS directly to the exposed pad ground and not to connect it to the common top layer ground.
- Route the PAVDD trace as **close** to the RF trace as possible. Consequently, the PAVDD filtering network should also be close to both the RF trace and the PAVDD pin, and it should comprise of two shunt capacitors (120pF + 1uF) and a series ferrite.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 39 mils.

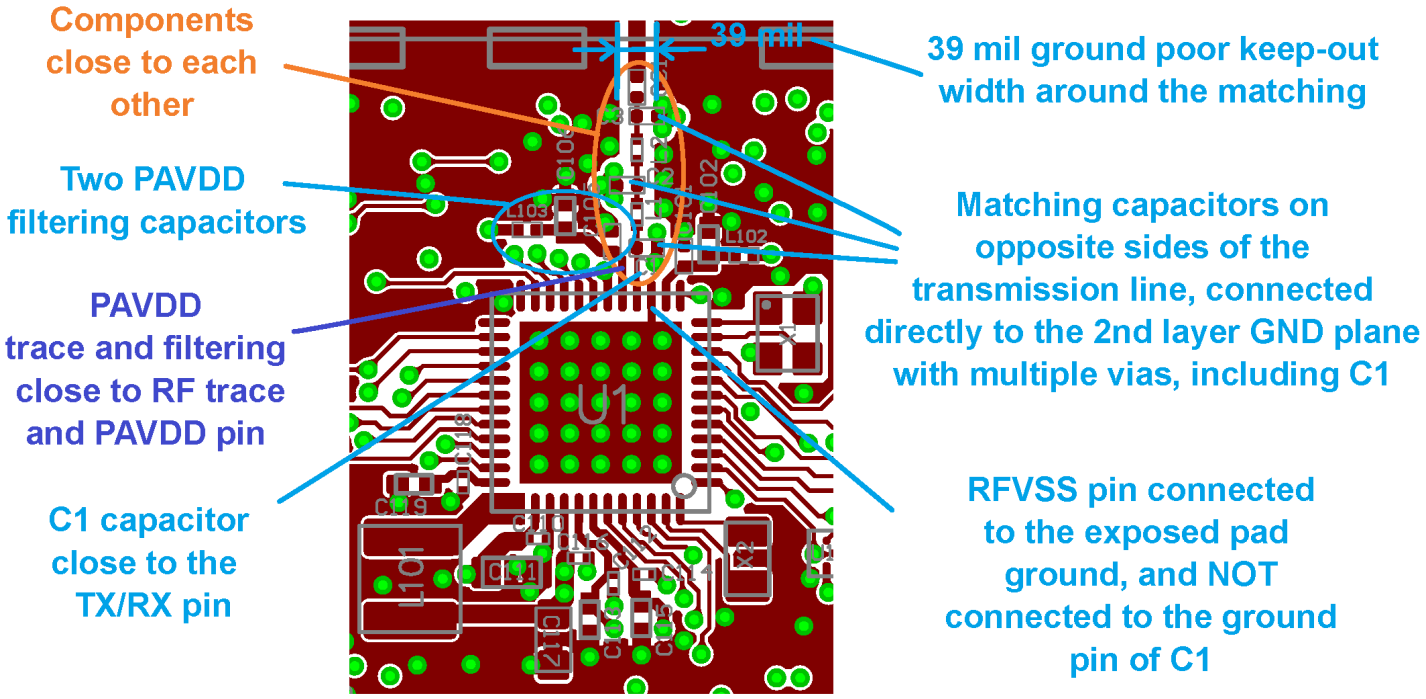


Figure 3.25. Matching Network Layout Guidelines on BRD4186C Radio Board (Top Layer)

3.2.5.2 Layout Design Guidelines for QFN Packages for High-Power Applications (>10 dBm)

- It is strongly recommended to keep a close distance between the C1 capacitor and the RF2G4_IO TX/RX pin of the EFR32xG24/26 IC.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Connect the nearby shunt capacitors in the matching network to the opposite side of the transmission line for the EFR32xG24/26 device.
- All shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pins to the common ground metal on the Top Layer should also be avoided in order to get optimal harmonic performance.
- **Connect** the ground pin of the first matching capacitor to the RFVSS ground pin of the chip.
- To achieve better harmonic performance, it is also recommended to connect RFVSS directly to the exposed pad ground directly and not to connect it to the common top layer ground.
- Route the PAVDD trace **further away** from the RF trace for ideal harmonic suppression. Consequently, the PAVDD filtering network should also be further away from both the RF trace and the PAVDD pin, and it should comprise of three shunt capacitors (0.5pF + 18pF + 1uF) and a series ferrite.
- The total copper keep-out on the component-layer GND pour around the RF matching circuit should be about 39 mils.

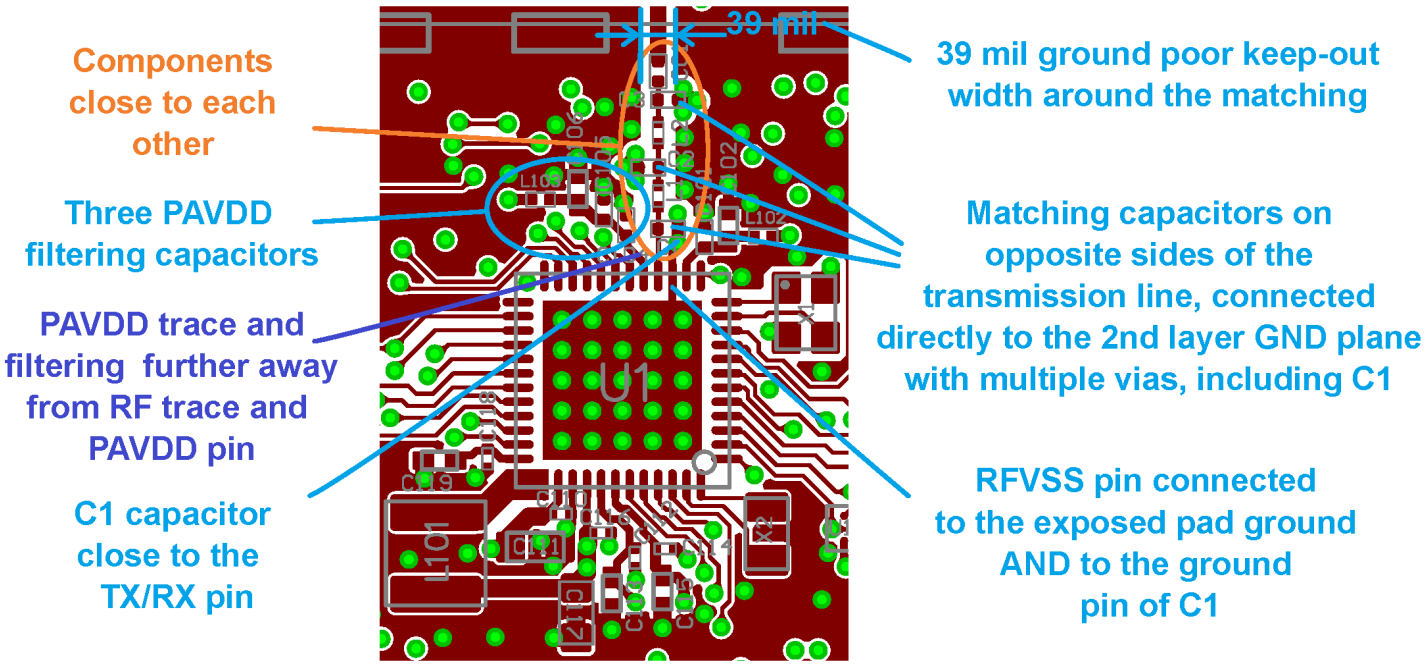


Figure 3.26. Matching Network Layout Guidelines on BRD4187C Radio Board (Top Layer)

3.2.5.3 Additional Layout Design Guidelines for WLCSP Package (xG24)

- It is strongly recommended to keep ~1.5 mm distance between the L1 inductor and the corresponding RF2G4_IO pin of the EFR32xG24 IC. The additional parasitic inductance of this short trace is part of the matching network; increased harmonic levels can be expected if not kept precisely.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Rotate the shunt capacitor of the matching network to the RFVDD side of the transmission line.
- The shunt capacitor in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pin to the common ground metal on the top layer should be avoided to get optimal harmonic performance.
- Use at least 0.3 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.
- Add ground copper between the matching network and the RFVDD filtering section.
- Due to the pin positions of the WLCSP package, some of the pins must be routed to the first inner layer using microvias. Make sure that these traces on the first inner layer are as short as possible to have a unique equal ground layer beneath the top layer as much as possible.

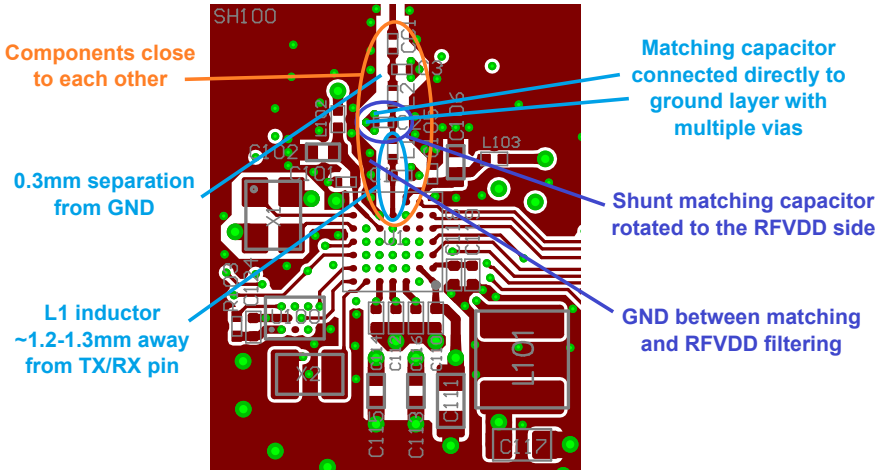


Figure 3.27. Matching Network Layout Guidelines on BRD4115B (Top Layer)

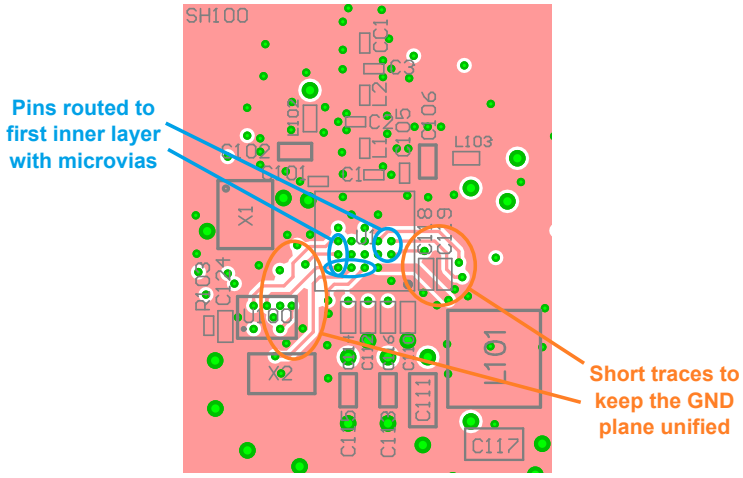


Figure 3.28. Inner Layer Trace Routing Recommendations on BRD4115B (Inner Layer 1)

3.2.5.4 Additional Layout Design Guidelines for Antenna Diversity Applications

The layout design guidelines specific to the selected transmit power for EFR32xG24 are described in the previous sections.

Besides the matching network related layout practices, an antenna diversity application requires additional considerations:

- Place the SMA antenna connectors at minimum λ/4 distance from each other.
- Place dc-blocking capacitors at all ports of the RF switch to protect it from DC signals.
- Arrange the external antennas (e.g., monopoles) orthogonally to each other to allow for two orthogonal antenna polarizations.
- Use 50 ohm lines to connect the matching network, switch and SMA connectors.

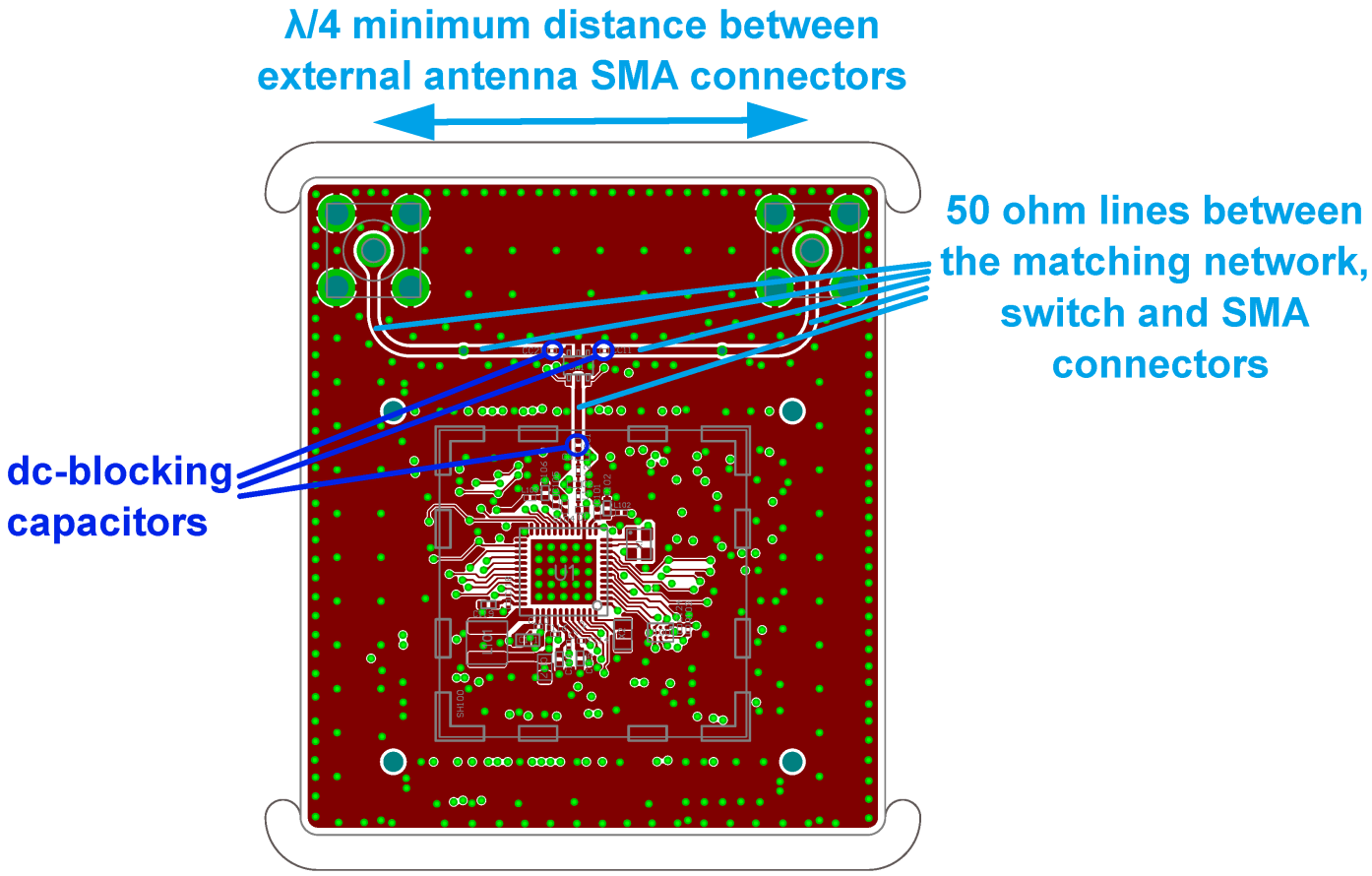


Figure 3.29. Antenna Diversity Layout Guidelines on BRD4188B Antenna Diversity Radio Board (Top Layer)

Note: Antenna diversity is not supported for EFR32xG26.

3.2.5.5 Additional Layout Design Guidelines for the BGA Package (xG26)

- It is strongly recommended to keep a close distance between the C1 capacitor and the RF2G4_IO TX/RX pin of the EFR32xG26 IC.
- Place the neighboring matching network components as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Directly connect the shunt capacitors in the matching network to PCB Layer 2 ground plane using multiple ground vias. Additionally, connect the first capacitor to the closest GND pin of the IC.
- Rotate the first matching capacitor to the RFVDD side of the PCB and connect its GND pad directly to the inner layers through multiple vias and also to the closest GND pad of the IC.
- Use at least 0.3 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

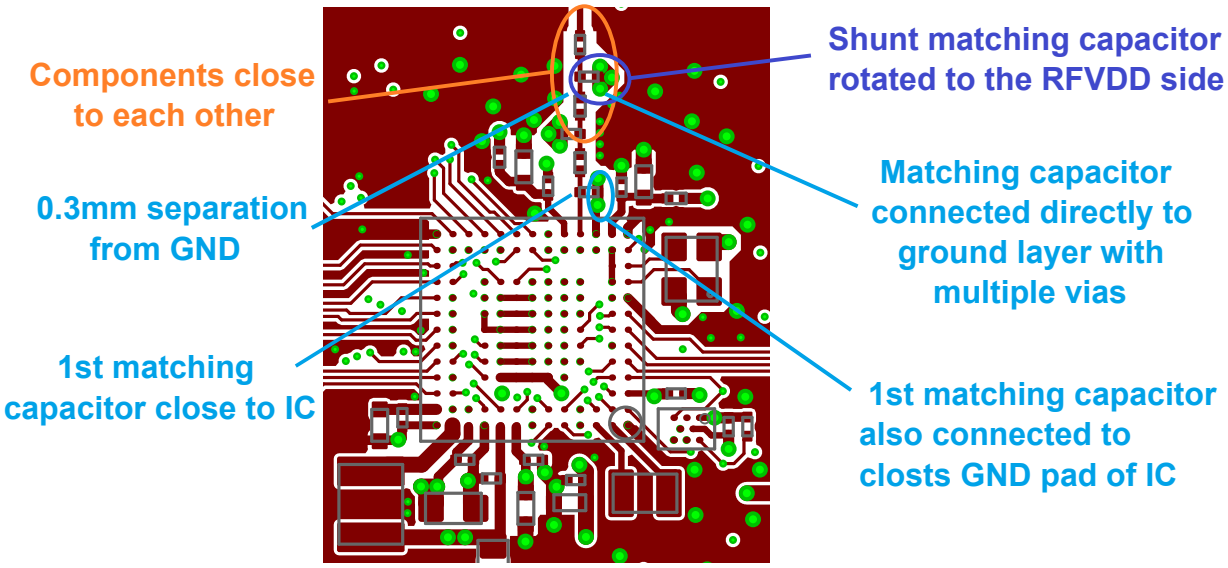


Figure 3.30. Matching Network Layout Guidelines on BRD4118A Radio Board (Top Layer)

3.2.6 Additional Layout Design Guidelines for the EFR32xG25 Matching Networks

As discussed in section 2.5 Matching Network Types for the EFR32xG25 Wireless MCU, two different approaches are available when designing matching network for EFR32xG25, as follows:

- Layout for the matching network structure using an external ceramic balun
- Layout for the full discrete matching network structure

This section will show the specific layout design guidelines for these different structures.

3.2.6.1 Matching Network Structure using an External Ceramic Balun

- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- The balanced TX matching network must be perfectly symmetrical as any asymmetry could deteriorate the necessary 180° phase shift between the signals of the differential TX pins.
- All shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane. Connecting the ground pins to the common ground metal on the Top Layer should also be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect PAVSS and RFVSS directly to the exposed pad ground and not to connect it to the common top layer ground.
- The thermistor GND pad should be directly connected to the XO crystal GND pad (with no connection to the Top layer GND pour) in order to properly sense the crystal temperature.
- Copy the RX matching structure as is: the additional traces that connect the RX matching inductor to the SUBG_I pin and to the common direct-tie point of the matching network can be considered as parasitic inductance and these traces are playing a part in the matching network. These additional traces should also be applied when using a matching network type other than direct-tie type (e.g., matching network with RF switch or FEM). If different trace lengths are used, the RX matching network can be detuned from its optimal form and additional tuning might be required. The effect of these traces is significant in high-band, sub-GHz frequencies (868/915 MHz), while the effect is less remarkable below 500 MHz.
- Use at least 0.6 mm separation between traces/pads to the adjacent ground pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

Note: Silicon Labs provides a common layout for the 868, 915, and 920 MHz bands.

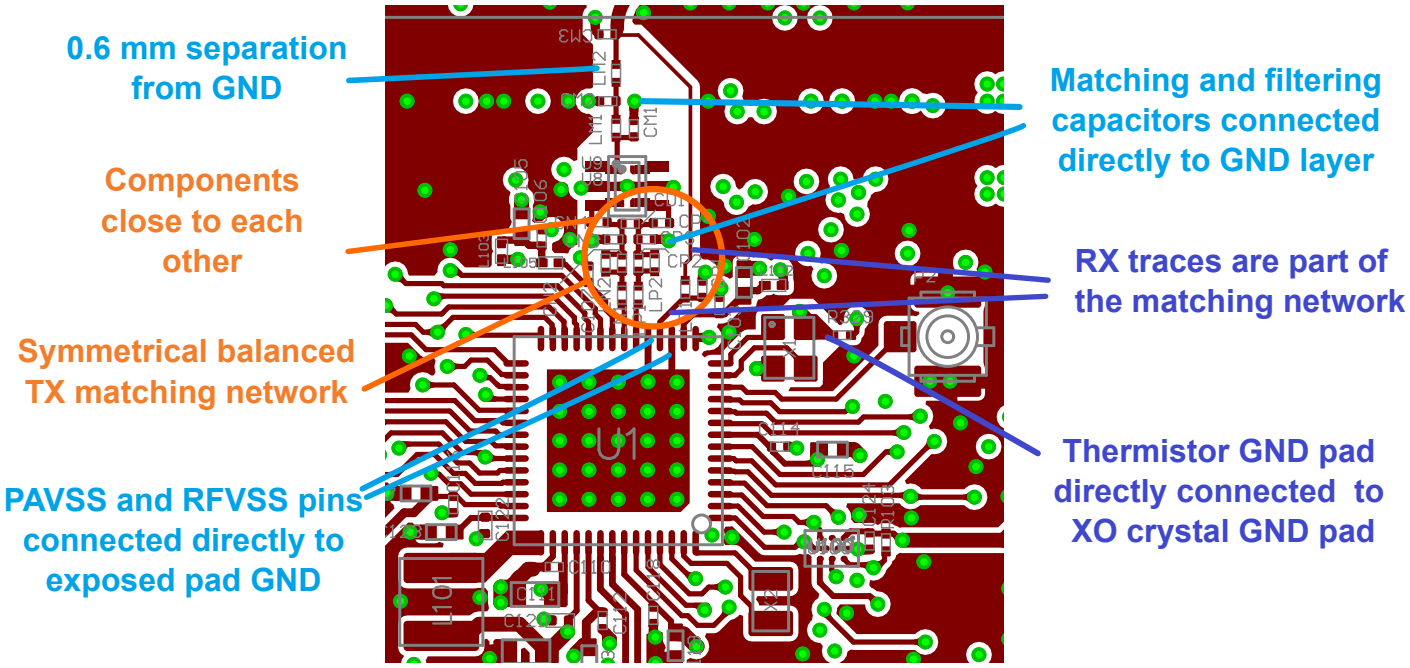


Figure 3.31. Matching Network Layout Guidelines on the BRD4270B Radio Board with an External Ceramic Balun (Top Layer)

3.2.6.2 Full Discrete Matching Network Structure

- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- All shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane. Connecting the ground pins to the common ground metal on the Top Layer should also be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect PAVSS and RFVSS directly to the exposed pad ground and not to connect it to the common top layer ground.
- The thermistor GND pad should be directly connected to the XO crystal GND pad (with no connection to the Top layer GND pour) to be able to properly sense the crystal temperature.
- Copy the RX matching structure as is: the additional traces that connect the RX matching inductor to the SUBG_I pin and to the common direct-tie point of the matching network can be considered as parasitic inductance and these traces are playing a part in the matching network. These additional traces should also be applied when using a matching network type other than direct-tie type (e.g., matching network with RF switch or FEM). If different trace lengths are used, the RX matching network can be detuned from its optimal form and additional tuning might be required. The effect of these traces is significant in high-band, sub-GHz frequencies (868/915 MHz), while the effect is less remarkable below 500 MHz.

Note: While the matching structures are similar for the 868, 915, and 920 MHz bands, it is slightly different for the 470 MHz band as can be seen from the layout figures below. Both radio boards are shown in the two figures below.

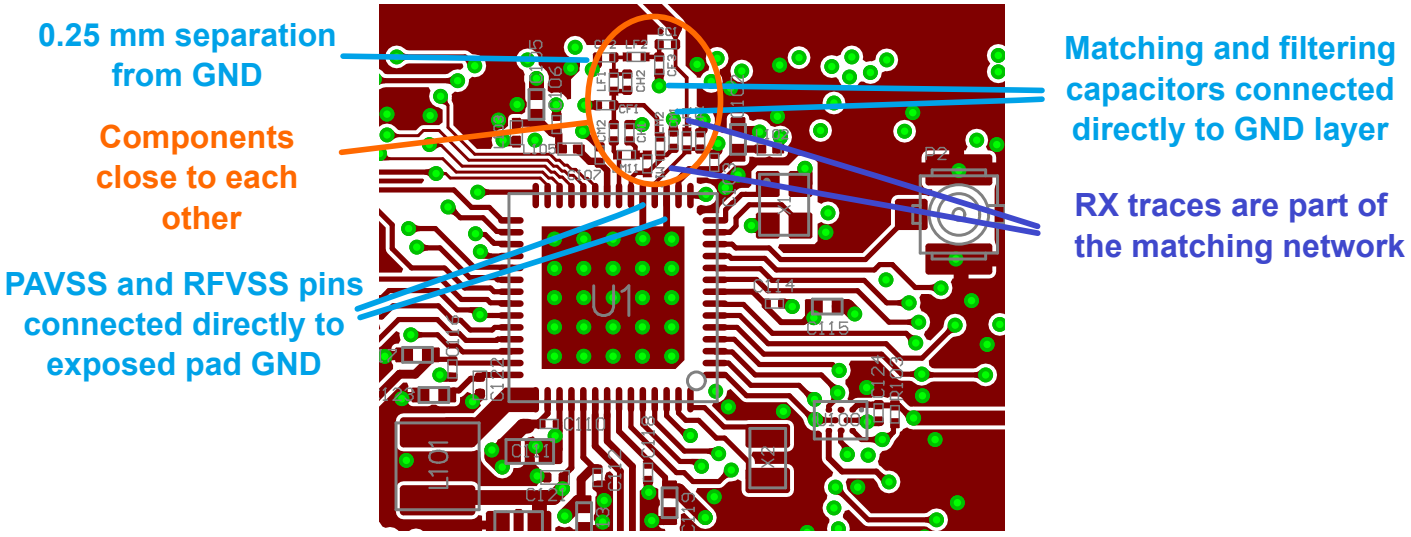


Figure 3.32. Matching Network Layout Guidelines on the 868, 915, and 920 MHz Band Full Discrete Match Prototype Radio Board (Top Layer)

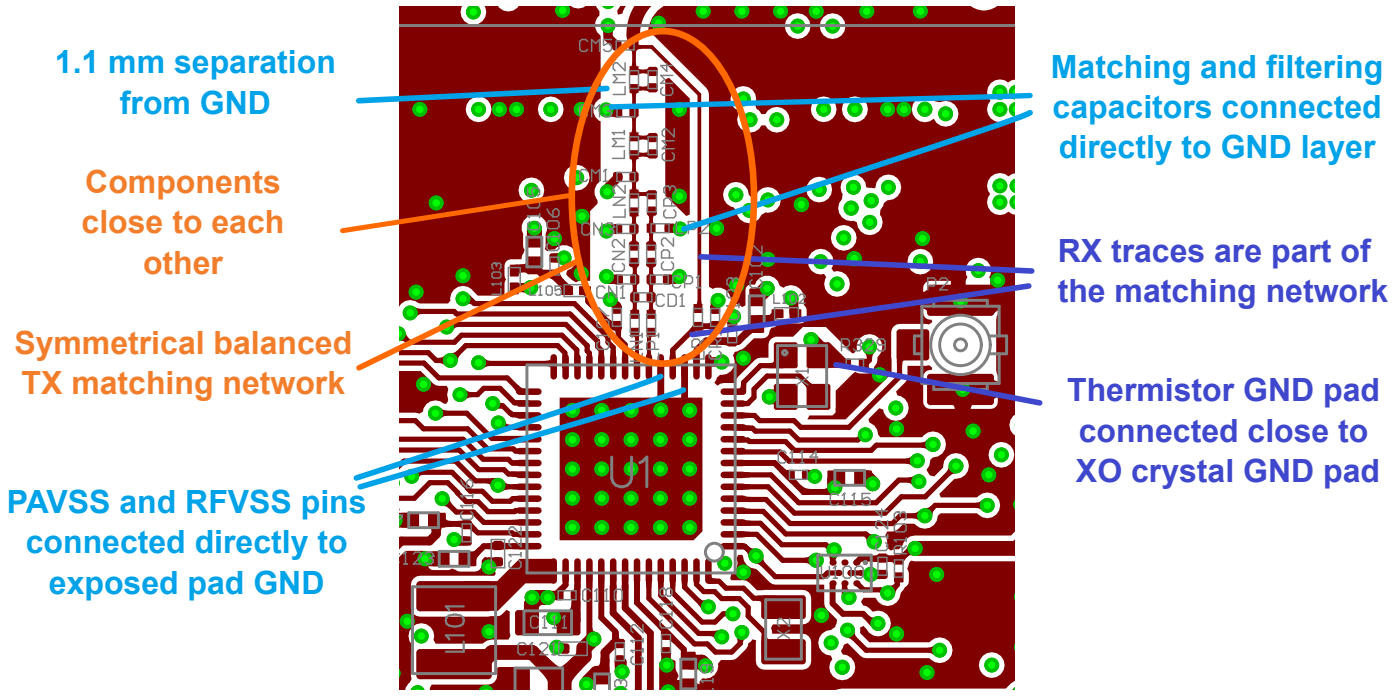


Figure 3.33. Matching Network Layout Guidelines on the 470 MHz Band Full Discrete Match BRD4272A Radio Board (Top Layer)

3.2.7 Additional Layout Design Guidelines for the EFR32xG27/29 Matching Networks

As discussed in 2.6 Matching Network Types for the EFR32xG27/29 Wireless MCU, EFR32xG27/29 matching networks are equally optimized for the 0 dBm and high-power PA, and both the buck and boost dc-dc converter variants require the same matching work. However, the optimal matching network component values and PCB layout guidelines are different for the QFN and WLCSP package types.

This section will show the specific layout design guidelines for both package types.

3.2.7.1 Layout Design Guidelines When Using the QFN Package Types

- It is strongly recommended to keep ~1.2-1.3 mm distance between the L1 inductor and the corresponding the RF2G4_IO pin of the EFR32xG27/29 IC (on the BRD4194A Radio Board, this distance is 1.28 mm). The additional parasitic inductance of this short trace is part of the matching network; increased harmonic levels can be expected if not kept precisely.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Rotate the shunt capacitor of the matching network to the RFVDD side of the transmission line.
- The shunt capacitor in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pin to the common ground metal on the top layer should be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect pin 13 (RFVSS) to the exposed pad ground directly and not to connect it to the common top layer ground.
- Use at least 0.3 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

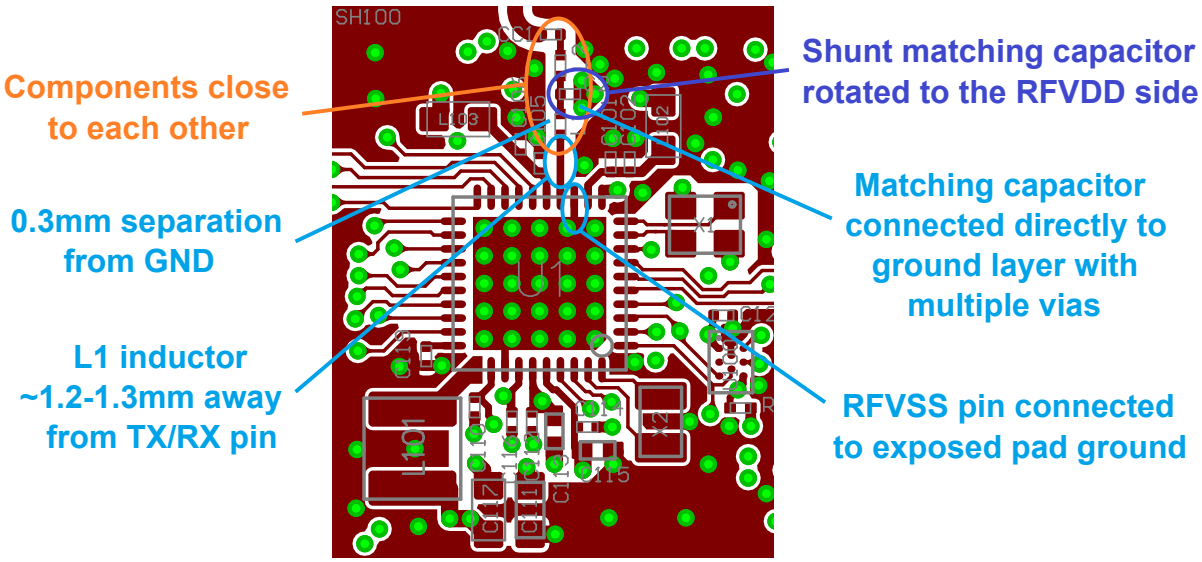


Figure 3.34. Matching Network Layout Guidelines on BRD4194A or BRD4412A Radio Board (Top Layer)

3.2.7.2 Layout Design Guidelines When Using the WLCSP Package Type

- It is strongly recommended to keep a close distance between the L1 inductor and the RF2G4_IO TX/RX pin of the EFR32xG27/29 IC.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Rotate the shunt capacitor of the matching network to the PAVDD side of the transmission line.
- The shunt capacitor in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias. Connecting the ground pin to the common ground metal on the top layer should be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is recommended to connect ground pins of the EFR32xG27/29 chip with each other and to the internal ground layer.
- Due to the pin positions of the WLCSP package, some of the pins must be routed to the first inner layer using microvias. Make sure that these traces on the first inner layer are as short as possible to have a unique equal ground layer beneath the top layer as much as possible.
- Use at least 0.3 mm separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.

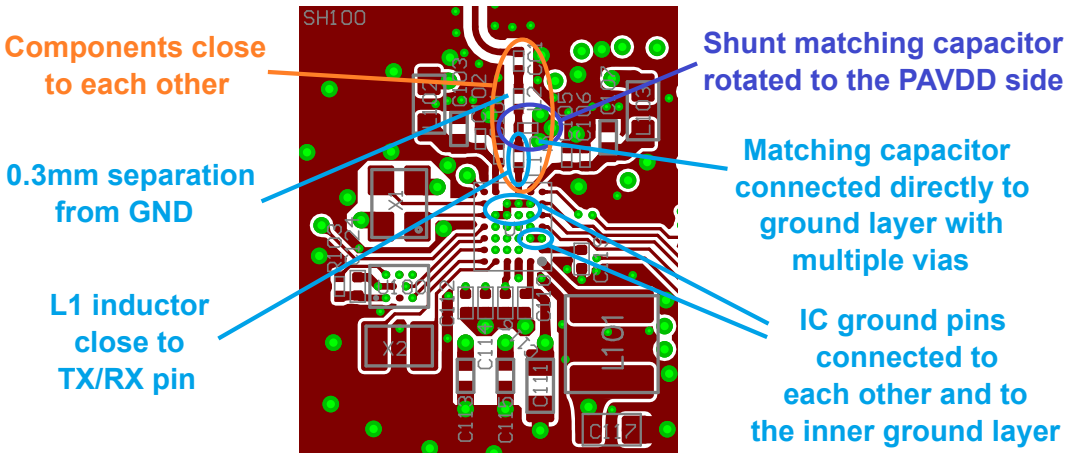


Figure 3.35. Matching Network Layout Guidelines on BRD4110B Radio Board (Top Layer)

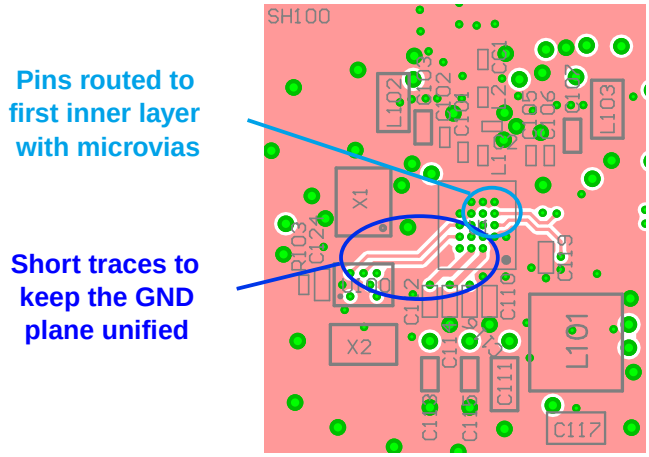


Figure 3.36. Inner Layer Trace Routing Recommendations on BRD4110B Radio Board (Inner Layer 1)

Note: The EFR32xG27 WLCSP package has 39 pins and the EFR32xG29 WLCSP package has 45 pins. The WLCSP layout guidelines presented above are shown for EFR32xG27, but the same rules apply for both devices.

3.2.8 Additional Layout Design Guidelines for the EFR32xG28 Matching Networks

- It is strongly recommended to keep a close distance between the L1 and L4 inductors and the corresponding the RF pins of the EFR32xG28 IC. The additional parasitic inductance of these short traces are part of the matching networks; increased harmonic levels can be expected if not kept precisely.
- The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- The shunt capacitors in the matching network should be connected directly to PCB Layer 2 ground plane using multiple ground vias.
- Connecting the ground pin to the common ground metal on the top layer should be avoided to get optimal harmonic performance.
- To achieve better harmonic performance, it is also recommended to connect to RFVSS pin to the exposed pad ground directly and not to connect it to the common top layer ground.
- Use a large copper keep-out and separation between traces/pads to the adjacent GND pour in the area of the matching network. This technique will minimize the parasitic capacitance and reduce the detuning effects.
- Route the RX trace (that crosses the TX path of the other RF port) under the dc-blocking capacitor of the TX path. Choose a larger, 0402 size component to make the routing possible.

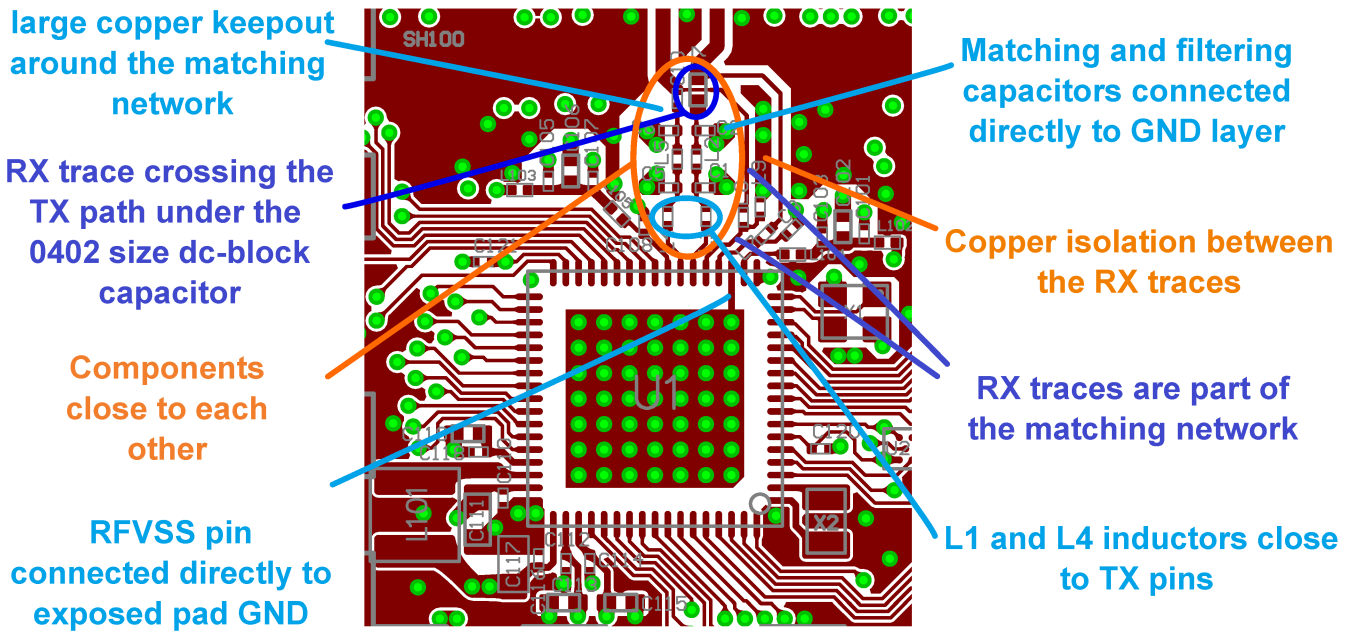
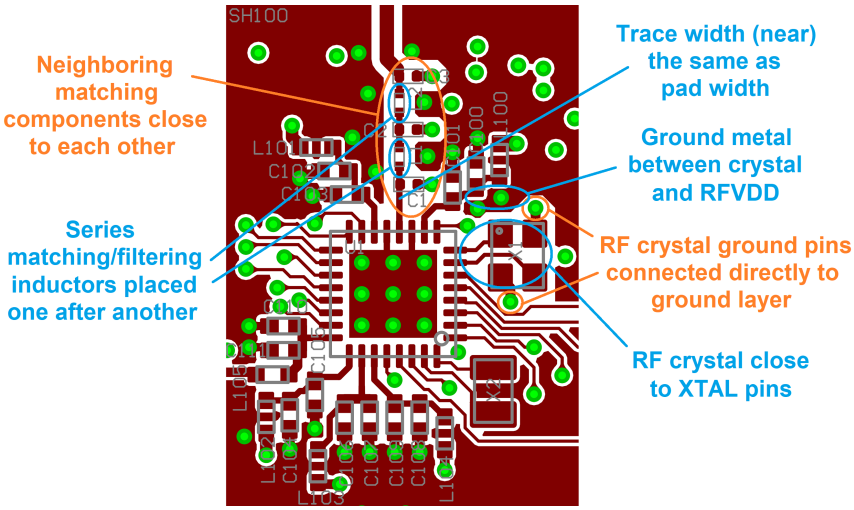
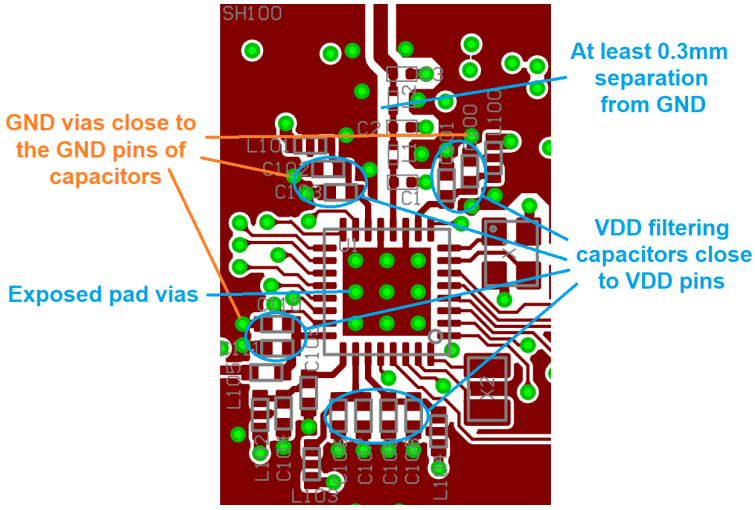
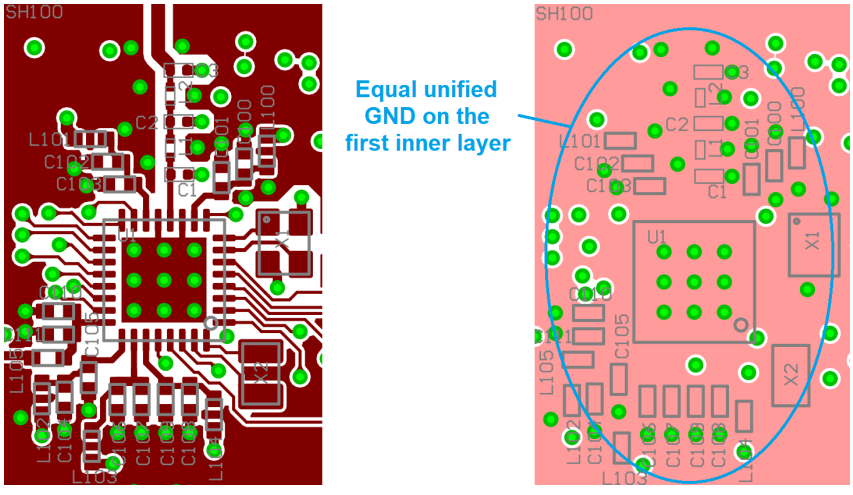


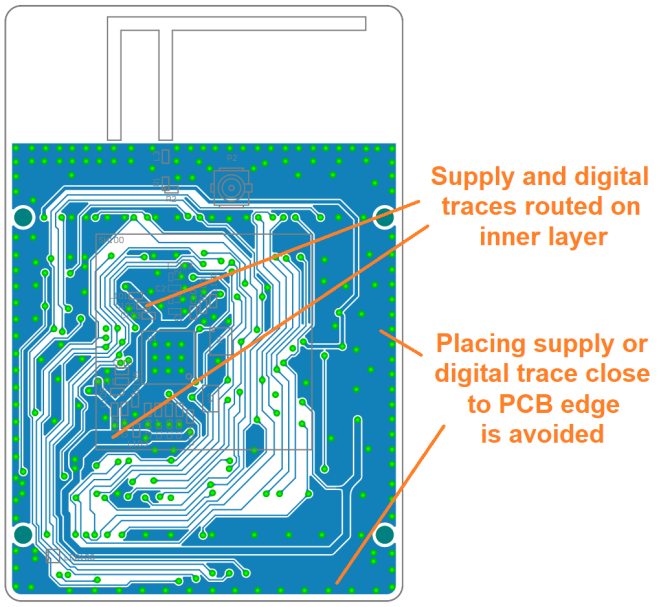
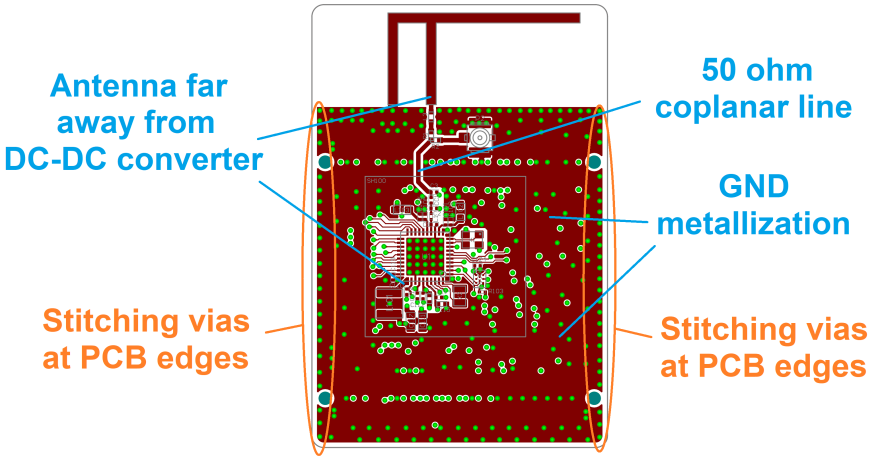
Figure 3.37. Matching Network Guidelines on BRD4400C Radio Board (Top Layer)

Note: EFR32xG28 is available in both QFN68 and QFN40 packages. Additionally, there are Sub-GHz/2.4 GHz and Sub-GHz/Sub-GHz versions of the device. The layout guidelines in this application note apply to all four package variants.

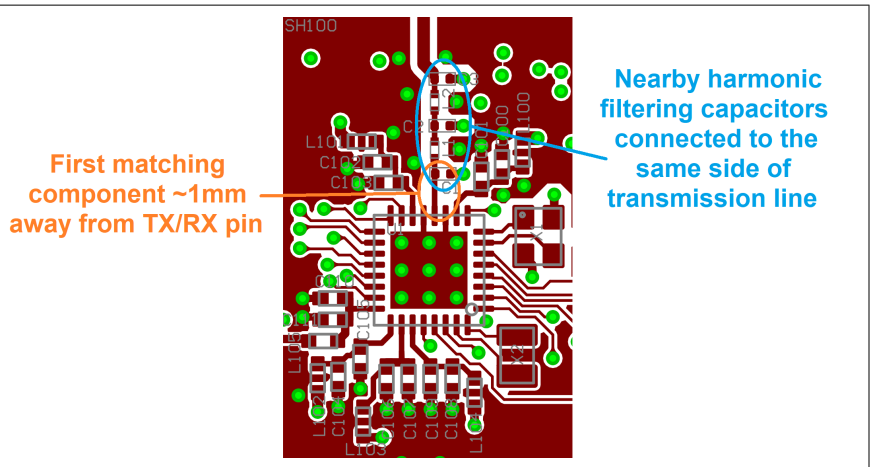
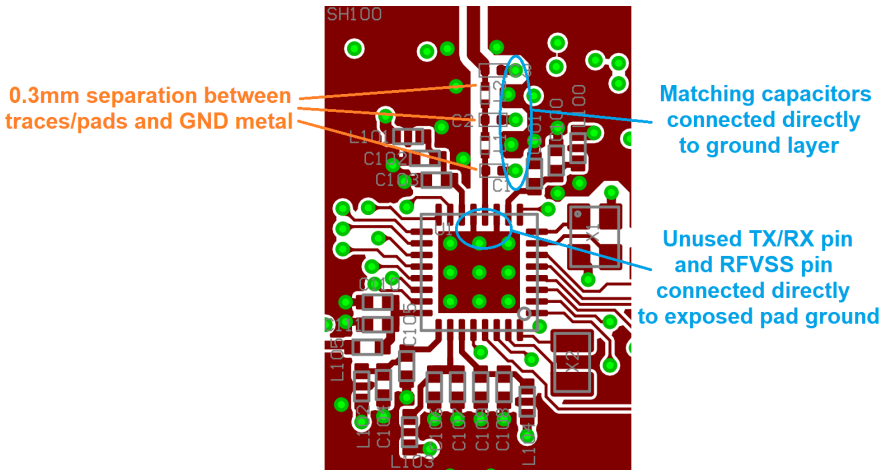
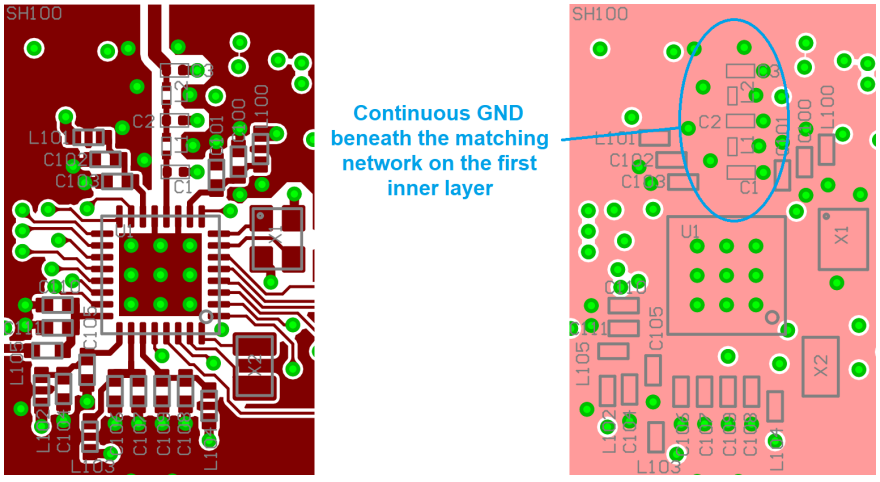
4. Checklists

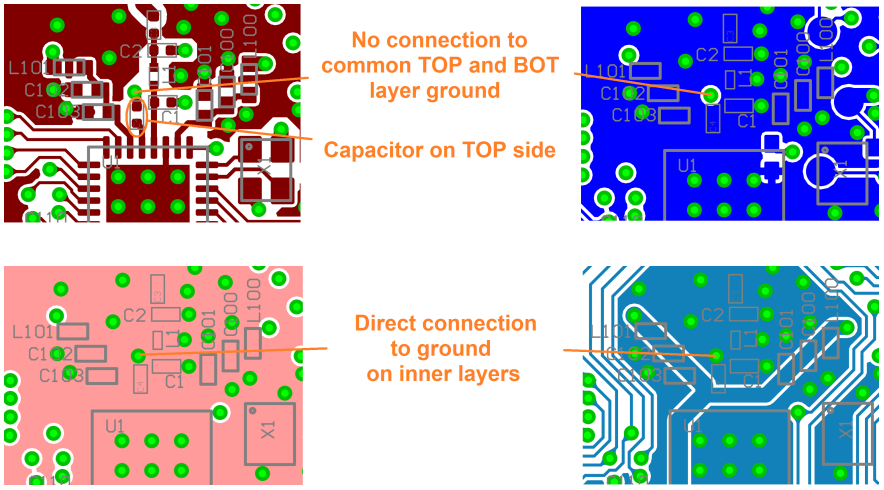
4.1 Main Layout Design Principles

1.	Is the number of PCB layers the same as in the reference design? Or at a minimum, is the distance between the top and first inner layers similar?	
2.	Are the neighboring matching network components as close to each other as possible?	
3.	Is the trace width (near) the same as pad width for connecting nearby components?	
4.	Are the series matching / filtering inductors placed one after another or perpendicular to each other?	
5.	Is the RF crystal as close to the XTAL pins of the EFR32 IC as possible?	
6.	Does ground metal exist between the crystal and the RFVDD feed?	
7.	Are the smallest value VDD filtering capacitors kept as close as possible to the VDD pins (RFVDD, PAVDD, AVDD, DVDD, IOVDD) of the EFR32?	
8.	Do the ground pins of the shunt capacitors use multiple vias close to these pins?	
9.	Does the exposed pad footprint use multiple vias?	
10.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
11.	Is wiring and routing avoided on (basically) the first inner (GND) layer between the grounding vias of VDD filtering capacitors and the exposed pad of the EFR32 IC?	

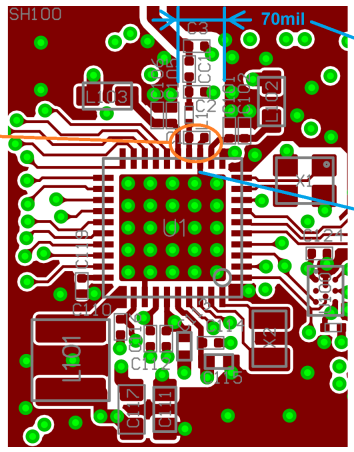
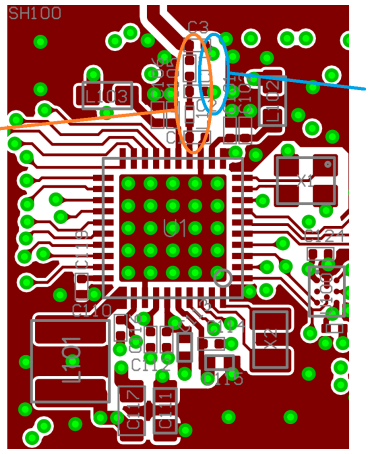
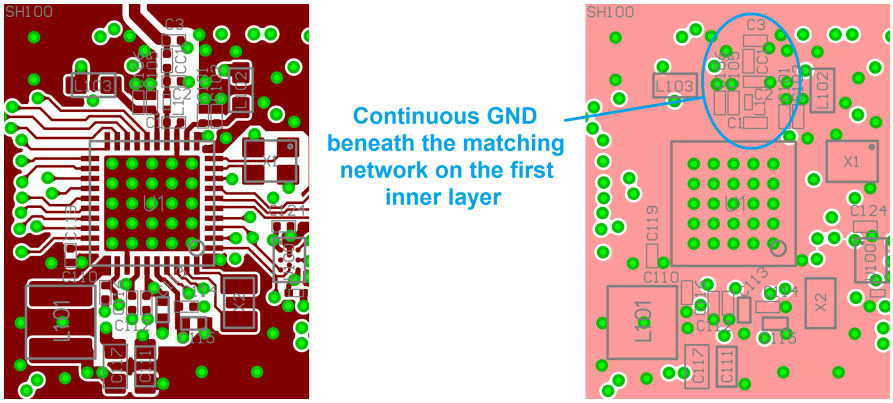
12.	Are supply and digital traces routed on inner layers? Or at a minimum, are the supply lines surrounded by ground metal with many GND vias if routed on the top or the bottom layers?	
13.	Is placing supply or digital lines close to the PCB edge avoided?	
14.	Is large, continuous GND metallization added to at least the RF sections using as many GND vias as possible?	
15.	Are the GND metal edges closed by "stitching vias" where possible, with a via distance less than lambda/10 of the highest (usually 10th) critical harmonic frequency?	
16.	Are 50 Ω grounded coplanar lines used for RF traces longer than λ/16 at the fundamental frequency?	
17.	Are there vias at the ground metallization near the 50 Ω transmission lines?	
18.	Are the RF related parts (especially the antenna) placed far away from the dc-dc converter output and the related dc-dc components?	

4.2 Additional Concerns for the EFR32xG21 Matching Network

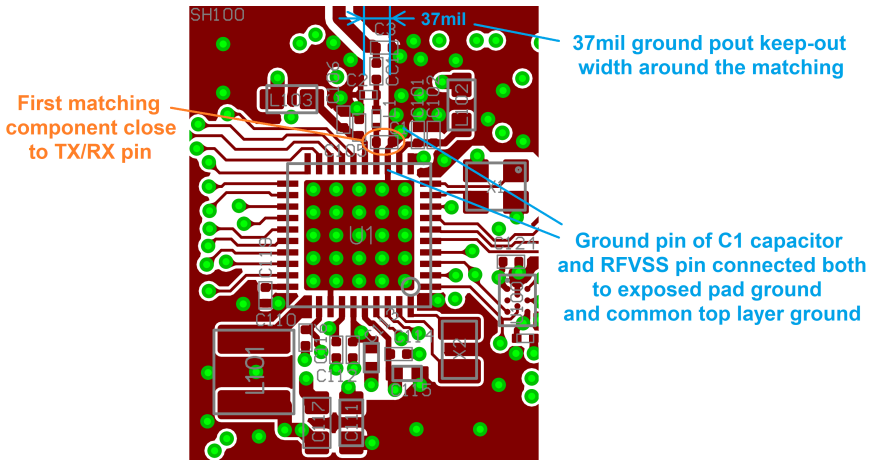
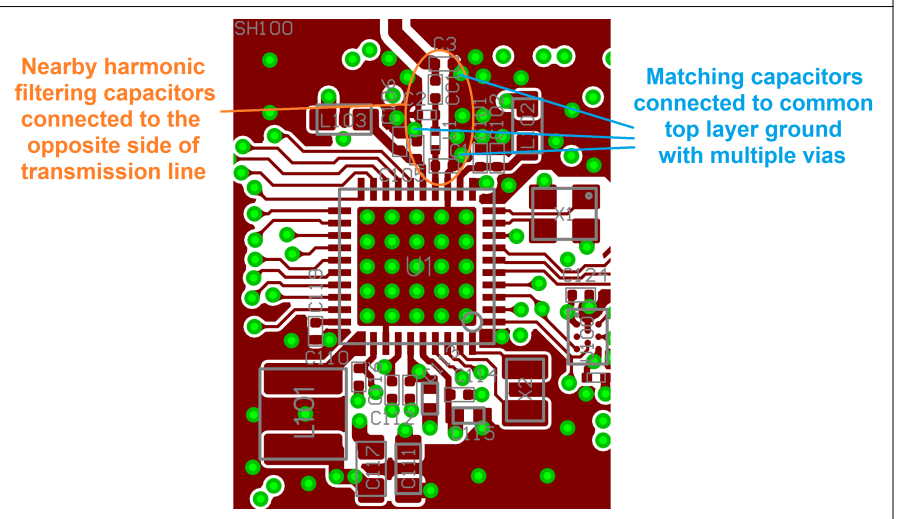
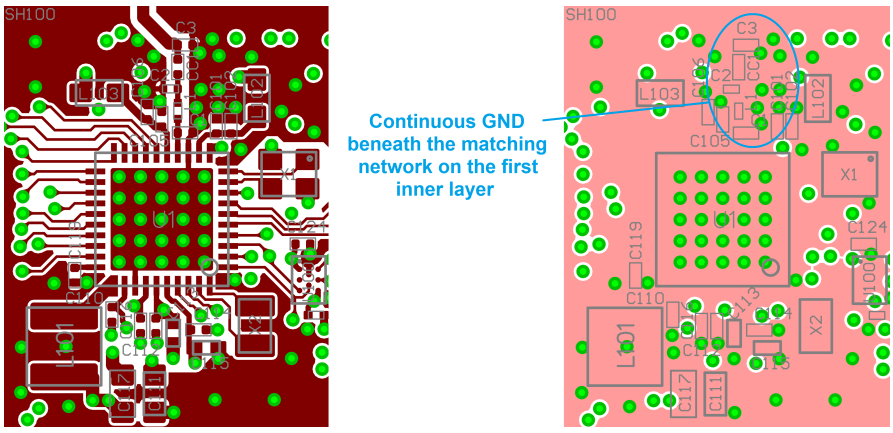
19.	Is the first matching network component (C1) placed ~1mm away from the corresponding TX/RX pin?	
20.	Are the nearby harmonic filtering capacitors connected to ground planes on the same sides of the transmission line?	
21.	Are shunt capacitors in the matching network connected directly to the first inner layer (common ground)? Is connecting the ground pins to the common ground metal on the Top Layer avoided?	
22.	Are the unused TX/RX pin and RFVSS pin connected directly to the exposed pad ground? Is connecting those to the common top layer ground avoided?	
23.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
24.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

25.	If using the 0 / 10 dBm combined matching network, is any of the two recommended capacitor placements followed?	TOP capacitor placement: 

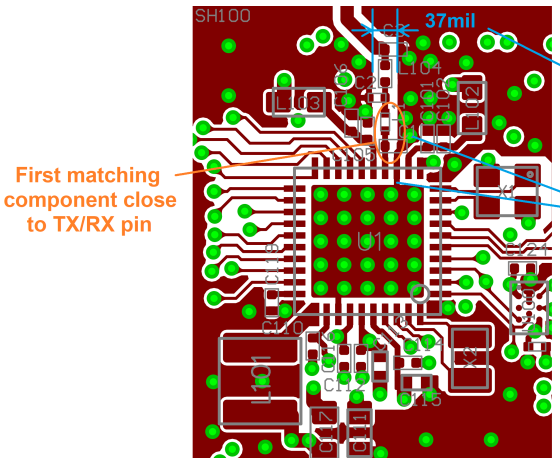
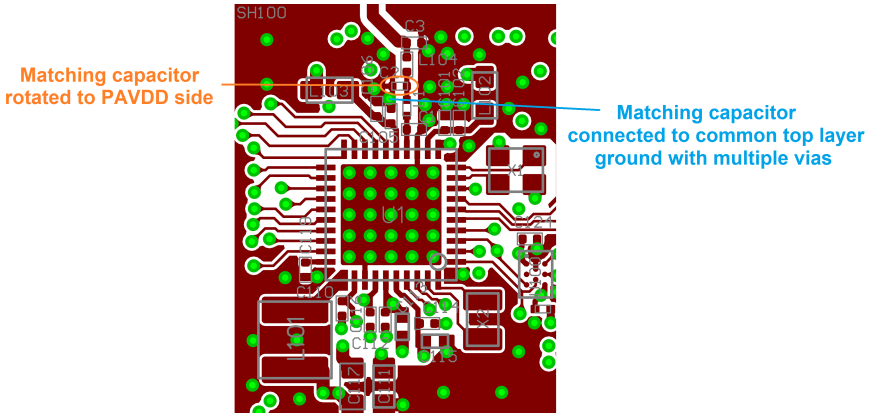
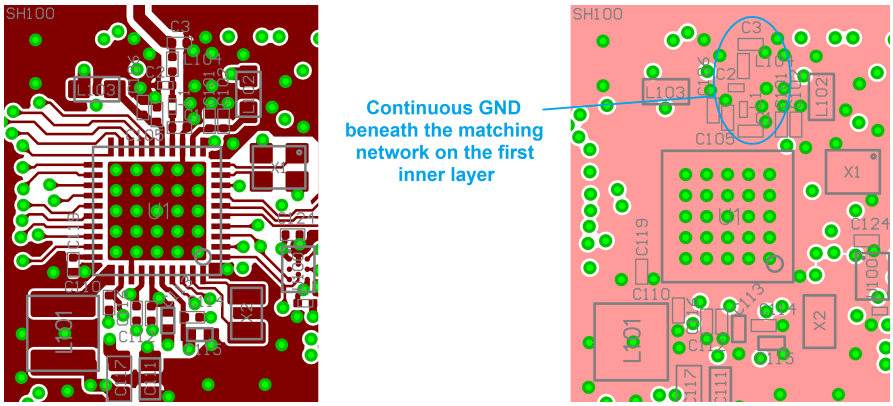
4.3 Additional Concerns for the EFR32xG22 Pi-Matching Network with Existing Layout Concept #1

26.	Is the first matching network component (C1) placed as close to the corresponding TX/RX pin as possible?	
27.	Are the ground pin of C1 capacitor and RFVSS pin of the EFR32 IC connected directly to the exposed pad ground? Is connecting those to the Inner layer ground or to the common Top layer ground avoided?	
28.	Is the recommended ~70 mil ground pour keep-out applied around the matching network area?	
29.	Are the nearby harmonic filtering capacitors connected to ground planes on the same sides of the transmission line?	
30.	Are shunt capacitors in the matching network (except for C1) connected directly to the first inner layer (common ground)? Is connecting the ground pins to the common ground metal on the Top Layer avoided?	
31.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

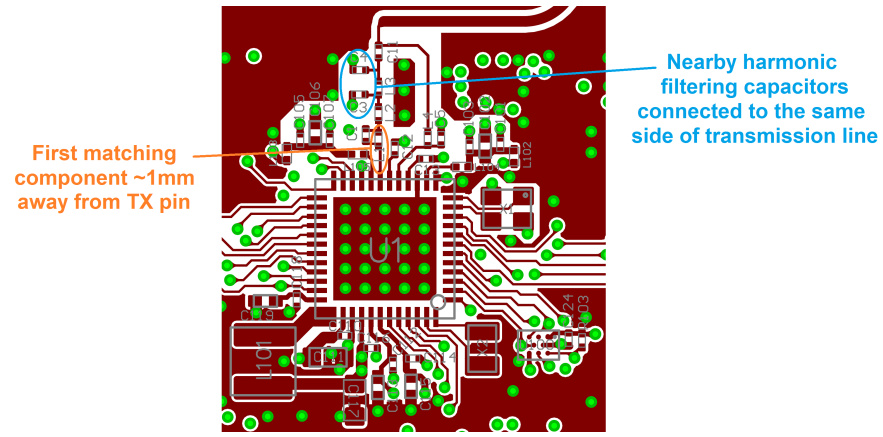
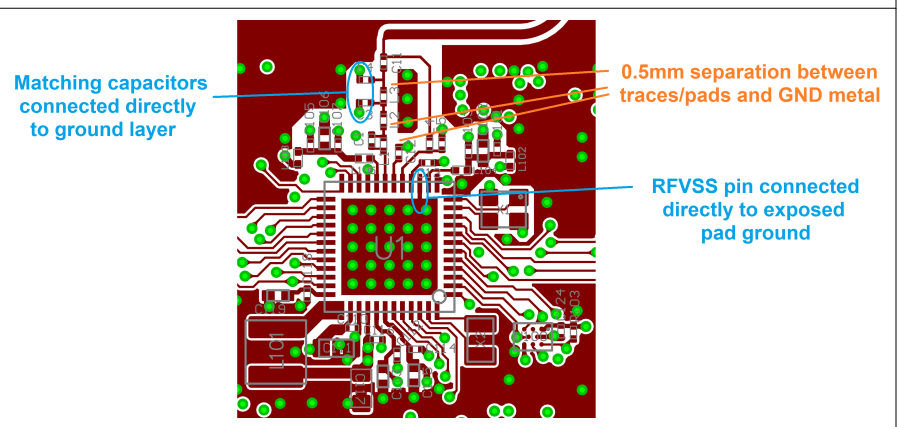
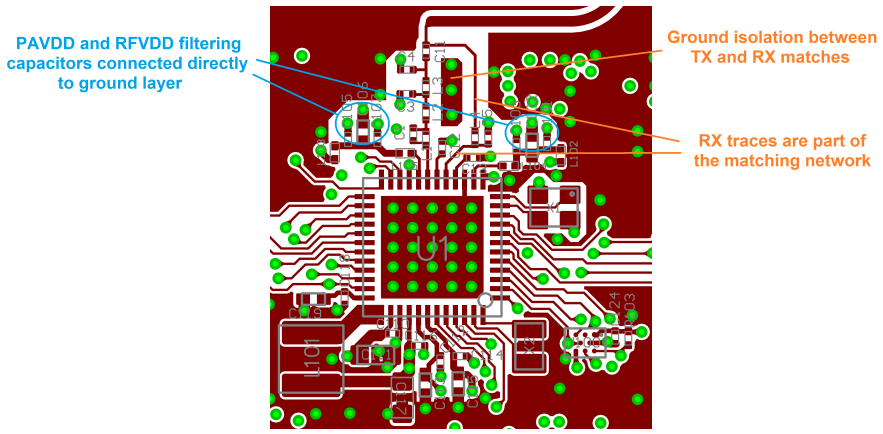
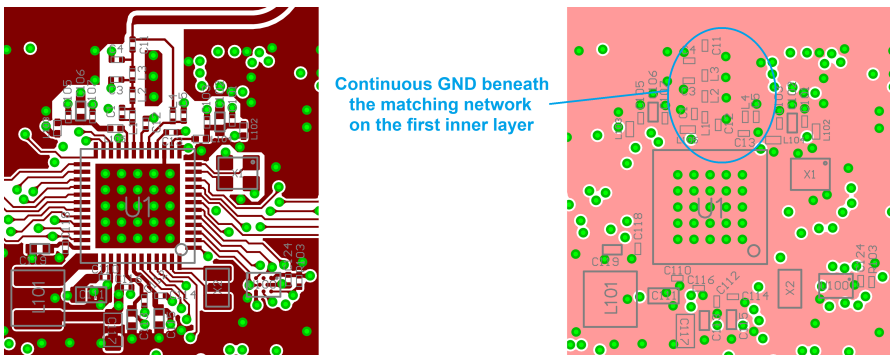
4.4 Additional Concerns for the EFR32xG22 Pi-Matching Network with Generic Layout Concept #2

32.	Is the first matching network component (C1) placed as close to the corresponding TX/RX pin as possible?	
33.	Are the ground pin of C1 capacitor and RFVSS pin of the EFR32 IC connected both to the exposed pad ground and to the common Top layer ground pour?	
34.	Is the recommended ~37 mil ground pour keep-out applied around the matching network area?	
35.	Are the nearby harmonic filtering capacitors connected to ground planes on the opposite sides of the transmission line?	
36.	Are the shunt capacitors in the matching network connected to the component-layer GND pour with multiple stitching vias?	
37.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

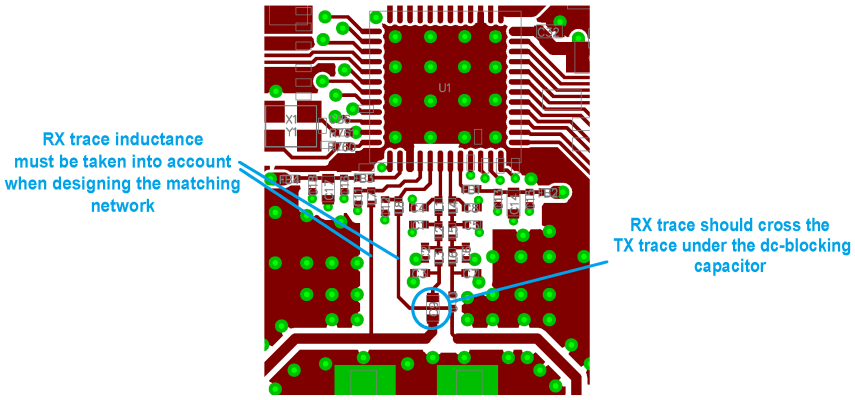
4.5 Additional Concerns for the EFR32xG22 T-Matching Network with Generic Layout Concept #2

38.	Is the first matching network component (C1/L1) placed as close to the corresponding TX/RX pin as possible?	
39.	Is the RFVSS pin connected to the Top layer ground pour with additional ground vias to internal ground layers?	
40.	Is the recommended ~37 mil ground pour keep-out applied around the matching network area?	
41.	Is the shunt matching network capacitor rotated to the PAVDD side of the transmission line?	
42.	Is the shunt matching network capacitor connected to the component-layer ground pour with multiple stitching vias?	
43.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

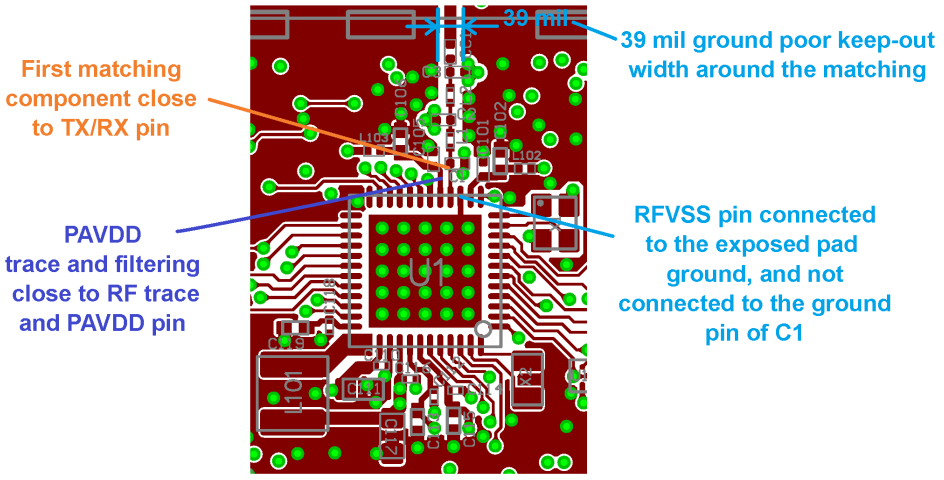
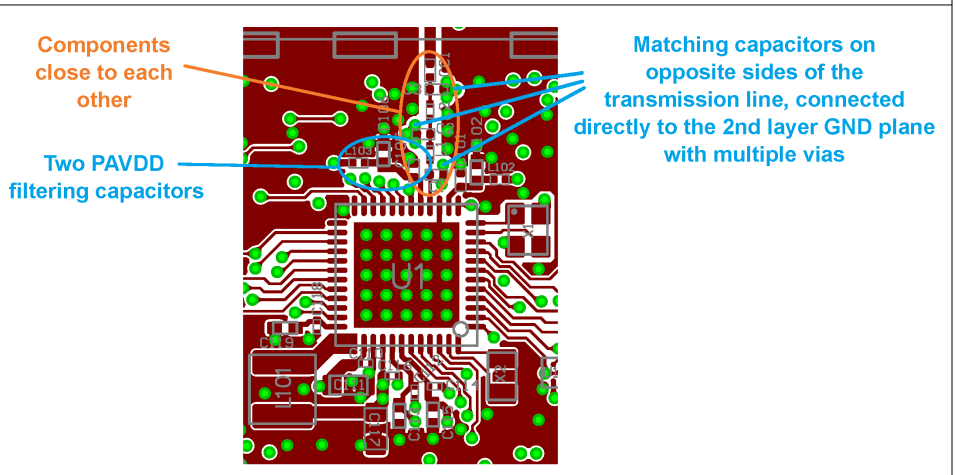
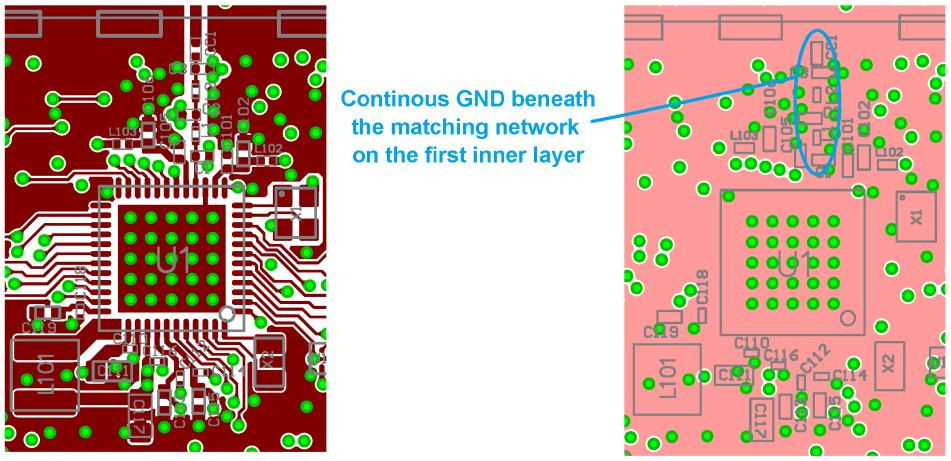
4.6 Additional Concerns for the EFR32xG23 Matching Network

44.	Is the first matching network component (L1) placed ~1 mm away from the corresponding TX pin?	
45.	Are the nearby harmonic filtering capacitors connected to ground planes on the same sides of the transmission line?	
46.	Are shunt capacitors in the matching network connected directly to the first inner layer (common ground)? Is connecting the ground pins to the common ground metal on the Top Layer avoided?	
47.	Is the RFVSS pin connected directly to the exposed pad ground? Is connecting this pin to the common top layer ground avoided?	
48.	Is there at least 0.5 mm separation in the matching between the traces/pads and the GND metal?	
49.	Is ground copper isolation added between TX and RX stages?	
50.	Are the additional traces applied for the RX matching network?	
51.	Are PAVDD and RFVDD filtering capacitors connected directly to the first inner layer (common ground)? Is connecting the ground pins of these capacitors to the common ground metal on the Top Layer avoided?	
52.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

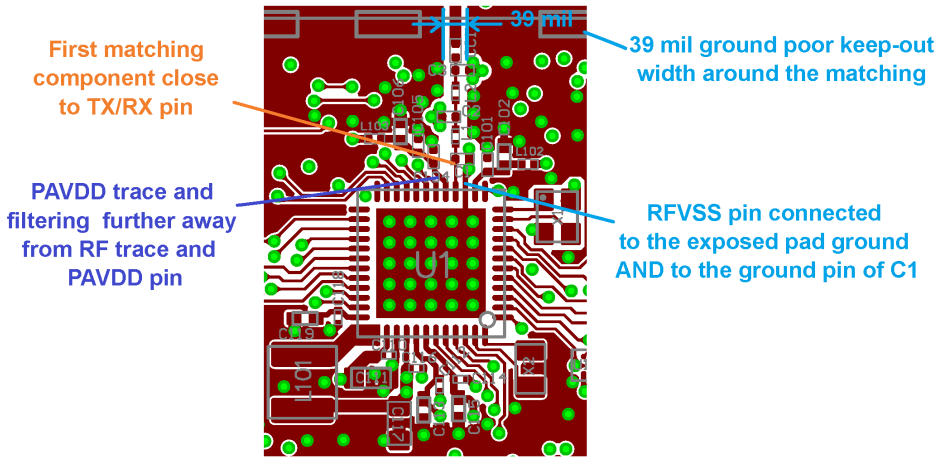
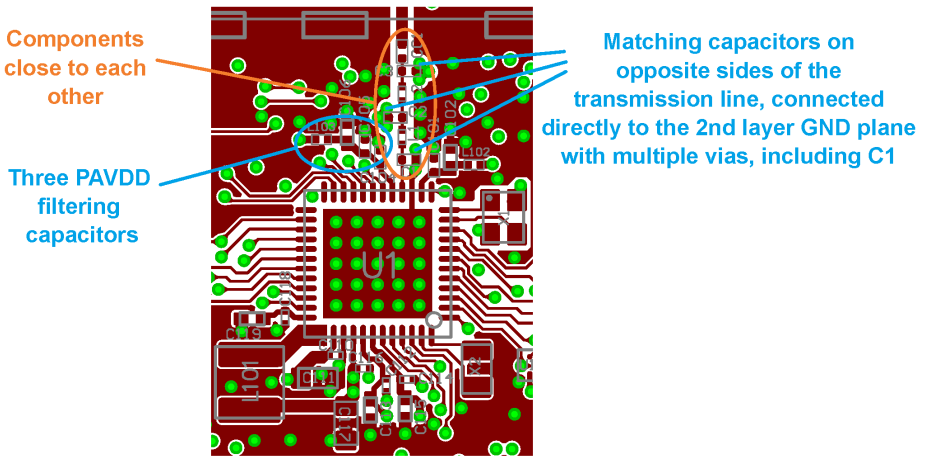
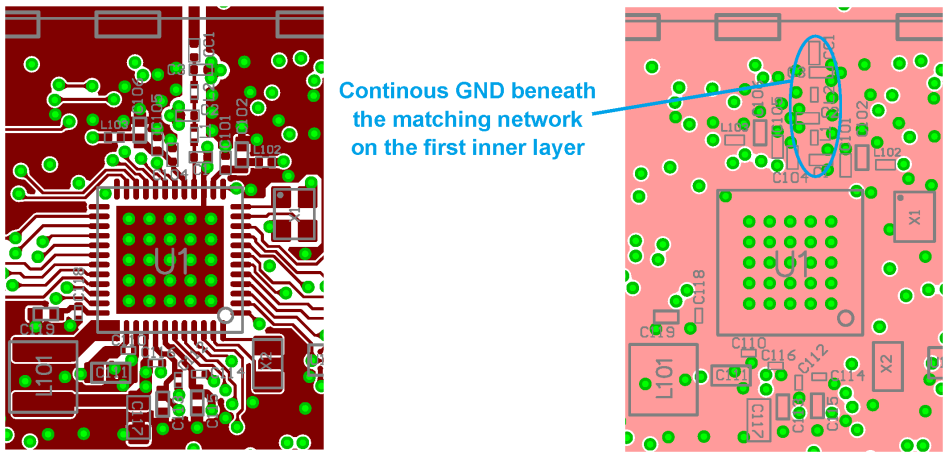
4.7 Additional Concerns for the EFR32xG23 Matching Network for 2 RF-Front End Use

53.	Does the trace of the SUBG_I0 RX pin cross the trace of the SUBG_O1 TX pin under the dc-blocking capacitor?	
54.	Are the inductances of the RX traces taken into account when designing the matching network?	

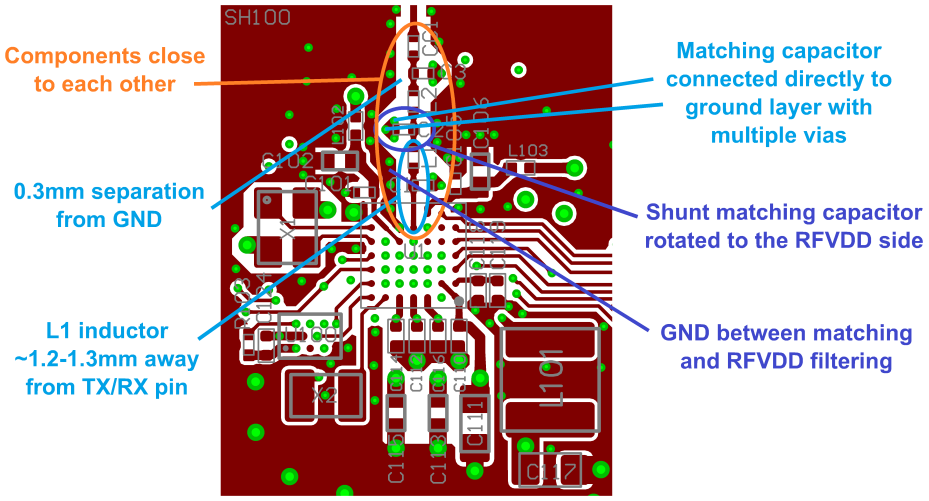
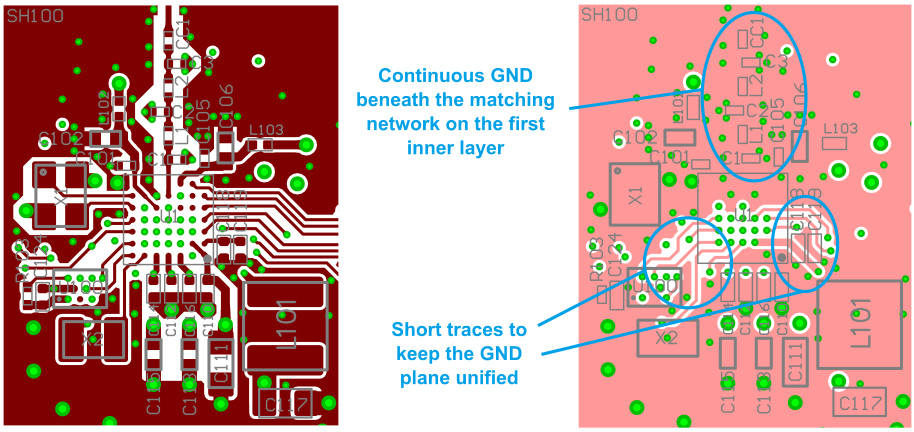
4.8 Additional Concerns for the EFR32xG24/26 Matching Network for Low-Power (≤10 dBm) Applications (QFN Package Variants)

55.	Is the first matching network component (C1) placed close to the TX/RX pin?	
56.	Is the recommended ~39 mil ground pour keep-out applied around the matching network area?	
57.	Is the PAVDD trace routed close to the RF trace? Is the PAVDD filtering network close to both the RF trace and the PAVDD pin?	
58.	Is the RFVSS pin connected to the exposed pad ground, and NOT connected to the ground of C1?	
59.	Are matching capacitors on opposite sides of the transmission line, and are they connected directly to the 2nd layer GND plane with multiple vias, including C1?	
60.	Are the matching components close to each other?	
61.	Does the PAVDD filtering network comprise of two shunt capacitors (120pF + 1uF) and a series ferrite?	
62.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

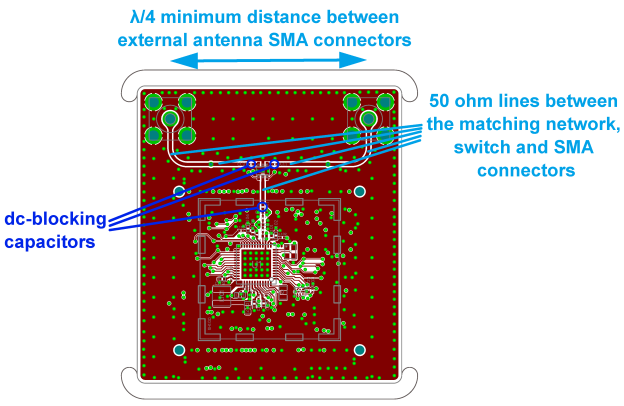
4.9 Additional Concerns for the EFR32xG24/26 Matching Network for High-Power (>10 dBm) Applications (QFN Package Variants)

63.	Is the first matching network component (C1) placed close to the TX/RX pin?	
64.	Is the recommended ~39 mil ground pour keep-out applied around the matching network area?	
65.	Is the PAVDD trace routed further away from the RF line? Is the PAVDD filtering network further away from both the RF trace and the PAVDD pin?	
66.	Is the RFVDD pin connected to the exposed pad ground AND to the ground of C1?	
67.	Are matching capacitors on opposite sides of the transmission line, and are they connected directly to the 2nd layer GND plane with multiple vias, including C1?	
68.	Are the matching components close to each other?	
69.	Does the PAVDD filtering network comprise of three shunt capacitors (120pF + 1uF) and a series ferrite?	
70.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

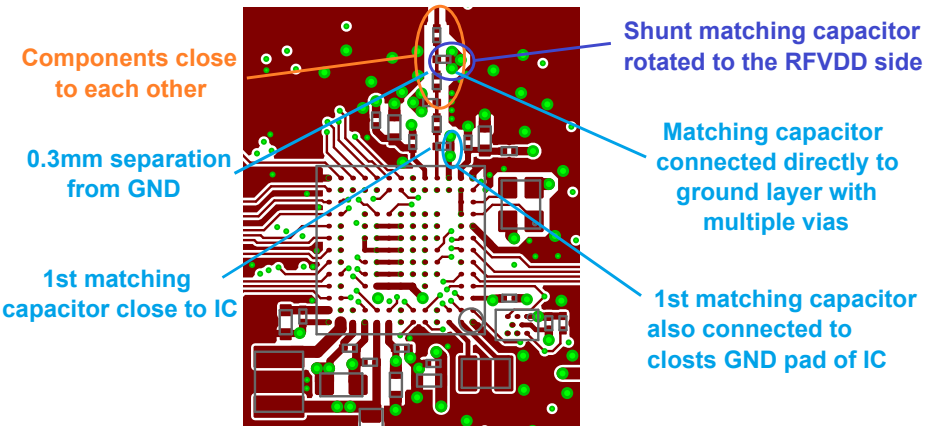
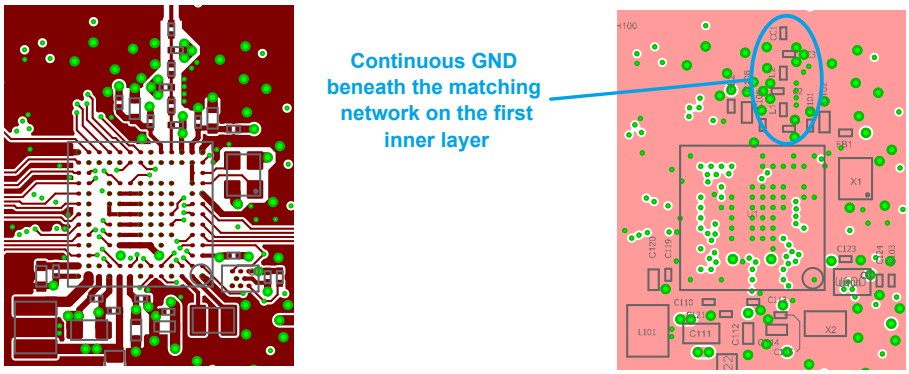
4.10 Additional Concerns for the EFR32xG24 Matching Network (WLCSP Package Variant)

71.	Are the matching components close to each other?	
72.	Is the first matching network component (L1) placed ~1.5 mm away from the TX/RX pin?	
73.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
74.	Is the shunt matching network capacitor rotated to the RFVDD side of the transmission line?	
75.	Is the shunt matching network capacitor connected directly to the 2nd layer GND plane with multiple vias?	
76.	Is GND added between the matching network and RFVDD filtering?	
77.	Is the area on the first inner layer beneath the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	
78.	Are the traces routed from the chip pins on the first inner layer with microvias as short as possible (to avoid splitting the GND plane)?	

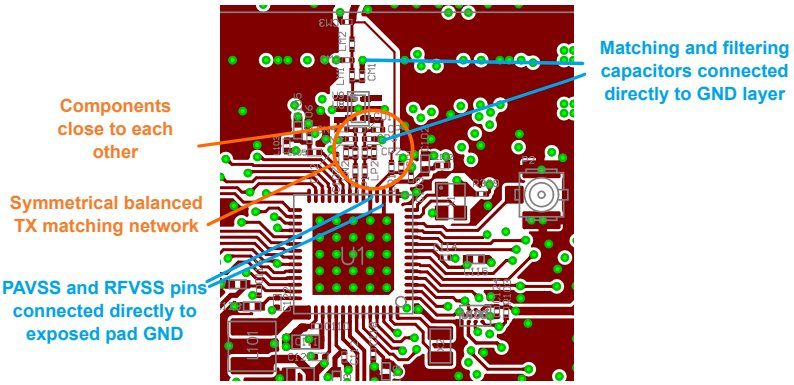
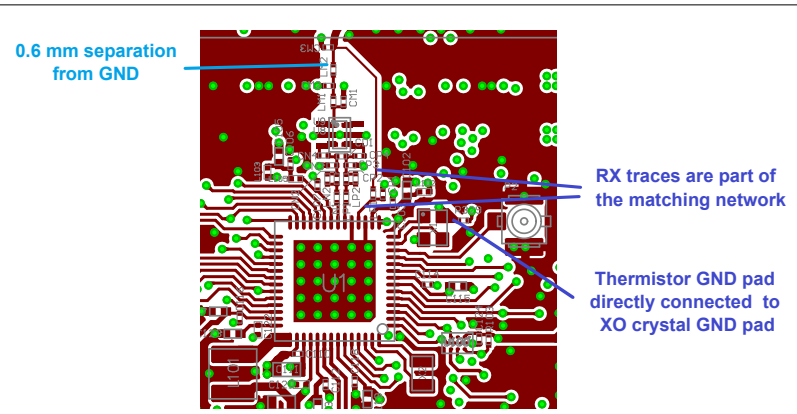
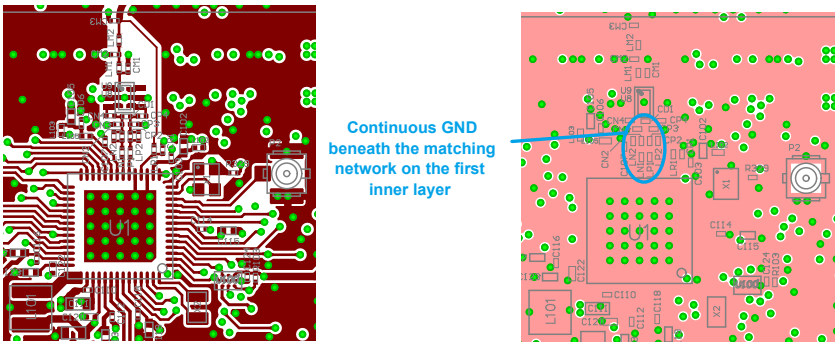
4.11 Additional Concerns for the EFR32xG24 Matching Network for High-Power Antenna Diversity Applications (>10 dBm)

79.	Are the SMA antenna connectors at minimum λ/4 distance from each other?	
80.	Are there dc-blocking capacitors at all RF switch ports?	
81.	Are the external antennas (e.g., monopoles) arranged orthogonally to each other?	

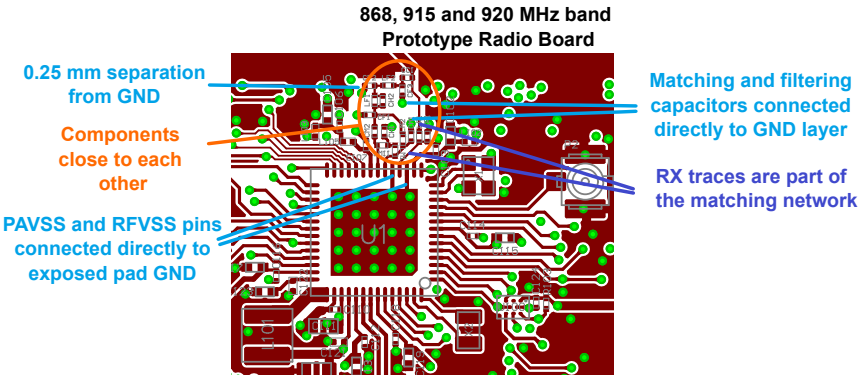
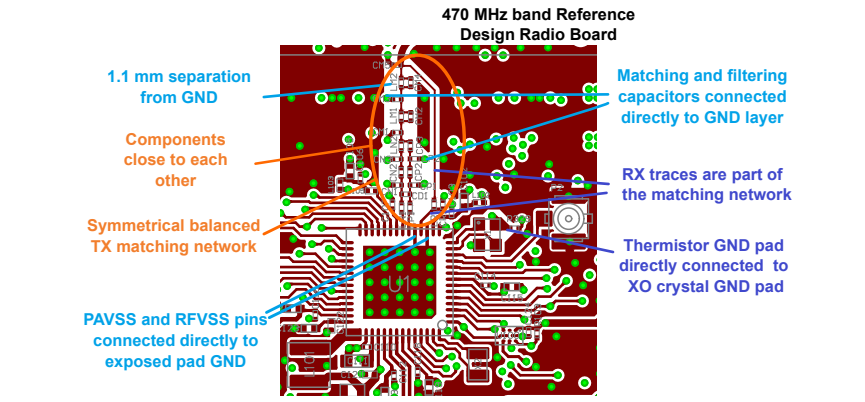
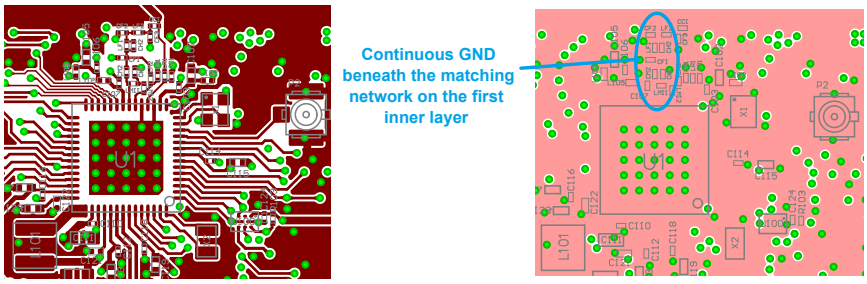
4.12 Additional Concerns for the EFR32xG26 Matching Network (BGA Package Variant)

82.	Are the matching components close to each other?	
83.	Is the first matching capacitor close to the TX/RX pin?	
84.	Are the shunt matching network capacitors connected directly to the 2nd layer GND plane with multiple vias? Is the 1st matching capacitor also connected to the closest GND pad of the IC?	
85.	Is the shunt matching network capacitor rotated to the RFVDD side of the transmission line?	
86.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
87.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

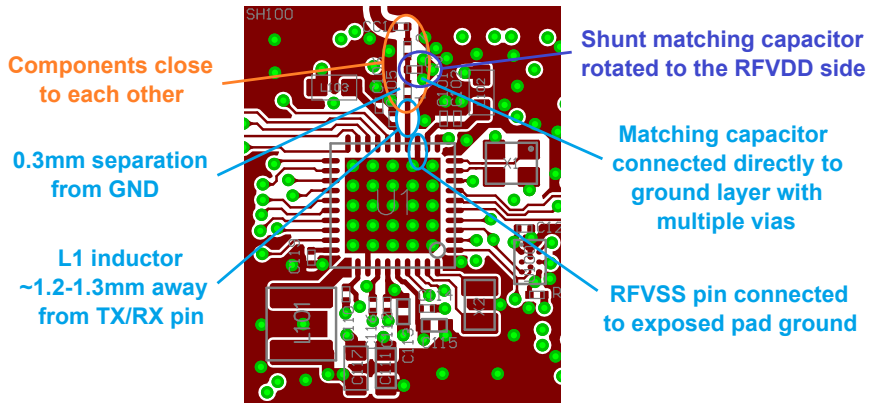
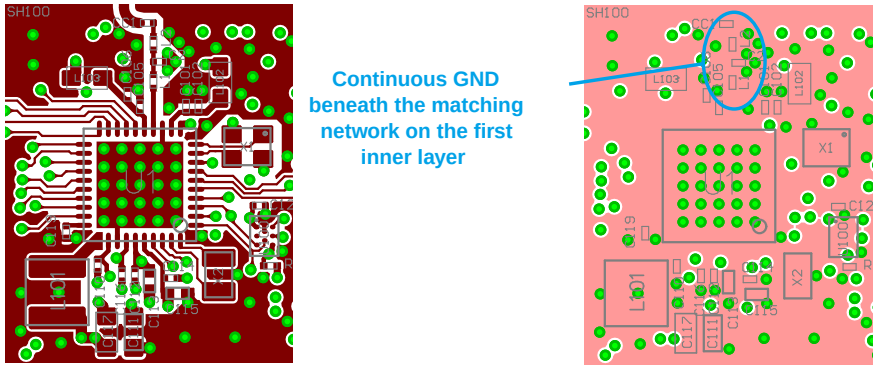
4.13 Additional Concerns for the EFR32xG25 Matching Network using an External Ceramic Balun

88.	Are the matching components close to each other?	
89.	Are shunt capacitors in the matching network connected directly to the first inner layer (common ground)? Is connecting the ground pins to the common ground metal on the Top Layer avoided?	
90.	Is the balanced TX matching network perfectly symmetrical?	
91.	Are the PAVSS and RFVSS pins connected directly to the exposed pad ground? Is connecting this pin to the common top layer ground avoided?	
92.	Is there at least 0.6 mm separation in the matching between the traces/pads and the GND metal?	
93.	Are the additional traces applied for the RX matching network?	
94.	Is the thermistor GND pad directly connected to the XO crystal GND pad (with no connection to the Top layer GND pour)?	
95.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

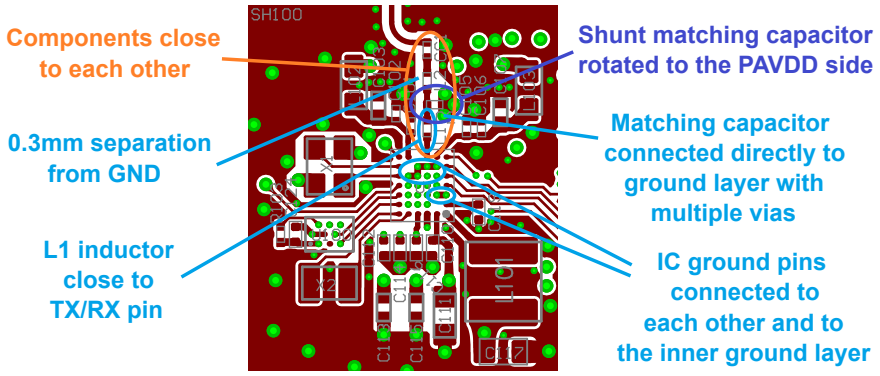
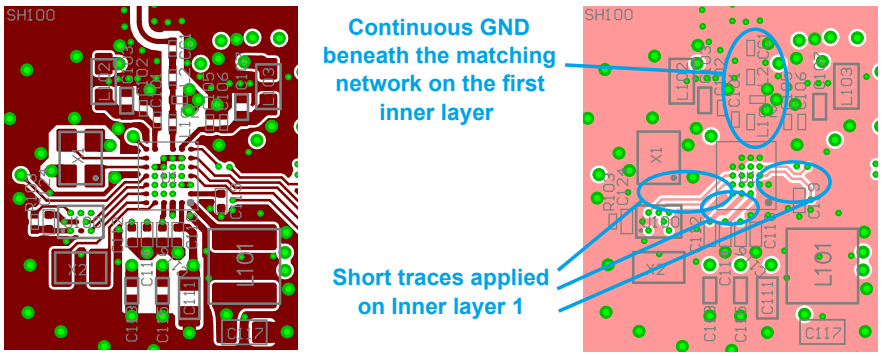
4.14 Additional Concerns for the EFR32xG25 Matching Network with Full Discrete Matching Network

96.	Are the matching components close to each other?	
97.	Are shunt capacitors in the matching network connected directly to the first inner layer (common ground)? Is connecting the ground pins to the common ground metal on the Top Layer avoided?	
98.	Are the PAVSS and RFVSS pins connected directly to the exposed pad ground? Is connecting this pin to the common top layer ground avoided?	
99.	Are the additional traces applied for the RX matching network?	
100.	For 470 MHz, is there at least 1.1 mm separation in the matching between the traces/pads and the GND metal?	
101.	For 868, 915, and 920 MHz, is there at least 0.25 mm separation in the matching between the traces/pads and the GND metal?	
102.	Is the thermistor GND pad directly connected to the XO crystal GND pad (with no connection to the Top layer GND pour)?	
103.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

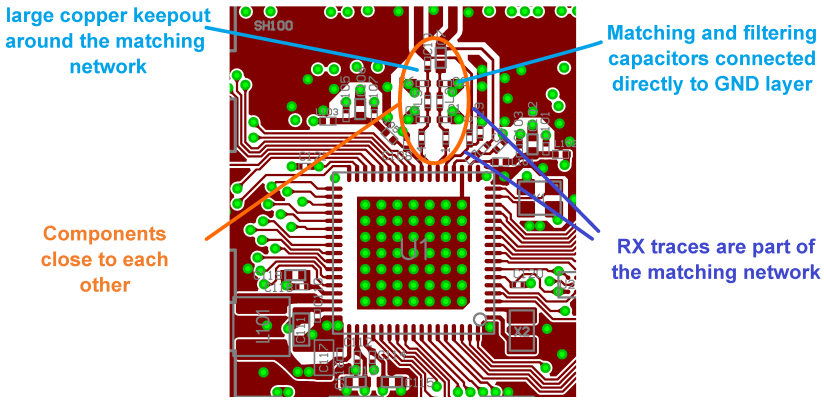
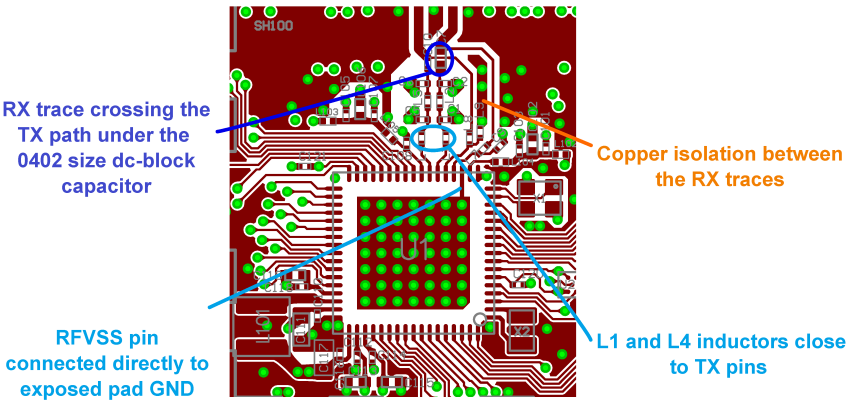
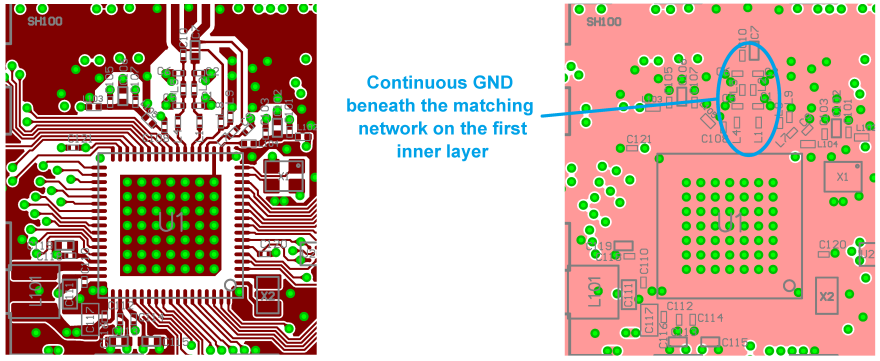
4.15 Additional Concerns for the EFR32xG27/29 Matching Network (QFN Package Variants)

104.	Are the matching components close to each other?	
105.	Is the first matching network component (L1) placed ~1.2-1.3 mm away from the TX/RX pin?	
106.	Is the RFVSS pin connected to the exposed pad ground only? Is connecting this pin to the common top layer ground avoided?	
107.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
108.	Is the shunt matching network capacitor rotated to the RFVDD side of the transmission line?	
109.	Is the shunt matching network capacitor connected directly to the 2nd layer GND plane with multiple vias?	
110.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

4.16 Additional Concerns for the EFR32xG27/29 Matching Network (WLCSP Package Variant)

111.	Are the matching components close to each other?	
112.	Is the first matching network component (L1) placed close to the TX/RX pin?	
113.	Are the chip GND pins connected to each other and to the inner GND layer?	
114.	Is there at least 0.3 mm separation in the matching between the traces/pads and the GND metal?	
115.	Is the shunt matching network capacitor rotated to the PAVDD side of the trans-mission line?	
116.	Is the shunt matching network capacitor connected directly to the 2nd layer GND plane with multiple vias?	
117.	Is the area on the first inner layer be-neath the matching network filled with continuous GND metal, and was wiring and routing avoided in this region? Are the traces routed from the chip pins on the first inner layer with microvias as short as possible (to avoid splitting the GND plane)?	

4.17 Additional Concerns for the EFR32xG28 Matching Network

118.	Are the first matching network components (L1 and L4) placed close to the RF pins?	
119.	Are the matching components close to each other?	
120.	Is the shunt matching network capacitor connected directly to the 2nd layer GND plane with multiple vias?	
121.	Is the RFVSS pin connected to the exposed pad ground only? Is connecting this pin to the common top layer ground avoided?	
122.	Is there a large copper keep-out and separation from the GND pour in the area of the matching network?	
123.	Is the RX trace routed under the 0402 size dc-blocking capacitor of the TX path of the other RF port?	
124.	Are the additional traces applied for the RX matching network?	
125.	Is there copper isolation between the RX traces of the two RF ports?	
126.	Is the area on the first inner layer beneath the RF chip and the matching network filled with continuous GND metal, and was wiring and routing avoided in this region?	

5. Revision History

Revision 1.7

July 2025
- Added EFR32xG29 recommendations.

Revision 1.6

February 2025
- Added EFR32xG26 recommendations.

Revision 1.5

July 2024
- Added +6 dBm 125 °C support for the EFR32xG27 WLCSP package.

Revision 1.4

September 2023
- Added EFR32xG24 WLCSP recommendations.
- Minor updates in various contents.

Revision 1.3

August 2023
- Added EFR32xG28 recommendations.

Revision 1.2

July 2023
- Updated EFR32xG21 to include revision EFR32xG21-C.

Revision 1.1

June 2023
- Added EFR32xG27 recommendations.
- Updated EFR32xG25 discrete matching network.

Revision 1.0

December 2022
- Added EFR32xG25 layout recommendations.

Revision 0.9

April 2022
- Added EFR32xG24 layout recommendations.
- Added EFR32xG23 with HFCLKOUT pin layout recommendations.
- Added EFR32xG23 2 RF Front-End Use layout recommendations.

Revision 0.8

September 2021
- Added EFR32xG23 layout recommendations.

Revision 0.7

August 2021
- Added T-matching network concept for EFR32xG22.

Revision 0.6

January 2021
- Corrected total copper keep-out value around the matching network for generic layout concept.

Revision 0.5

December 2020
- Corrected broken links

Revision 0.4

November 2020
- EFR32xG22 existing and generic layout concept recommendations were added

Revision 0.3

March 2020
- EFR32xG22 layout recommendations were added

Revision 0.2

November 2019
- EFR32xG21 0 dBm and 0 / 10 dBm matching network layout recommendations were added

Revision 0.1

March 2019
- Initial release.

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