AN930.1: EFR32 Series 1 2.4 GHz Matching Guide

The EFR32 devices include chip variants that provide 2.4 GHz-only operation, sub-GHz-only operation, or dual-band (2.4 GHz and sub-GHz) operation. In addition, the EFR32 chips are available in a 7x7 mm 48-pin package and a 5x5 mm 32-pin package. This application note describes the matching techniques applied to the EFR32 Series 1 Wireless Gecko Portfolio in the 2.4 GHz band.

For information on PCB layout requirements for proper 2.4 GHz operation, refer to AN928.1: EFR32 Series 1 Layout Design Guide. Refer to AN933.1: EFR32 Series 1 Minimal BOM for information on minimizing the bill of materials. For information on the matching procedure for the sub-GHz path, refer to AN923: EFR32 sub-GHz Matching Guide.

KEY POINTS

- Description of the applied 2.4 GHz matching networks and techniques for the EFR32 device
- Detailed discussion of the design steps and design examples
- Three different EFR32 versions: 7x7 mm 48-pin dual band version, 7x7 mm 48-pin 2.4 GHz version, and 5x5 mm 32-pin 2.4GHz version.
- Measured TX spectrum and RX sensitivity results

1. Introduction

This application note is intended to help users achieve the best 2.4 GHz RF match for targeted applications. It describes the details of matching network design procedures and presents additional test results.

Thorough derivations of four different matching topologies are presented:

- A ladder 2-element LC match for up to 10 dBm power levels
- A ladder 4-element LCLC match for up to 20 dBm power levels
- A hybrid type match applying both discrete elements and a transmission line (LC-Tline-C) for up to 20 dBm power levels
- A parallel LC 2-element match for up to 13 dBm power levels

Readers simply seeking recommended values, topologies, and RF performance data should skip to Appendix 2. 2.4 GHz RF Network Schematics and Technical Data.

The presented matches are tested with three EFR32 variants:

- 7x7 mm, 48-pin 2.4 GHz
- 5x5 mm, 32-pin 2.4 GHz
- 7x7 mm, 48-pin dual band

For example, the 7x7 mm, 48-pin 2.4 GHz-only version's package pinout is shown in the figure below. The 2.4 GHz RF pins are high-lighted with a red box.
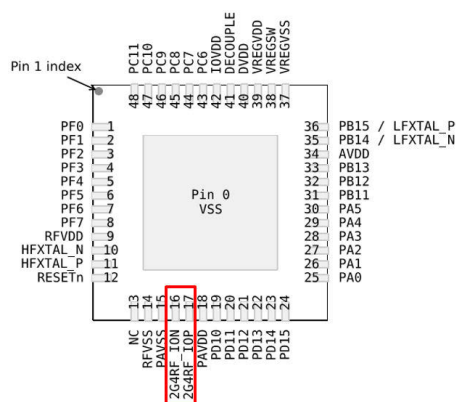

Figure 1.1. EFR32 2.4 GHz RF Pins

1.1 Related Literature

Related documentation includes:

- AN923: EFR32 sub-GHz Matching Guide
- AN928.1: EFR32 Series 1 Layout Design Guide
- AN933.1: EFR32 Series 1 Minimal BOM
- AN0002.1: EFM32 and EFR32 Wireless Gecko Series 1 Hardware Design Considerations

2. EFR RF Architecture Overview

The EFR32 chip family has separate sub-GHz and 2.4 GHz RF front ends. The sub-GHz part is not detailed here. The 2.4 GHz RF front end architecture of the EFR32 chip is shown in the figure below.

The 2.4 GHz front end has a unified, single-ended TX and RX pin (2G4RF_IOP), so the TX and RX paths are tied together internally. The 2G4RF_ION TX pin has to be grounded at the pin. It should consist of a good RF ground with multiple parallel GND vias.
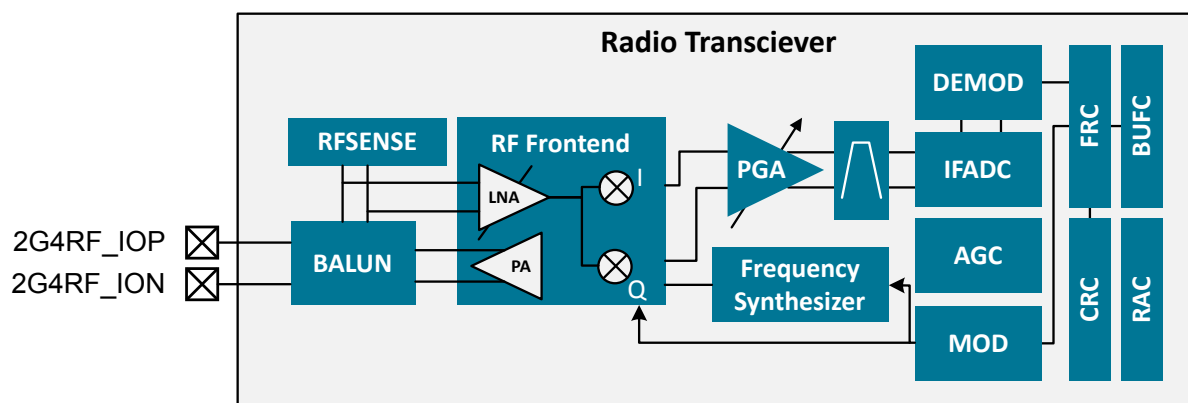

Figure 2.1. 2.4 GHz Front End Configuration

The on-chip part of the front end comprises a variable (from 0 dBm to 20 dBm) power class AB differential PA, a variable PA tuning cap, a differential LNA, an LNA/low-power PA match and protection circuit, and an integrated balun. The high-power PA is biased through the PAV_{DD} pin. Externally, a single-ended matching network and harmonic filtering are required.

3. 2.4 GHz RF Matching Design Steps

2.4 GHz RF matching design for EFR32 chips consists of the following steps:

1. Determine the optimum termination impedance for the PA.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the pcb have a major effect, so tuning/ optimization of the design is required. Here an optional EM simulation can be done, but simulations with well-estimated pcb parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

3.1 Determining the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the 2G4RF_IOP pin if 50 Ω termination is applied at the antenna port.

The 2G4RF_IOP RF port termination determines the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX mode. In addition, proper harmonic suppression and good RX sensitivity in reception mode are required.

The optimum termination impedance for delivering maximum power in TX mode is determined by load-pull testing. A good termination impedance compromise for all EFR variants and for all power levels is Zload_opt = ~23+j11.5 Ω. Refer to Appendix 1. PA Optimum Impedance Determination for more details. This termination impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load.

The proper impedance at the single-ended output pin (2G4RF_IOP) also depends on the grounding of the other (2G4RF_ION) TX pin. To keep its effect negligible, this pin should be massively connected ("back-routed") to the next ground layer beneath it by multiple vias, as shown by the blue dashed ellipse in the figure below. More detailed information about proper layout design can be found in AN928.1: EFR32 Series 1 Layout Design Guide.
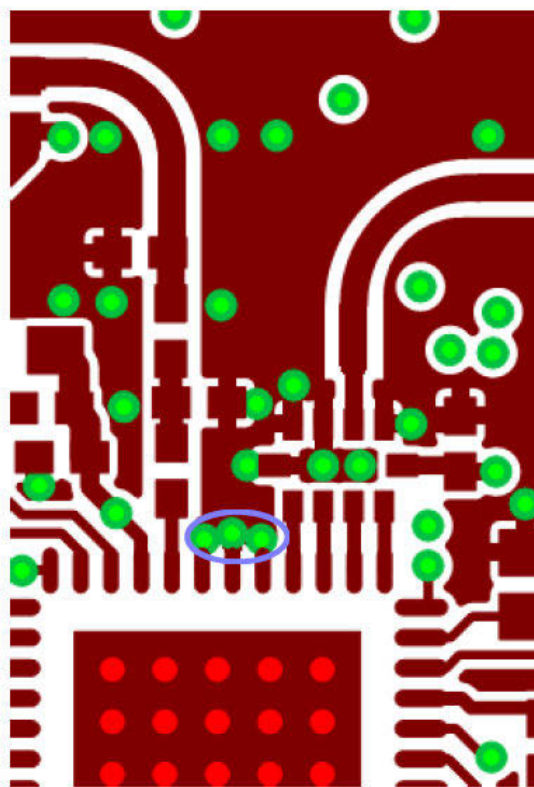

Figure 3.1. Element Match PCB Layout with Good 2G4RF_ION Grounding

In real radio links, the TX power and the receiver sensitivity together (i.e., the link budget) determine the range. So, with the applied TX termination impedance, the impedance match in RX mode should also be acceptable. Fortunately, the RX sensitivity is quite immune to impedance variations. The sensitivty variation is less than 0.2 to 0.3 dB if the termination changes from 50 Ω to the PA optimum impedance (Zload_opt) given above.

3.2 Choosing the RF Matching Topology

The second step of the matching design procedure is to choose the appropriate RF matching topology.

In addition to creating an optimum termination impedance on the IC side, the matching solution must exhibit sufficiently robust harmonic filtering characteristics to comply with emissions standards. There are many different types of RF matching topologies. Separate matching and harmonic filtering sections can be utilized, or they can be combined in one circuit. To minimize the number of elements, all matches presented here are of the combined type, with low-pass circuits employed for their inherent harmonic suppression characteristics.

Four 2.4 GHz matching topologies are presented here:
* A ladder 2-element LC match for up to 10 dBm power levels.
* A ladder 4-element LCLC match for up to 20 dBm power levels.
* A hybrid type applying both discrete elements and a transmission line (LC-Tline-C) for up to 20 dBm power levels.
* A parallel LC 2-element minimal BOM match for up to 13 dBm power levels. This match is derived from the hybrid LC-Tline-C match by eliminating the Tline and second capacitor.

For final match schematics and RF performance data, refer to Appendix 2. 2.4 GHz RF Network Schematics and Technical Data.

The selection of the proper match from the above four topologies depends on special application requirements.
* The **Ladder 2-Element Match** has moderate second harmonic suppression, and, therefore, can only operate up to 10 dBm with FCC compliance. It applies a series film type SMD (LQP15TN series from Murata) inductor and so has a higher cost than the parallel LC match. Moreover, it has slightly higher insertion loss. The advantage of the Ladder 2-Element Match lies in its superior suppression of third and higher harmonics. The Ladder 2-Element Match will be detailed in subsequent sections.
* At high power levels, the **Ladder 4-Element LCLC Match** gives very strong second and higher harmonic suppression but has slightly lower TX power and worse sensitivity due to higher insertion loss. However, it is a very stable match, being less sensitive to element spreading. For more information about the Ladder 4-Element Match design, refer to Appendix 3. 2.4 GHz Ladder 4-element RF Matching Design Steps.
* The **Hybrid Type LC-Tline-C Match** uses the inexpensive LQG15HS multilayer inductor series from Murata. Its harmonic suppression is nearly as good as that of the Ladder 4-Element type but with lower cost and better insertion loss, i.e., slightly higher power and better sensitivity. The drawback is a slightly larger footprint due to the 3.5 mm long transmission line. For more information about the LC-Tline-C Match design, refer to Appendix 4. Transmission Line (Tline) Match for Minimal BOM Solutions (U.S. Patent US9780757B1).
* The **Parallel LC Match** is a very low-cost, simplified version of the Hybrid Type LC-Tline-C match since the transmission line and second parallel capacitor are eliminated. It features an inexpensive LQG15HS series inductor and minimal PCB area. It has very low insertion loss and thus good power and sensitivity. The drawback is its reduced third or higher harmonic suppression, so it is only FCC compliant up to ~13 dBm. It may be compliant at higher power levels if used with an antenna possessing higher harmonic suppression characteristics. For more information about the parallel LC, refer to Appendix 4. Transmission Line (Tline) Match for Minimal BOM Solutions (U.S. Patent US9780757B1).

3.3 Initial Design with Ideal, Loss-Free Elements

After choosing the best topology for the application, the third step of the matching design procedure is to generate a lumped element schematic of the match with ideal loss-free elements and without PCB parasitics. The matching circuit should show an input impedance of Zload_opt = ~23 + j11.5 Ω terminated with a 50 Ω load at its output.

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free ideal capacitors and inductors are used, and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization.

In the following sections, the design steps of the Ladder 2-Element Match are demonstrated. The design steps for the other three match types can be found in Appendix 3. 2.4 GHz Ladder 4-element RF Matching Design Steps and Appendix 4. Transmission Line (Tline) Match for Minimal BOM Solutions (U.S. Patent US9780757B1).

The matching circuit should show the Zload_opt = ~23 + j11.5 Ω impedance at the input while it is terminated by 50 Ω at its output. The general, lumped, two-reactive-element matching technique can be applied to create a schematic of the simplest two-element match (see Item 1 in 6. References). In theory, two possible solutions exist: low-pass and high-pass. These procedures, along with their corresponding schematics and Smitch chart solutions, are shown in the figure below. The antenna side is denoted by the 50 Ω ZL load impedance in the schematics and indicated by the DP1 points in the Smith chart centers. The PA side impedance is denoted by Zin in the schematics and given by the TP3 endpoints in the Smith charts. In both the low-pass and high-pass cases, the TP3 endpoint is the optimum impedance (Zload_opt = 23+j11.5 Ω). Since the circuit should also filter the harmonics, only the low-pass solution, which consists of a series 2.3 nH inductor and a 1.4 pF parallel capacitor (as shown in the first column of the figure) can be used in real designs.
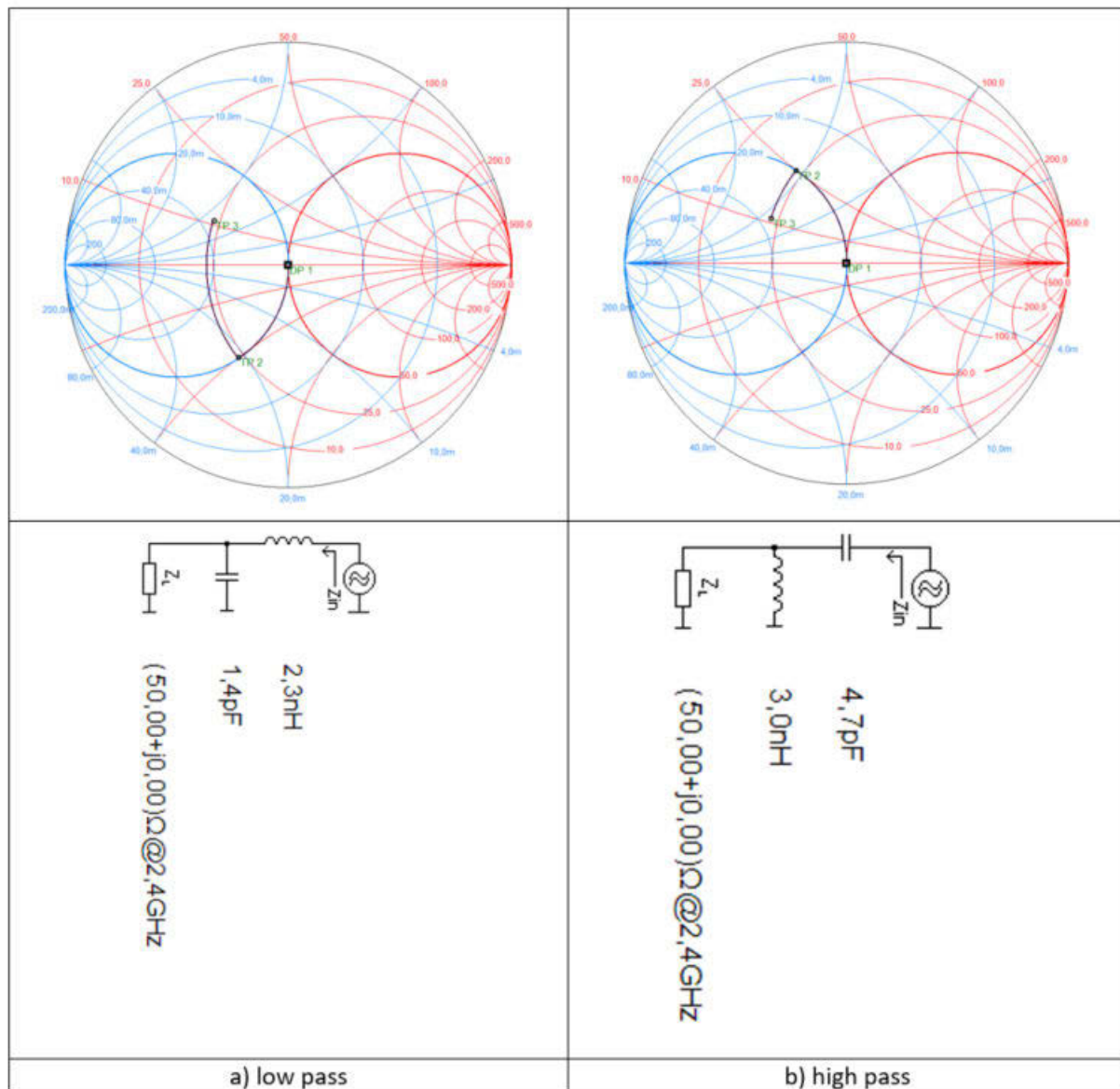
Figure 3.2. Basic Two-Element Matching Techniques with Ideal Lumped Elements

3.4 Design with Parasitics and Losses

The fourth step should be to take into account the parasitics of the discrete components. For Silicon Labs reference designs 0402 or 0201-sized, surface mount device (SMD) elements are used. With 0201 elements, one can expect lower parasitics, but their handling is more difficult.

3.4.1 Effects of SMD Discrete Parasitics and Losses

Inductors are the most critical elements in matching networks due to their higher cost and lower Q compared to SMD capacitors. There are three basic SMD inductor types: wirewound, metal-film-based, and multilayer. A good description of SMD inductors can be found in Item 2 of 6. References. The wirewound inductor has the best Q, while the multilayer type has the worst. The better Q (i.e., lower loss) helps achieve low insertion loss in low-pass ladder structures where the inductor is the series element. Unfortunately, the price of the wirewound inductor is the highest, typically several cents, while the multilayer is the least expensive, typically much less than a cent when purchased in high volume. Film type inductors are between these in cost, so they are a good compromise at 2.4 GHz in terms of price and Q.

SMD parasitics are investigated in the ladder two-element match employing 0402 SMD elements and a film type inductor. Simplified equivalent circuits of the Murata SMD capacitance (1.4 pF) and film inductance (2.3 nH) are shown in the figure below. These simplified equivalent circuits are only accurate at the fundamental frequency. For higher harmonic simulations, the measured S-parameters given by the SMD manufacturer are used. Using these SMD models, the impedance differs slightly from the optimum Zload_opt = 23 + j11.5 Ω at the generator side of the match (see Figure 3.4 2-Element Match Mistuning with Real SMD Elements on page 9). To shift it back to the optimum, a slight decrease of the parallel capacitance to 1.2 pF is required.
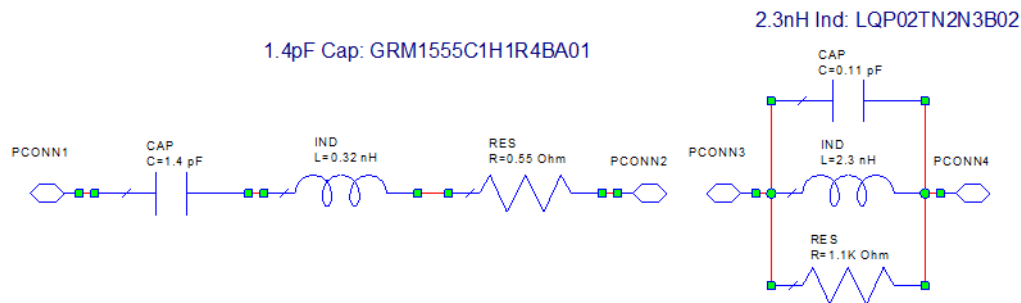

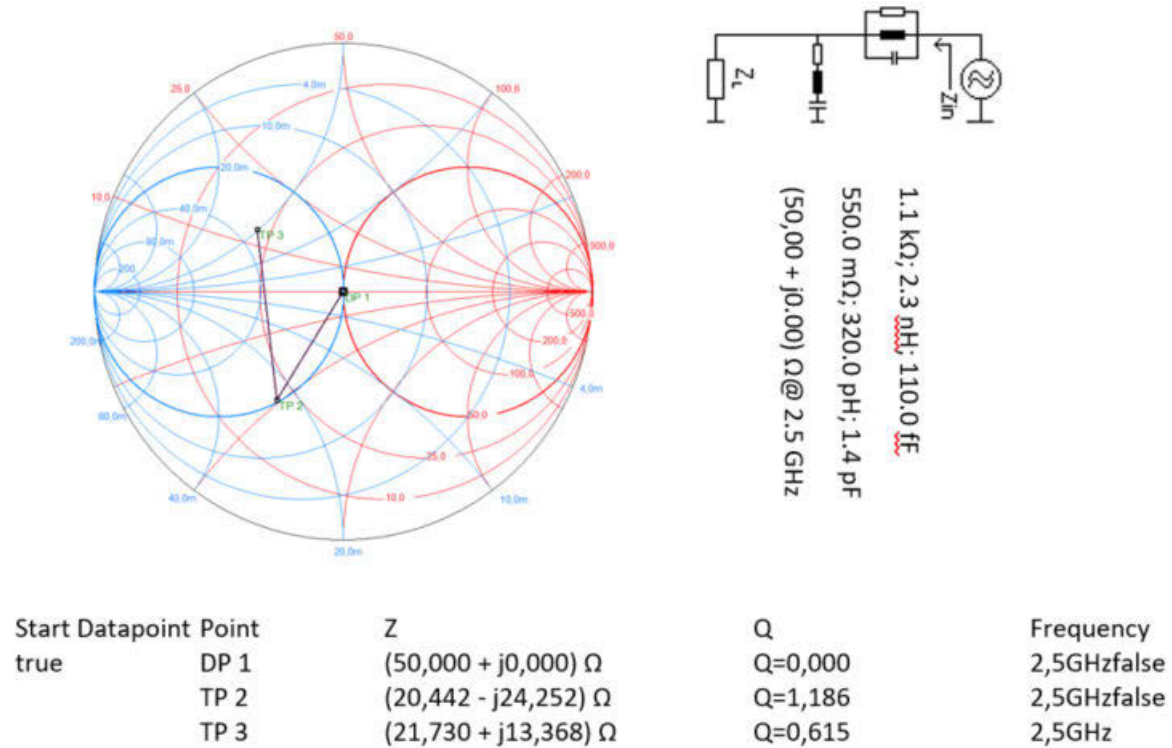**Figure 3.3. Equivalent Circuits of Real SMDs at the Fundamental Frequency**

Start Datapoint	Point	Z	Q	Frequency
true	DP 1	$(50{,}000 + j0{,}000)\ \Omega$	Q=0,000	2,5GHzfalse
	TP 2	$(20{,}442 - j24{,}252)\ \Omega$	Q=1,186	2,5GHzfalse
	TP 3	$(21{,}730 + j13{,}368)\ \Omega$	Q=0,615	2,5GHz

Figure 3.4. 2-Element Match Mistuning with Real SMD Elements

3.4.2 Rough Estimation of PCB Parasitics

In addition to the discrete parasitics, the following PCB trace parasitics also have significant effects:

• Series inductances (denoted by Ls)
• Parallel capacitances (denoted by Cp)
• Losses

These trace parasitics usually enforce the further decrease in values of the discrete low-pass prototype matching elements (series inductance and parallel capacitance). There are three approaches to simulating PCB parasitics: lumped element, distributed element, and EM-based. Since the trace lengths in the match are usually shorter than 1 mm (much lower than the wavelength at 2.4 GHz), even the simple lumped element method gives good accuracy. The most accurate is the EM-based method, but that usually requires expertise and expensive CAD tools.

The figure below shows the reference plane positions used in the simulations for the EFR32 IC 2G4RF_IOP pin and for the discrete SMD pins. Since the IC pin covers the whole pad area, the reference plane falls to the geometric center of the PCB pad. With the discrete SMD elements, the reference plane is put at the ends of the SMD soldering pin.
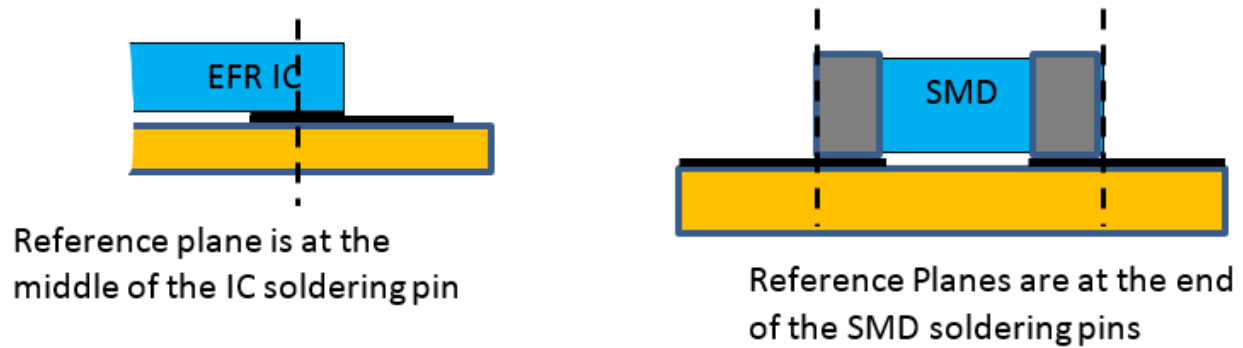

Figure 3.5. Reference Planes with Real SMD Elements

Figure 3.6 Estimation of PCB Layout Parasitics on page 10 shows the Rf part of the top layer of the 5x5 mm packaged EFR single band design with estimated pcb series parasitic inductor and parallel capacitor values. The series pcb parasitic inductors are calculated here using the reference plane definitions of Figure 3.5 Reference Planes with Real SMD Elements on page 10. The parallel parasitic cap values are calculated to the whole printed area including the soldering pads. Here, estimation both for the area cap (calculated from the dielectric thickness down to the grounding layer beneath and from the pad dimensions) and the fringing field caps (to the side ground metal on the same layer) are required. The gap to the side ground metal are given by the G parameters in the figure. The easiest way to make that estimation is to use a grounded coplanar calculator, which computes the unit parallel capacitance and series inductance parasitics as well. Numerous calculators can be found on the internet. An example of this type of calculator is given in Item 3 of 6. References at the end of this document.

The ladder 2-element matching circuit with PCB parasitics is shown in Figure 3.7 2-Element Lumped Element Match with Discrete Models of PCB Layout Parasitics on page 11. The applied PCB layout is proper for incorporating a ladder four-element match; so, if only the ladder two-element match is applied, the additional LC section (a series inductor denoted by L1 and a parallel capacitor denoted by C1) is not populated. In this case, a 0 Ω resistor has to be used in the place of the series L1. The parasitic series inductance of this 0 Ω resistor is ~0.1 nH, which is also included in the figure. The losses of the PCB traces are not taken into account because they are much smaller compared to the losses of the applied SMD discretes.
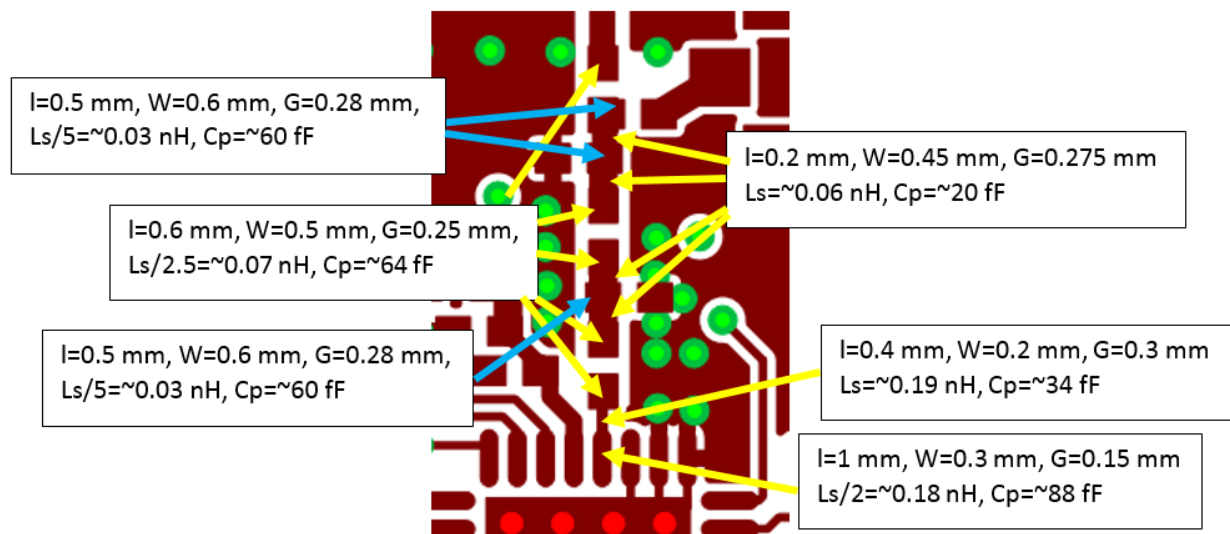

Figure 3.6. Estimation of PCB Layout Parasitics

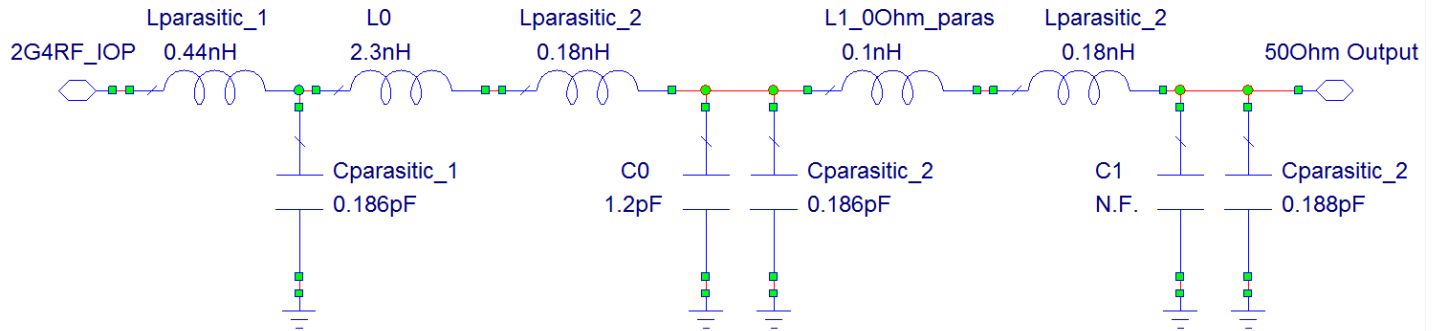## 2 element 2.4GHz match with discrete layout pcb parasitics

Figure 3.7. 2-Element Lumped Element Match with Discrete Models of PCB Layout Parasitics

These PCB parasitics detune the matching network in the same way as the SMD parasitics described previously. Here, the further decrease of the applied series inductor (L0) to 1.8 nH and parallel capacitor (C0) to 1.1 pF compensates for the PCB parasitic effects. Unfortunately, the harmonic suppression of the ladder two-element match is insufficient at the 20 dBm power level, so it is only used up to 10 dBm. At power levels above 10 dBm, the ladder four-element match is required to comply with the harmonic restrictions of the ETSI and FCC standards. However, below 10 dBm power levels, the ladder two-element match is advantageous because it has lower cost and lower insertion loss compared to the ladder four-element match. Furthermore, if a dedicated match is designed for the low-power regime, then it is useful to tune it to the optimum load-pull impedance of the 10 dBm power level, which is ~20 + j10 Ω as documented in Appendix 1. PA Optimum Impedance Determination and . The figure below shows the modified match (with L0 = 1.7 nH, C0 = 1.2 pF) to this new impedance.
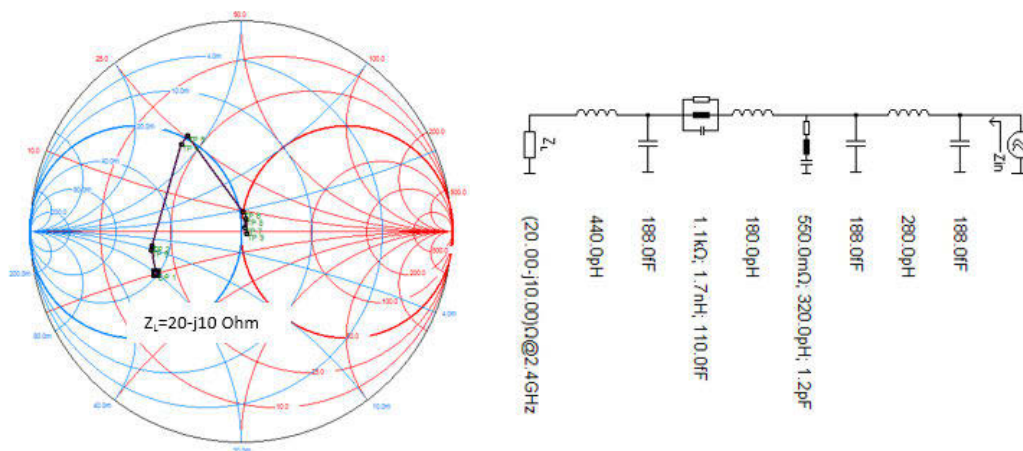

Figure 3.8. 2-Element Match with SMD and PCB Layout Parasitics Tuned for the 10 dBm Power Level Optimum (20 + j10 Ω)

3.4.3 EM Simulations

As mentioned previously, the best accuracy can be achieved by EM simulations. However, this step can be skipped if the proper CAD tool is not available. The EM simulated results shown here were created by an Axiem 3D planar simulator of AWR Corporation.

The figure below shows a simulated layout. This layout is used for both the ladder two-element and four-element matches. Here, the 2G4RF_IOP pin of the EFR32 chip is connected to Port 2. The L0 inductor is connected between Ports 3 and 4, the C0 capacitor between Ports 5 and 6, the L1 inductor between Ports 7 and 8, and the C1 capacitor between Ports 9 and 10. For the ladder two-element match, a 0 Ω is connected to the place of L1 and the C1 and is not fitted.
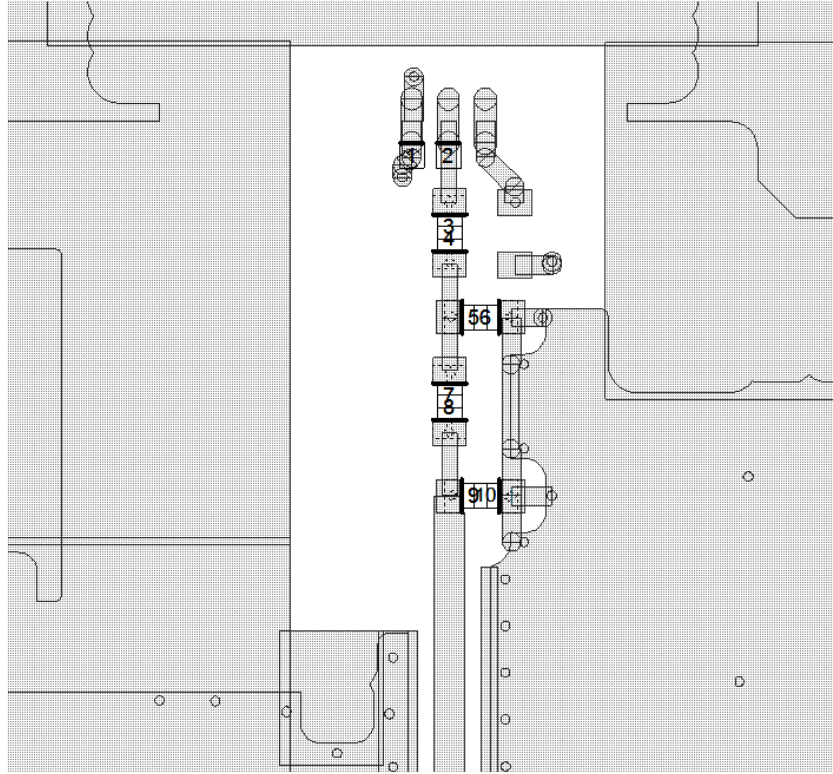

Figure 3.9. EM Simulated Layout for the Discrete Lumped Element Matches

Figure 3.10.a shows the EM simulated impedance of the ladder two-element match at the EFR32 TX pin (Port 2) together with the targeted 10 dBm power impedance (~20 + j10 Ω). They are quite close. Here an L0 series inductance of 1.9 nH and a C0 parallel capacitance of 1.5 pF is used as shown in the following table.

Table 3.1. Final SMD Values for the Ladder Two-Element Match

Two-element Matching Network				
Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
LH0	1.9 nH	±0.05 nH	LQP15MN1N9W02	Murata
CH0	1.5 pF	±0.1 pF	GRM1555C1H1R5BA01D	Murata

Figure 3.10.b shows the simulated transfer characteristic from the TX pin to the 50 Ω output port. As expected, the second harmonic suppression is sufficient only up to ~10 dBm fundamental power.
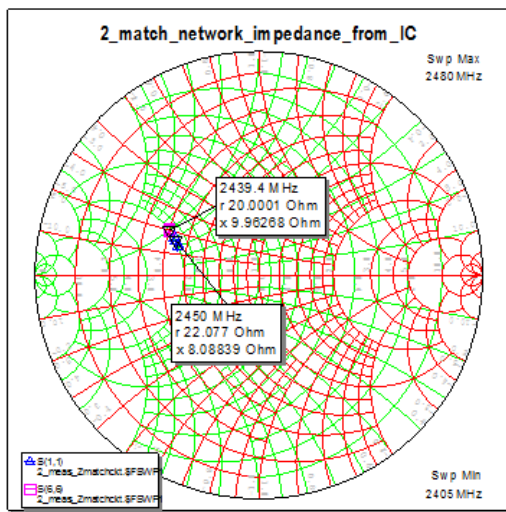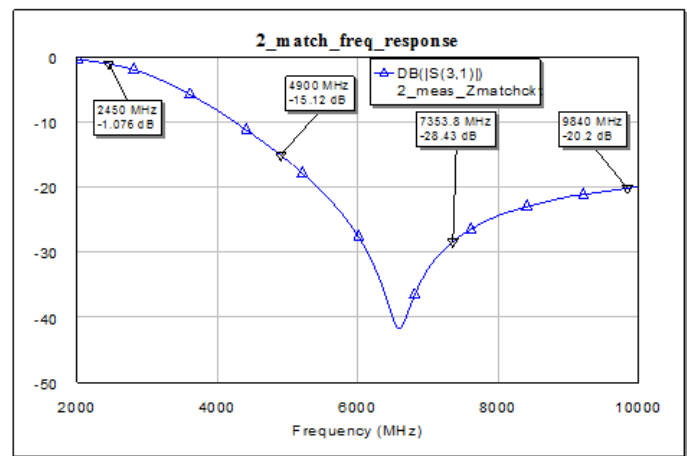
Figure 3.10. EM Simulation Results of the Ladder Two-Element SMD Match

3.5 Bench Tuning and Measured Results

The final (fifth) step of the matching design is bench tuning with real measurements. The figure below shows the impedance and transfer characteristic measurement setup. Port 1 of the VNA is connected to the soldering pad of the 2G4RF_IOP pin through a pigtail (the EFR32 chip is removed here as only the matching network is measured). The reference plane of the S-parameter measurements is shifted to the TX pin. Port 2 is connected to the matching 50 Ω side output through a UFL connector.
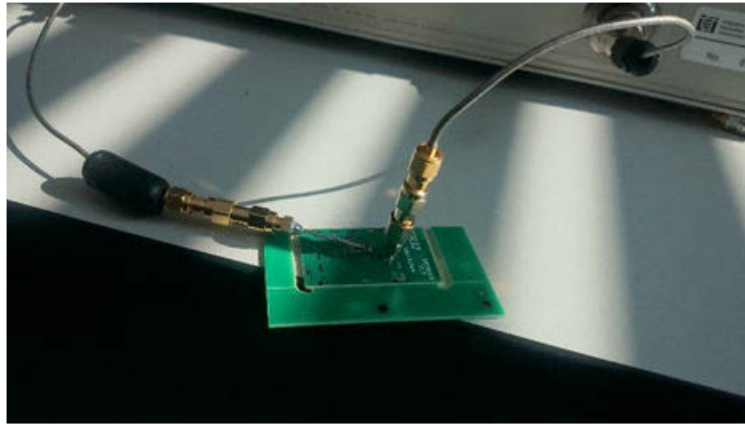

Figure 3.11. Match Impedance and Transfer Characteristic Measurement

The figure below shows the measured impedance and transfer characteristic of the ladder two-element match with the final SMD elements. As shown, the real part is very close to the targeted 20 Ω, but the reactance is slightly higher (14 Ω instead of the targeted 10 Ω). This slight deviation causes a negligible (> 0.1 dB) power drop, so the match is not tuned further.

Second harmonic suppression is only 13.7 dB, so the ladder two-element match is, as expected, only proper for the lower (< +10 dBm) power regimes.
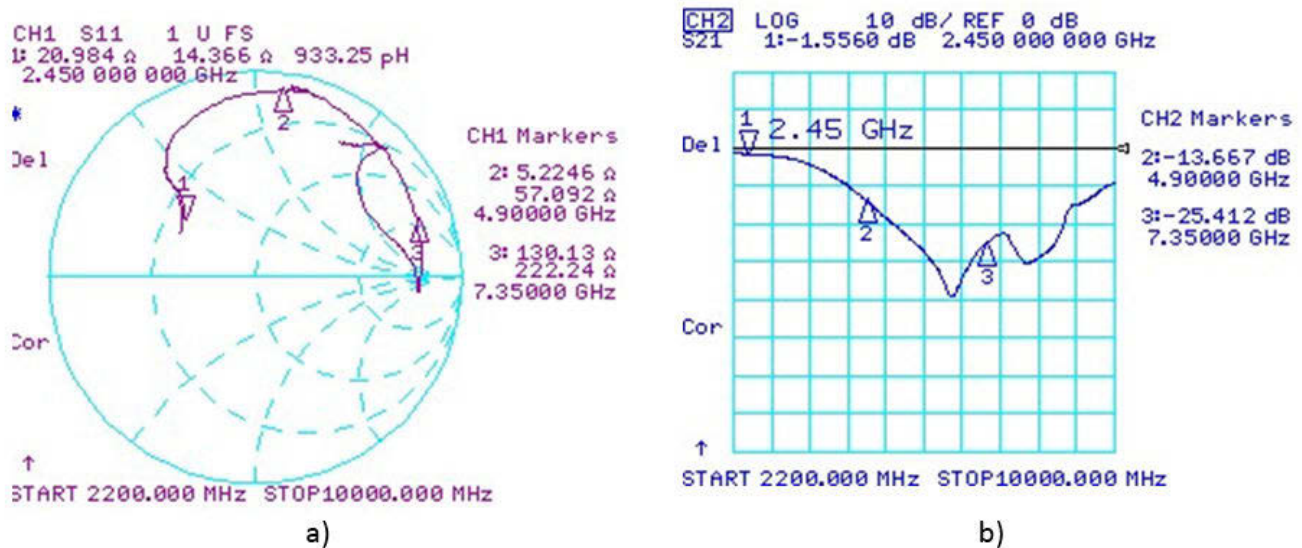

Figure 3.12. Measured S11 and S21 (Transfer) Characteristic of the Ladder 2-element SMD Match

The measured ladder two- and four-element spectrum plots in the middle of the band (2.45 GHz) with the 7x7 mm dual band EFR32 version is shown in in the first column of Figure 3.13 Measured Spectrum Plots of the Dual Band 7x7 mm EFR32 with (a) a Ladder Two-Element Match in 10 dBm Power State and (b) a Ladder Four-Element Match in 20 dBm Power State on page 15. In the second column, the four-element match spectrum is also given. The ladder two-element match is tested with a 10 dBm power setting, while the four-element match is tested with a 20 dBm power setting.

In the 20 dBm power setting, the achieved fundamental power is ~19 dBm at 2.45 GHz. Large volume measurements show approximately ±1 dB variation of the output power. The average is typically ~19.5 dBm with 134 mA total IC current. Note that the loss of the applied UFL connector is approximately 0.3–0.5dB. With direct connection, the delivered power is around 20 dBm.

With the ladder two-element match, the IC consumes ~40 mA current at ~10 dBm power level. At low power levels, due to the lower current consumption and the required lower PA supply voltage, the built in dc-dc converter can supply the PA through the PA_VDD pin. The generated supply voltage by the dc-dc converter is 1.8V, which is correct for PA operation up to 13 dBm power levels. Since the dc-dc converter converts the higher external supply voltages to the optimum 1.8 V with good efficiency, the PA efficiency improves significantly. Without the dc-dc converter, the PA unnecessarily burns significant dc power and, thus, has lower efficiency at higher supply voltages. A second advantage is that, with the dc-dc converter, the PA power is stable independently of external VDD variations. For these reasons, Silicon Labs suggests supplying the PA_VDD rail from the internal dc-dc converter up to power levels of 13 dBm. The allowed harmonic level by the US FCC is –41.2 dBm EIRP (or 500 µV/m electric field strength at a distance of three meters), while it is -30 dBm EIRP by EU ETSI regulation. As shown in the figures, the second harmonic with the ladder two-element match has approximately 3 dB margin to the more strict FCC limit at a 10 dBm power level. With the ladder four-element match, the margin is much larger, even at the highest (20 dBm) power level.

It should be noted that, in the spectrum measurements, the Spectrum Analyzer is used as a wideband 50 Ω termination. With a real antenna, the termination at the harmonics can differ significantly from 50 Ω with variations in power delivered to the antenna. Moreover, the harmonic termination impedance at the matching output depends on the transmission line properties between the matching network and the antenna. In addition, the radiation gain of the antenna can differ at harmonic frequencies. Due to these facts, the radiated harmonic power levels can be very different from the conducted measurement results and must be checked with the final antenna.

The different package versions have no significant effect on the output spectrum using both the ladder two-element and four-element matches. Band edge (2.4 GHz and 2.48 GHz) spectrum variations across the bands are typically less than 0.5 dB, and the harmonics are also much lower than the allowed limits, independent of package versions. More information about power variation across the band and the package effect can be found in Appendix 2. 2.4 GHz RF Network Schematics and Technical Data.

a)   b)
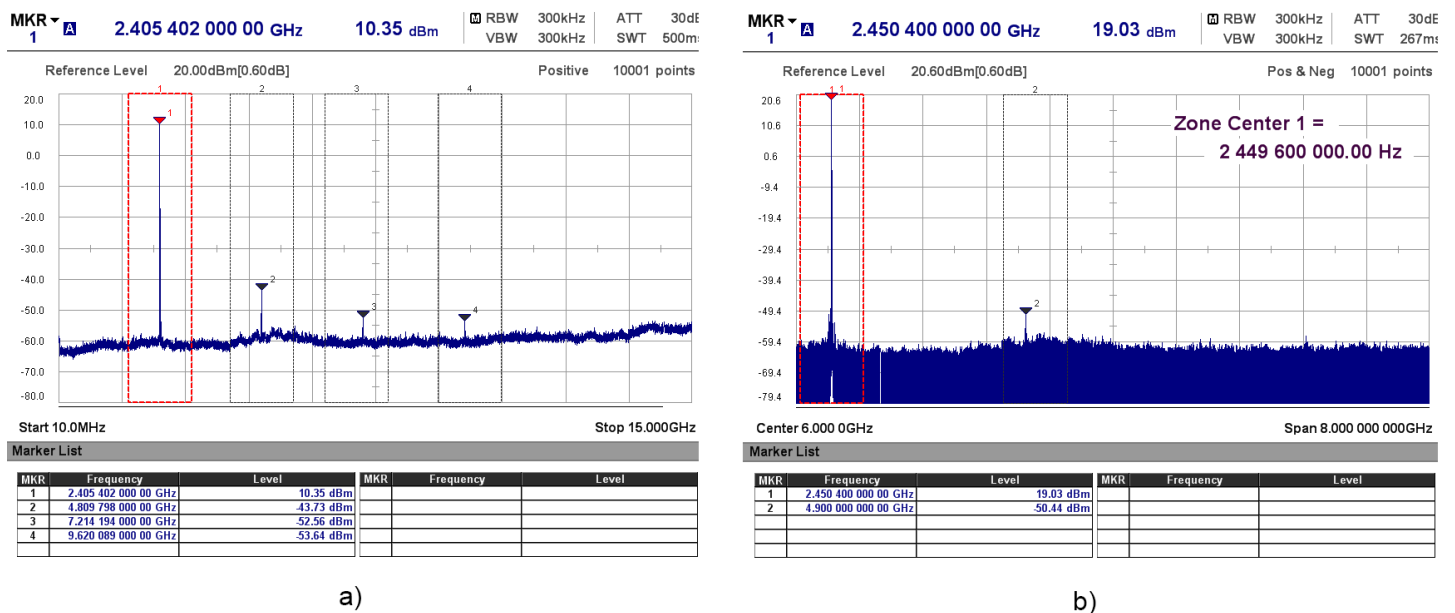
Figure 3.13. Measured Spectrum Plots of the Dual Band 7x7 mm EFR32 with (a) a Ladder Two-Element Match in 10 dBm Power State and (b) a Ladder Four-Element Match in 20 dBm Power State

4. Sensitivity Measurements

The sensitivity of the ladder two-element and four-element matches with the 7x7 mm dual band EFR32MG1 series is compared in the table below. Here, 20 byte long standard ZigBee® packages are used and 1 % PER sensitivity is shown. The measurements were made at room temperature. More sensitivity data can be found in Table 4.1 on page 16.

The applied setup includes the WSTK motherboard and the BRD41XX type development boards with different match types. The BRD41XX type boards apply a UFL RF connector and a UFL-SMA transition. These two elements cause approximately 0.5 dB additional attenuation. The RX sensitivity results shown are already compensated for by this error. The frequency is 2.405 GHz, i.e., the first Zigbee channel.

These RX test results are done on a very limited number of samples and are typical. Large test sample sensitivity results are only available for the 7x7 mm dual band package with a four-element lumped element match and are provided in the data sheet.

Table 4.1. Measured Sensitivities of the Ladder Two-Element and Four-Element Matchings Using Standard 20-Byte ZigBee Packages (After UFL Connector Compensation)

Package Type	Matching Type	Sensitivity [dBm]
7x7 mm, 48-pin, Dual Band	Ladder 2-Element	–99.1
	Ladder 4-Element	–98.5

The Rx test conclusions are as follows:

1. The Rx sensitivity variation resulting from the different package versions is lower than 1 dB and typically 0.5dB (see Appendix 2.1 Measured TX Emission).
2. The low-power reduced element matches have approximately 0.2–0.5 dB better sensitivity compared to their high power counterpart. In other words, two-element vs. four-element ladder match, or two-element minimum BOM vs. Tline minimum BOM match.

5. Conclusions

1. The minimal BOM Tline match has nearly the same fundamental power, harmonic levels, and current consumption as the four-element lumped element match, but with lower cost.
2. Both the ladder four-element match and the minimal BOM Tline match complies with the U.S. FCC (~ –41 dBm EIRP) and EU ETSI (~ –30 dBm EIRP) harmonic limits with large (>10 dB) margin up to power levels of ~ 20 dBm.
3. The two-element minimal BOM match is ETSI and FCC-compliant up to a 13 dBm power level, while the ladder two-element match complies up to 10 dBm.
4. Both the minimal BOM matches and the lumped element matches work well with the different package versions without significant effects on the output spectrum. The power variation is usually less than 0.5 dB, which is less than the chip-to-chip variation.
5. All matches with all EFR32 package versions have less than ~0.5 dB power variation across the entire 2.4 GHz band.
6. Typical total IC current consumption is ~30 mA at 10 dBm and ~135 mA at 20 dBm power levels. For power levels up to 13 dBm, Silicon Labs recommends that the PA be supplied from the internal dc-dc converter. The current does not vary excessively with different packages.
7. The cost of the minimal BOM matches is significantly lower because only one affordable, external multilayer type SMD inductor is used. The ladder matches are more expensive because film type inductors are used.
8. The sensitivity of the minimal BOM matches is the same or slightly better than that of their ladder counterparts.

6. References

1. Christian Gentili: Microwave Amplifiers and Oscillators, McGraw-Hill, 1987, ISBN0-07-022995-3
2. MuRata: http://www.murata.com/products/inductor/chip/feature/rf
3. http://wcalc.sourceforge.net/cgi-bin/coplanar.cgi(Copyright © 2001-2009 Dan McMahill.CGIC, copyright 1996, 1997, 1998, 1999, 2000 by Thomas Boutell and Boutell.Com, Inc.. Permission is granted to use CGIC in any application, commercial or noncommercial, at no cost.)

Appendix 1. PA Optimum Impedance Determination

The matching network should present an optimum impedance for the PA at the 2G4RF_IOP pin if a 50 Ω termination is applied at the antenna port. The optimum impedance depends on the power level and the package version. Fortunately, as shown below, they are quite close to each other, so one proper match is a good compromise for all versions and power levels. The optimum impedances are determined empirically by load-pull methods.

Figure A below shows the 2.4 GHz load-pull curves measured at the TX pin of the 7x7 mm, 48-pin 2.4 GHz single band EFR version with 20 dBm power setting. The optimum impedance point here is ~23.7+j7.1 Ω and is quite constant with frequency. For example, in the middle of the 2.4 GHz band (2.45 GHz), it is only very slightly off (~24.1 + j7.2 Ω).

Figure B below shows the measured 20 dBm, 2.4 GHz load pull data for the 7x7 mm, 48-pin dual band EFR version at the TX pin. Here, the optimum impedance is approximately 23 + j11.5 Ω. At 2.45 GHz, the optimum is slightly lower: ~21 + j10.4 Ω.

Figure C below shows the measured 20 dBm, 2.4 GHz load-pull data for the 5x5 mm, 32-pin single band EFR version at the TX pin. The optimum impedance here is approximately 20 + j14 Ω.
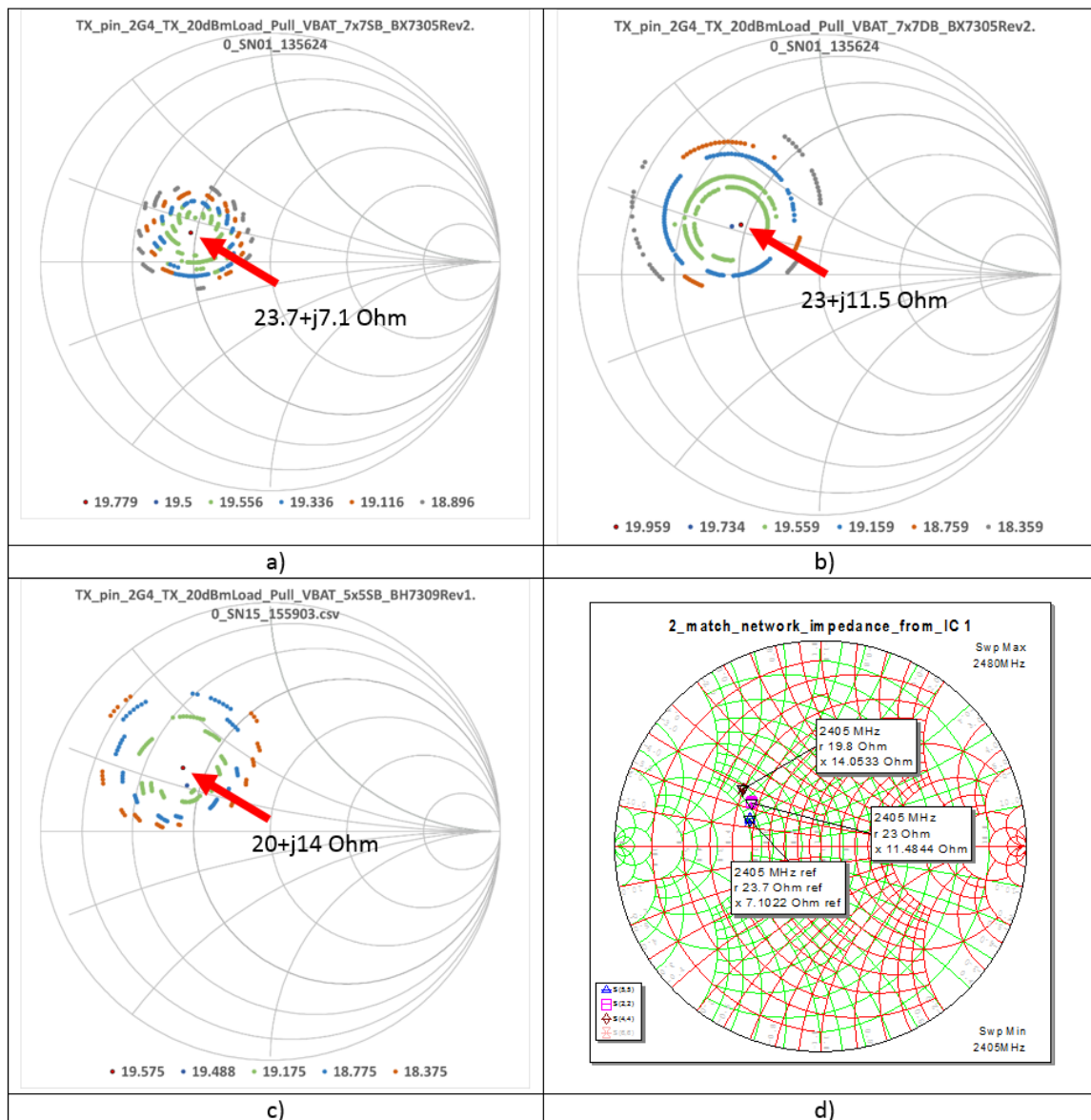

Figure 1.1. Load-Pull Curves and Optimum TX Load Impedances at the 2G4RF_IOP Pin of the Different EFR32 Package Versions: a) 7x7 mm Dual Band, b) 7x7 mm Single Band, c) 5x5 mm Single Band, d) Optimum TX Impedances Shown in One Smith Chart

The 2.4 GHz, 20 dBm level optimum termination impedances for the three EFR versions are shown together in D of the above figure. As only one common match will be used for all variations, a compromise must be found. Fortunately, the three optimum impedances are close to each other i.e., within the ~0.3 dB degradation load-pull circles if one chooses the middle point, so if a good compromise is

used, the power variation is less than 0.3 dB. According to this, the selected target impedance for further PA matching design is Zload_opt = ~23 + j11.5 Ω.

Further, the optimum impedance does not depend much on the power level. At a power level of 10 dBm, the optimum termination is only slightly off: Zload_opt_10dBm = ~20 + j10.6 Ω for the 7x7 mm dual band EFR version.

**Appendix 2. 2.4 GHz RF Network Schematics and Technical Data**

Four 2.4 GHz matching topologies are presented here:

- A ladder two-element LC match up to 10 dBm power levels
- A ladder four-element LCLC match up to 20 dBm power levels
- A low-cost hybrid type applying both discrete elements and a transmission line (LC-Tline-C) up to 20 dBm power levels
- A low-cost parallel LC match for up to 13 dBm power levels

The schematics of the above matches are given in Figures B1 through B4. All matches use GRM1555 type SMD capacitors from Murata. The ladder two-element and four-element matches use film-type LQP15MN series inductors, while the hybrid Tline and parallel LC matches apply low-cost, multilayer LQG15HS series inductors from Murata. The low-cost, hybrid-type LC with T-line and the parallel LC matches rely on the self resonance of the first shunt capacitor to enhance the 2nd harmonic suppression (while the parallel inductor resonates with that capacitor at the fundamental frequency), so care should be taken when utilizing a different part number or SMD size for that shunt capacitor. In that case, fine-tuning the parallel LC components might be required. It is also recommended to connect the GND pads of the parallel LC components on the same, solid GND pour side of the RF path. The ladder 2- and 4-element matches do not rely on self resonance of matching components, so in terms of component selection, they are more robust. In the figures, the 50 Ω antenna side load is denoted by Z_L, while the impedance shown at the IC side is denoted by Z_{IN}. The generator represents the PA.
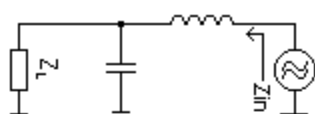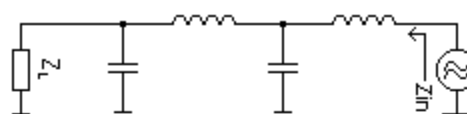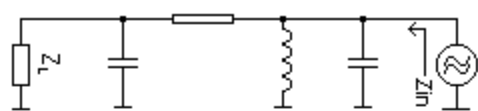

B1. Ladder 2-element LC Match Schematic
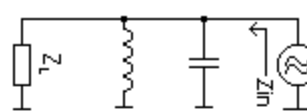

B2. Ladder 4-element LCLC Match Schematic

B3. Hybrid LC-Tline-C Match Schematic

B4. Parallel LC Match Schematic

Appendix 2.1 Measured TX Emission

The measured TX emissions with the 5 x 5 mm 32-pin package 2.4 GHz EFR version at 2.44 GHz are given in the table below. The tested boards apply a UFL RF connector and a UFL-SMA transition, which together cause approximately 0.5 dB additional attenuation. So, the real power delivered by the match is approximately 0.5 dB higher.

The TX power does not change much with the different package versions, the variation being lower than 0.5 dB.

Table 2.1. 2.44G TX Results, 5 x 5 mm 32-Pin Single Band Package

Match Type	Fundemental [dBm]	2nd Harmonic [dBm]	3rd Harmonic [dBm]	Cost	Notes
4-element ladder	18.7	−58.7	−66	High	ETSI, FCC Compliant with full power and large margin
2-element ladder	18.8	−21.4	−42	Low	Second harmonic strongly violates FCC at high power levels
2-element ladder @10 dBm	9.7	−42.8	−63.5	Low	Up to 10 dBm ETSI, FCC compliant
Hybrid LC-Tline-C	19.1	−51.5	−60	Low-Middle	ETSI, FCC Compliant with full power and large margin
Parallel LC @13 dBm	13.3	−58.9	−50.4	Very Low	Up to 13 dBm ETSI, FCC compliant

Power variations across the band are shown in the figure below. The (a), (b), and (c) figures show the ladder four-element match with the 7x7 mm, 48-pin dual band, 7x7 mm, 48-pin single band, and 5x5 mm, 32-pin single band versions, respectively. The last figure (d) shows the Tline match variation. In all cases, the variation across the band is less than 0.5 dB. The second and third harmonic variations are also shown. They are far below the ETSI (~−30 dBm) and FCC (~−41 dBm) limits in all cases.
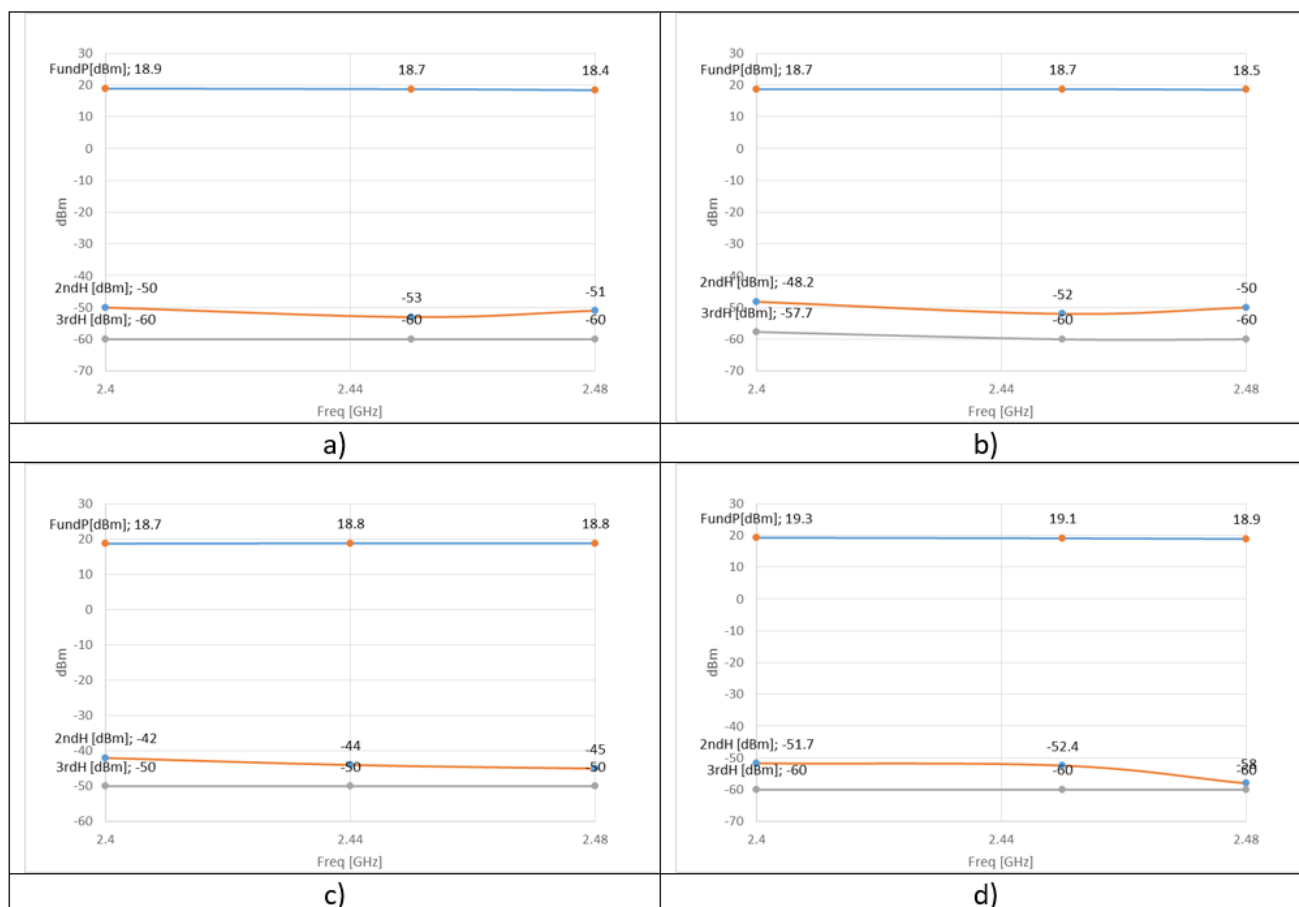
Figure 2.1. Power Variations across the Band: (a), (b), (c) Ladder Four-Element Match with the Three EFR Package Versions (d) T-line Match with 7x7 mm Dual Band EFR Version

Appendix 2.2 RX Sensitivity

The sensitivities of the different matches are compared in the table below. Here, 20 byte long standard ZigBee packages are used, and 1 % PER sensitivity is shown. The measurements are made at room temperature.

The tested EFR32MG1 series boards apply a UFL RF connector and a UFL-SMA transition with extra attenuation of 0.5 dB. The RX sensitivity results shown are already compensated.

The frequency is 2.405 GHz (i.e., the first Zigbee channel). These RX test results are done on a limited number of samples. High quantity sensitivity results are available for the ladder four-element match only in the data sheet.

Table 2.2. Measured Sensitivities with Different Matching Types and EFR32 Package Versions Using Standard 20 byte ZigBee Packages, after UFL Connector Compensation

Package Type	ApMatching Type	Sensitivity [dBm]
7x7 mm, 48-pin, dual band	Ladder 2-element	–99.1
	Ladder 4-element	–98.5
	Hybrid T-line	–98.8
	parallel LC min. BOM	–99.3
7x7 mm, 48-pin, single band	Ladder 2-element	–98.6
	Ladder 4-element	–98.5
	Hybrid T-line	–99.1
	parallel LC min. BOM	–99.3
5x5 mm, 32-pin, single band	Ladder 2-element	–98.6
	Ladder 4-element	–98.1
	Hybrid T-line	–98.8
	Parallel LC min BOM	–99

Appendix 2.3 Conclusions

1. Both the ladder four-element lumped match and the hybrid T-line match comply with the U.S. FCC (~–41 dBm EIRP) and EU ETSI (~–30 dBm EIRP) harmonic limits with large (>10 dB) margin up to ~ 20 dBm power levels.
2. The LC parallel minimal BOM match is ETSI and FCC compliant up to 13 dBm power level, while the ladder two-element lumped element match complies up to 10 dBm.
3. Due to the applied, inexpensive, multilayer SMD inductor, the LC parallel minimal BOM match and the hybrid T-line match are significantly cheaper than the ladder two-element and four-element matches, which use more expensive film-type inductors.
4. All matches works well with the different package versions without significant effects on the emitted spectra. The power variation is usually less than 0.5 dB.
5. All matches with all EFR32 package versions has less than ~0.5 dB power variation across the whole 2.4 GHz band.
6. Typical total IC current consumption is ~30 mA at 10 dBm and ~135 mA at 20 dBm power level. For up to 13 dBm power levels, Silicon Laboratories recommends the PA be supplied from the internal dc-dc converter. The current does not vary excessively with the different matches and packages.
7. The hybrid T-line match has a slightly higher fundamental power and better sensitivity compared to the ladder four-element match.
8. The parallel LC match has slightly higher fundamental power with the same reduced power setting and better sensitivity compared to the ladder two-element match.
9. Rx sensitivity variation due to the different package versions is lower than 0.5 dB
10. Rx sensitivity variation across the 2.4 GHz band is lower than 0.5 dB.

Appendix 3. 2.4 GHz Ladder 4-element RF Matching Design Steps

After the optimum termination impedance for the 2G4RF_IOP RF port is determined as Zload_opt = 23+j11.5 Ω in Chapter 2.1 the ladder four-element 2.4 GHz RF matching design for EFR32 chip has the following steps remaining:

1. Initial design with ideal, loss free elements and without PCB parasitics.
2. Design with parasitics using the initial design of the previous step as a starting point. The parasitics of the SMD elements and the PCB have a significant effect at 2.4 GHz, so tuning/optimization of the design is required. Here, an optional EM simulation can be performed for increased accuracy.
3. Bench testing and tuning.

Appendix 3.1 Initial Design with Ideal, Loss-free Elements

In this step, the ideal skeleton design of the ladder four-element match is shown with losses and parasitic-free discretes and without PCB parasitics.

The ladder four-element match is devoted to 20 dBm applications, so the load impedance that the match should show at the IC side is: Zload_opt = ~23+j11.5 Ω if the antenna side is terminated by 50 Ω.

A ladder four-element match can be designed in two ways: using the ladder two-element match with an additional two- or three-element filter section (for matches with an additional 3-element PI low-pass filter, the shunt capacitor of the 2-element ladder match is combined with the first shunt capacitor of the PI LPF; see Figure 3.1 Element Match PCB Layout with Good 2G4RF_ION Grounding on page 4) or using a four-element matching + filter combo (see Figure 3.2 Basic Two-Element Matching Techniques with Ideal Lumped Elements on page 7). In the latter case, all four elements take part in the impedance match, and, thus, it is less sensitive to element spreading. Additionally, the (reactive) elements realize less phase shift, so the impedance locus varies closer to the Smith chart center, which means a lower Q route. As a result, the loss of elements has less influence. Unfortunately, due to having multiple stages, the overall insertion loss can be higher with four elements. Possible ladder four-element designs with ideal elements are shown in the figures below. The antenna side is denoted by the 50 Ω ZL load impedance while the PA side impedance is denoted by Zin.

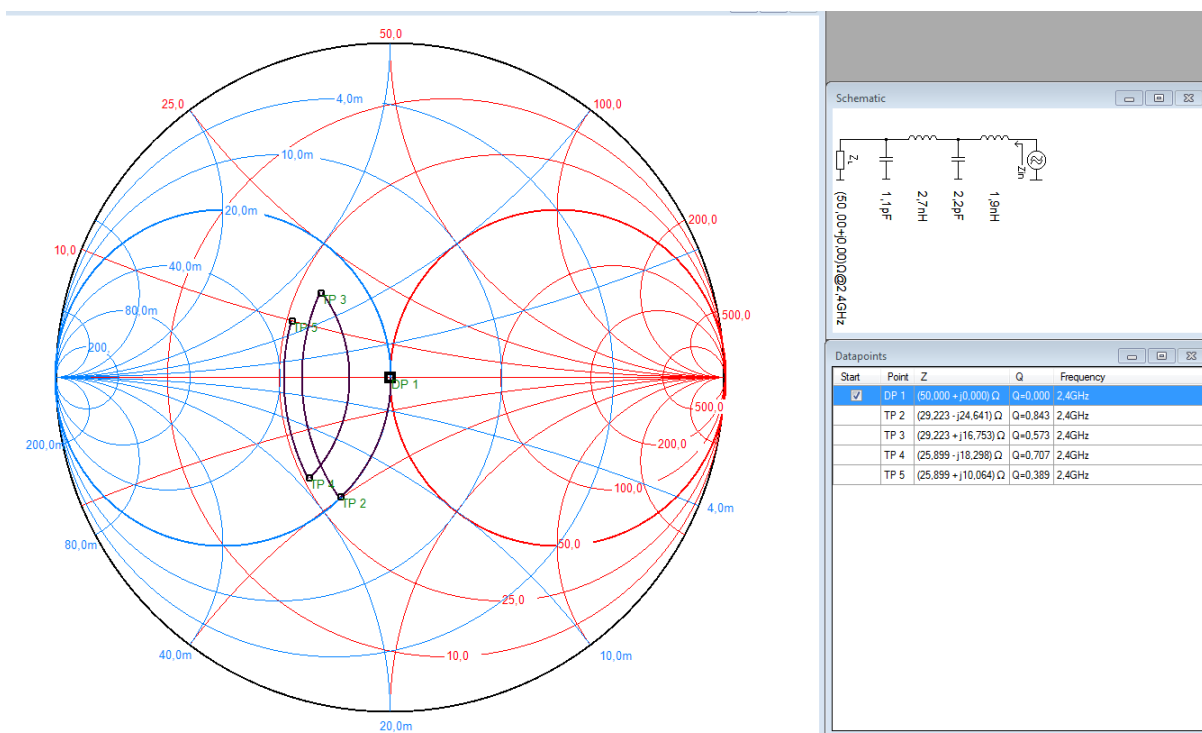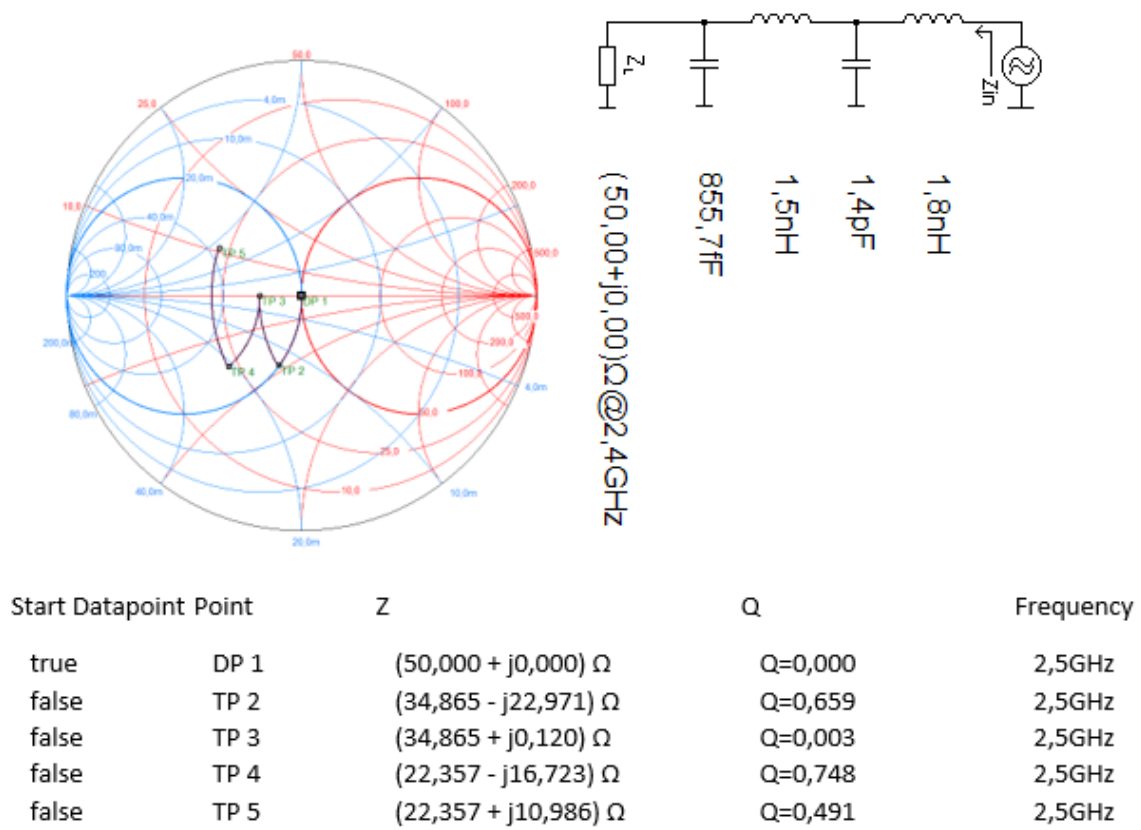**Figure 3.1. Basic Ladder Four-Element Matching Technique with Ideal Lumped Elements #1**

Start Datapoint	Point	Z	Q	Frequency
true	DP 1	(50,000 + j0,000) Ω	Q=0,000	2,5GHz
false	TP 2	(34,865 - j22,971) Ω	Q=0,659	2,5GHz
false	TP 3	(34,865 + j0,120) Ω	Q=0,003	2,5GHz
false	TP 4	(22,357 - j16,723) Ω	Q=0,748	2,5GHz
false	TP 5	(22,357 + j10,986) Ω	Q=0,491	2,5GHz

Figure 3.2. Basic Ladder Four-Element Matching Technique with Ideal Lumped Elements #2

Appendix 3.2 Design with Parasitics

In this step, the PCB and element parasitics and losses are introduced. As with the ladder two-element match design example, the same 0402 SMD series from Murata (LQP15MN film type inductors and GRM1555 type capacitors) is used with the equivalent circuits given in Figure 3.5 Reference Planes with Real SMD Elements on page 10. The applied layout is also the same, and, thus, the PCB parasitics shown in Figure 3.6 Estimation of PCB Layout Parasitics on page 10. are used. The figure below shows the tuned ladder four-element match locus and schematic with parasitics. The endpoint at the IC side (denoted by TP11 in the Smith chart and by Zin in the schematic) is very close to the targeted optimum (Zload_opt = ~23 + j11.5 Ω).

Start Datapoint	Point	Z	Q	Frequency
true	DP 1	(50,000 + j0,000) Ω	Q=0,000	2,5GHz
false	TP 2	(48,996 - j7,014) Ω	Q=0,143	2,5GHz
false	TP 3	(25,603 - j24,798) Ω	Q=0,969	2,5GHz
false	TP 4	(25,603 - j22,027) Ω	Q=0,860	2,5GHz
false	TP 5	(27,880 + j27,968) Ω	Q=1,003	2,5GHz
false	TP 6	(32,699 + j27,565) Ω	Q=0,843	2,5GHz
false	TP 7	(23,376 - j26,650) Ω	Q=1,140	2,5GHz
false	TP 8	(23,376 - j23,880) Ω	Q=1,022	2,5GHz
false	TP 9	(24,144 + j5,173) Ω	Q=0,214	2,5GHz
false	TP 10	(24,754 + j3,514) Ω	Q=0,142	2,5GHz
false	TP 11	(24,754 + j10,287) Ω	Q=0,416	2,5GHz

Figure 3.3. Ladder 4-Element Match Tuning with SMD Element and PCB Parasitics

Optionally, EM simulations can be done for better accuracy, but the SMD element values of the schematic of Figure C2 is already a good starting point for the bench tuning.

Appendix 3.3 Bench Measurements and Tuning

Using the same test setup as in the ladder two-element match (shown in Figure 2.11 in Chapter 2.6), one can tune the macth and acquire the measured S11 and S21 (transfer) characteristics. They are given in the figure below. As expected, second and third harmonic suppression is ~40 dB, i.e., much stronger than with the two-element match. The final ladder four-element match element values are given in the table below.
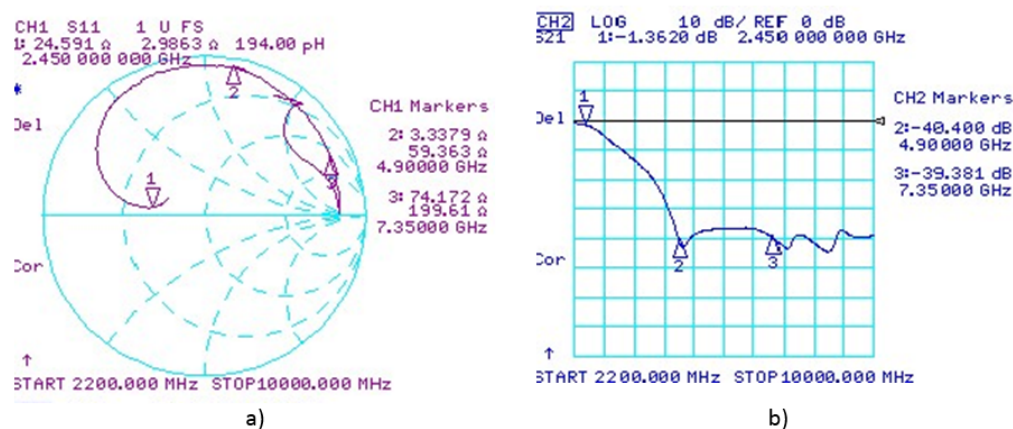
a)

Figure 3.4. Ladder 4-Element Match Design Bench Test Results with SMD Element and PCB Parasitics

Table 3.1. Final SMD Values for the Ladder Four-Element Match

Ladder Four-Element Matching Network				
Schematic reference designator	Component value	Tolerance	Part Number	Manufacturer
LH0	1.8 nH	±0.1 nH	LQP15MN1N8B02	Murata
LH1	3.0 nH	±0.1 nH	LQP15MN3N0B02	Murata
CH0	2.0 pF	±0.1 pF	GRM1555C1H2R0BA01D	Murata
CH1	1.0 pF	±0.1 pF	GRM1555C1H1R0BA01D	Murata

Measured RX sensitivites are given in Table 4.1 Measured Sensitivities of the Ladder Two-Element and Four-Element Matchings Using Standard 20-Byte ZigBee Packages (After UFL Connector Compensation) on page 16.

Appendix 4. Transmission Line (Tline) Match for Minimal BOM Solutions (U.S. Patent US9780757B1)

An alternative low-cost matching technique involves replacing some lumped elements with distributed elements, which saves the cost of the deleted SMD elements. In this regard, replacing the more expensive high-Q series inductors is desirable. The second reason for eliminating or replacing the higher-priced high-Q series inductors is the additional losses they introduce, especially when they are used in the series arm of a K-ladder filter configuration.

The Q of the SMD capacitors is much higher, and their price is much lower, which, in turn, renders their replacement less important.

Together with the optimized Vdd and dc-dc converter filtering, this matching concept is used in the low-cost, minimal BOM 2.4 GHz reference designs, which can be found on the Silicon Labs Website and described in detail in AN933.1: EFR32 Series 1 Minimal BOM.

SMD capacitors have an inherent series self-resonance as indicated by the equivalent circuit described in 3.4 Design with Parasitics and Losses. The self-resonance frequency is determined by the parasitic inductance. In other words, by the internal electrode structure and geometry. As the structure and geometry are quite fixed, the self-resonant frequency is also quite stable. Variation is caused mainly by the capacitance change and, therefore, has the same spreading properties.

As a result of the low impedance of the series self-resonance, a parallel-connected capacitor behaves as a second order notch filter around its resonant frequency. If choosing a cap value as such, the self-resonance falls close to the most critical harmonic frequency (usually the second) and an additional 25–35 dB suppression can be achieved. Figure 4.1 Effect of a Shunt SMD Capacitor Self-Resonating Close to the Second Harmonic on page 30 part a. shows the basic concept of this approach with one 2 pF SMD capacitor (S-parameters of the GRM155 type, 0402 size SMD capacitor from Murata is used here) denoted by C0. In the simulation stage, shown in Figure 4.1 Effect of a Shunt SMD Capacitor Self-Resonating Close to the Second Harmonic on page 30 part a., the L0 and C1 elements are disabled and have no effect on the results. Also, the effect of the short series transmission line to the 50 Ω port is negligible compared to the impact of C0.
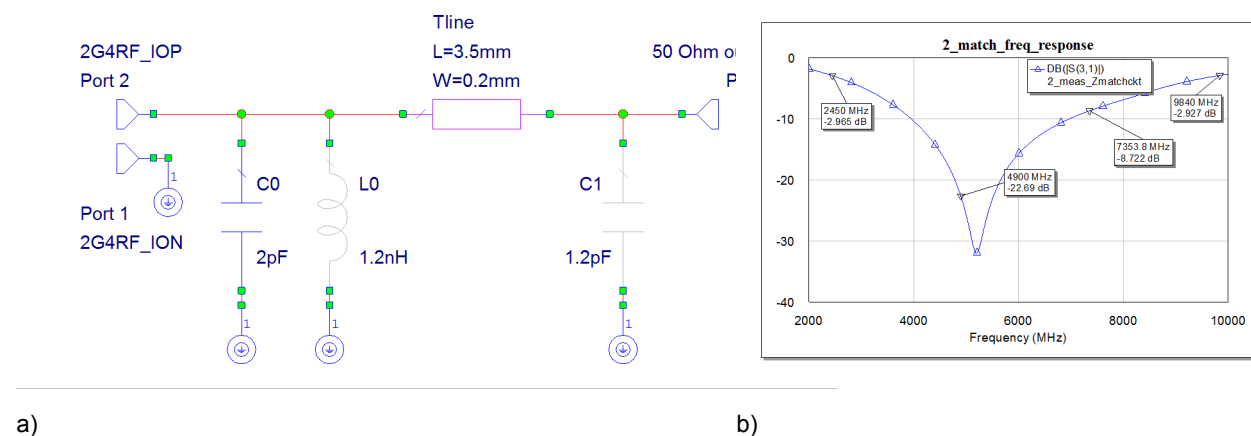

a)   b)

Figure 4.1. Effect of a Shunt SMD Capacitor Self-Resonating Close to the Second Harmonic

The transfer characteristic is shown in Figure 4.1 Effect of a Shunt SMD Capacitor Self-Resonating Close to the Second Harmonic on page 30 part b. As shown, the capacitive self-resonance causes significant attenuation at the second harmonic frequency but has some attenuation at the third harmonic frequency as well. Unfortunately, as a result of the discrete value of the real capacitors (E12 or E24 series), the resonant frequency usually does not fall exactly into the critical harmonic frequency. For example, with the next available value (2.2 pF), the resonance would already shift significantly below the second harmonic frequency. Note that, in the setup of Figure 4.1 Effect of a Shunt SMD Capacitor Self-Resonating Close to the Second Harmonic on page 30 part a., the capacitor is connected to the ground through a via hole, which introduces an additional series parallel inductance and, therefore, detunes the C0 self-resonance to a lower frequency. Therefore, the via properties, such as diameter, dielectric thickness, etc., and the trace variation between the via and the C0 capacitor give some limited flexibility to tune down the resonant frequency if it is required.

Unfortunately, because of the shunt effect of the C0, the application of the parallel C0 capacitor causes the insertion loss at the fundamental frequency to become unacceptably high (~3 dB), which is a critical issue. To avoid this issue, an inductor (denoted by L0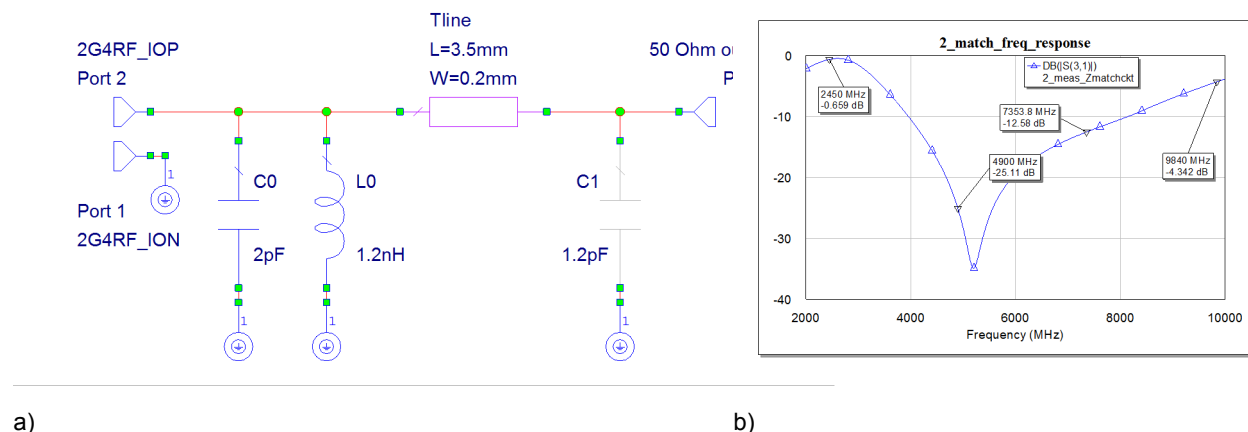), parallel with the C0 capacitor, is introduced as shown in Figure 4.2 Effect of a Shunt Cap Self-Resonating at the Second Harmonic Together with a Parallel SMD Inductor Resonating with the Shunt Cap at the Fundamental on page 31 part a. Note that the C1 capacitor is still disabled in this simulation. The formed L0-C0 parallel resonator is tuned to resonate and show high impedance around the fundamental frequency; in other words, to be practically invisible. As a result, the introduction of L0 drastically reduces the insertion loss from ~3 dB to ~0.5 dB at the fundamental, as shown by the leftmost marker in Figure 4.2 Effect of a Shunt Cap Self-Resonating at the Second Harmonic Together with a Parallel SMD Inductor Resonating with the Shunt Cap at the Fundamental on page 31 part b. In this simulation, the S-parameter file of a low-cost multilayer type (LQG series from Murata) 1.2 nH SMD inductor is used.

a)   b)

Figure 4.2. Effect of a Shunt Cap Self-Resonating at the Second Harmonic Together with a Parallel SMD Inductor Resonating with the Shunt Cap at the Fundamental

The circuit shown in part A of the above figure has a moderate attenuation at the third harmonic frequency. Up to ~13 dBm output power level, this limited third harmonic attenuation is enough for the EFR32 to comply with the ETSI and FCC standards. Therefore, a low BOM two-element match formed by the L0-C0 elements can be used because the transmission line is not required for operation. With this match, the impedance at the TX pin is usually not the optimum, but rather close to 50 Ω. Fortunately, the L0-C0 ratio variation allows for limited impedance tuning. Even if some residual impedance does occur, the slight reduction of power can be easily compensated for by higher power state settings with a minimal increase in total IC current at low power levels.

However, at higher power levels, EFR32 requires more harmonic suppression. For example, at a 20 dBm output power level, at least 30 dB third harmonic attenuation is required to comply with the 41.2 dBm limit of the US FCC standard. To resolve this issue, introduce a second parallel capacitor denoted by C1, which has the self-resonance close to the third harmonic frequency. Unfortunately, the second parallel capacitor mistunes the fundamental C0-L0 parallel resonator if it is connected directly parallel to it. Besides, the C1 alone has a shunt effect, which again increases the insertion loss at the fundamental frequency. To resolve both issues, separate the C1 capacitor either by a series inductor or a transmission line to form a ladder network. Now, a series transmission line is used becacuse of the higher cost and higher loss of applying a series inductor.

However, separation is not the only function of the transmission line. Because the C0-L0 parallel resonant circuit is invisible at the fundamental frequency, the series transmission line together with the C1 capacitor should also generate the optimum impedance at the TX pin. As mentioned previously, the L0-C0 can be tuned in a limited fashion to get the right impedance. However, the main tuning element is the transmission line because of the C0 and the C1 capacitor value variation limitation, which dictates that self-resonant frequencies should be close to the critical harmonics. The transmission line is only several mm long, which is much shorter than the wavelength at the fundamental frequency and can, therefore, be modeled as a lumped inductor with some parasitic parallel capacitance. The value of C1 adds directly to this parasitic cap. Usually, the width of the transmission line has to be decreased close to the technological minimum (~0.2 mm) to have sufficiently high inductance and to minimize the parasitic cap effect beside the C1. Because the width is more or less fixed, the residual main tuning possibility is the length of the transmission line.

The matching network with 3.5 mm long and 0.2 mm wide transmission line and with 0.8 pF C1 value is shown in part A of the figure below. Part B shows the transfer characteristic. The third harmonic is efficiently suppressed with the 0.8 pF C1 value. However, the input impedance at the TX pin (at Port 2 in the schematic) is quite far from the optimum impedance as shown in part A. Here, some tuning is required to shift the impedance closer to the targeted 23+j11.5 ohm. This can be done either by varying C1 and L0–C0 slightly or by tuning the transmission line length. For example, with a C0 of 2 pF, L0 of 1.2 nH and C1 of 0.9 pF and with 5 mm long transmission line, the impedance is quite close to the optimum (see with good transfer characteristic.

Based on the above experiences, the design steps of the transmission line match are as follows:

1. Choose a C1 capacitor value, which has its self-resonance, good suppression, and is nearly at the third harmonic. Additional layout series parasitic inductances, such as via or trace inductance, shift down the resonant frequency.

2. Choose a transmission line with 0.2–0.25 mm width and with a length, which together with C1 tunes nearly the optimum impedance (~23+j11.5 ohm) at the TX pin.

3. Choose a C0 value that has its self-resonance close to the second harmonic. Again, the series parasitic inductances, such as via or trace, of the layout decreases the resonant frequency.

4. Choose a parallel L0 value that resonates with the C0 at the fundamental frequency and provides a low insertion loss. Slight tuning of L0 can further improve the impedance optimization.
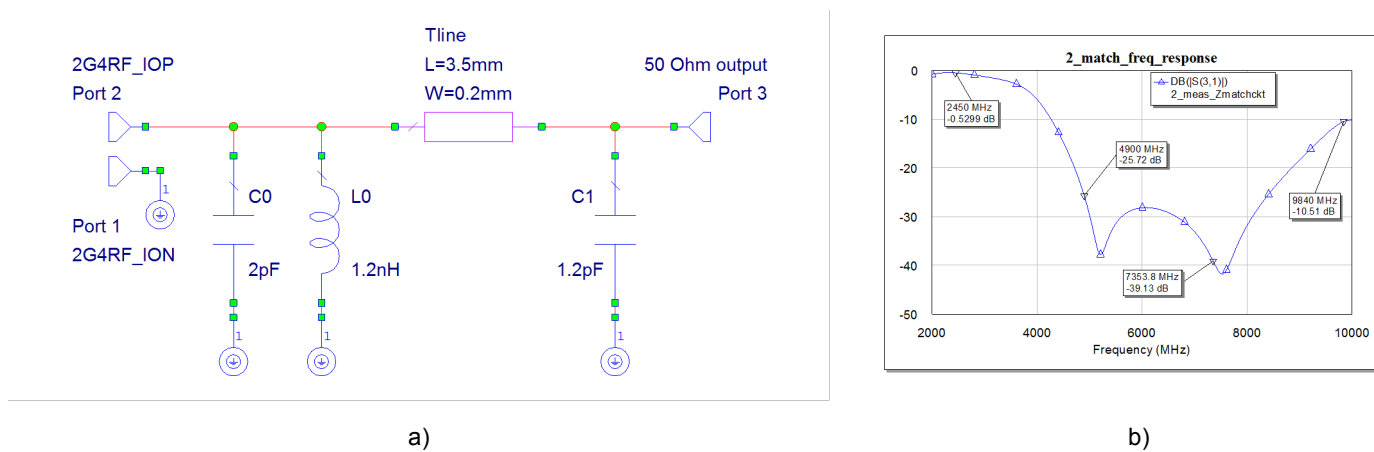
a)

b)

Figure 4.3. The Final Tline Match Concept with Real SMD and Transmission Line Elements (PCB Parasitics are Neglected)
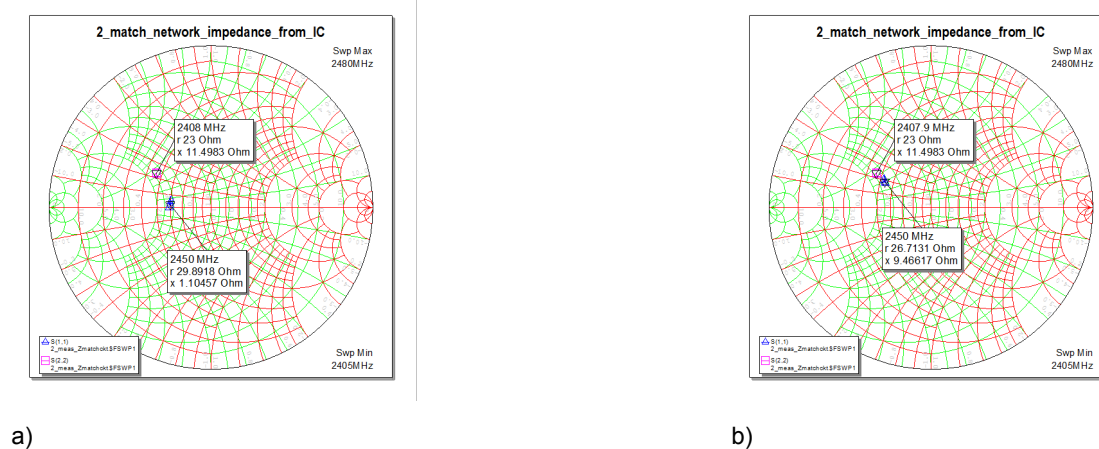

a)

b)

Figure 4.4. Impedances of Differently Tuned Tline Matches on the 2G4RF_IOP Pins

Appendix 4.1 EM Simulations of the Tline Match

More accurate tuning can be done with EM simulations. Figure 4.5 EM Simulation of the Tline Match on page 33 part a. shows the EM simulated layout with 3.5 mm long and 0.2 mm wide transmission line. As the first design step, the C1 capacitor with 1 pF value (Murata GRM155 series S-parameter file) is connected between Ports 7 and 8 as shown in part B of the following figure.

a)   b)
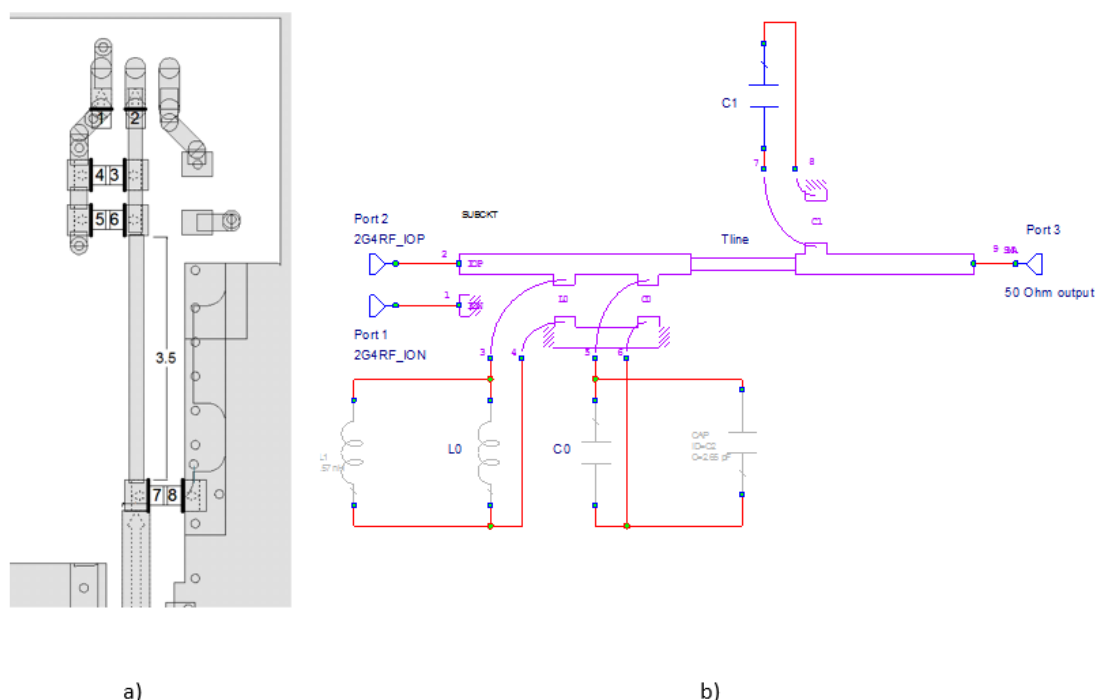
Figure 4.5. EM Simulation of the Tline Match

The simulated transfer characteristic and the impedance at the TX pin (Port 2 in the layout) is shown in Figure 4.6 Steps 1 and 2 of the Design: Setting C1 to Have Self-Resonance at the Third Harmonic and Setting the Tline Length to Get Good Impedance at the 2G4RF_IOP Pin on page 34. The impedance falls very close to the target, which ensures that the Tline length is properly tuned and makes Step 2 unnecessary.

For Step 3, a proper C0 value is chosen to suppress the second harmonic (4.9 GHz). This C0 value is approximately 2.2 pF (using the S-parameter data given by the vendor).

For Step 4, a proper L0, connected between Ports 5 and 6, as shown in Figure 4.5 EM Simulation of the Tline Match on page 33 part a., value is chosen, which resonates with C0 close to the fundamental frequency, results in low insertion loss, and, if possible, also tunes the impedance further towards the optimum. The best L0 value found is 1.2 nH (using the LQG15HS type S-parameters from Murata) but, as can be seen in Figure 4.6 Steps 1 and 2 of the Design: Setting C1 to Have Self-Resonance at the Third Harmonic and Setting the Tline Length to Get Good Impedance at the 2G4RF_IOP Pin on page 34 part b., due to the L0 parasitics the impedance is not exactly optimal. Unfortunately, the LQG series inductors are available only in E12 series discrete values. As a result, the optimum impedance usually cannot be fully reached, and some deviation remains. As mentioned before, some fine tuning can be done by inserting a proper series parasitic inductance, such as a proper short trace between the inductor and the ground metal. However, the deviation from the optimum impedance is so small that the power degradation is negligible (from the load-pull curves) and, as a result, fine tuning is not required
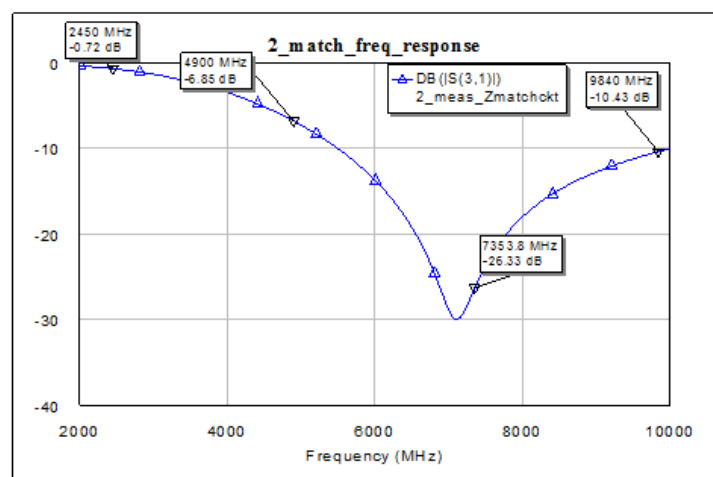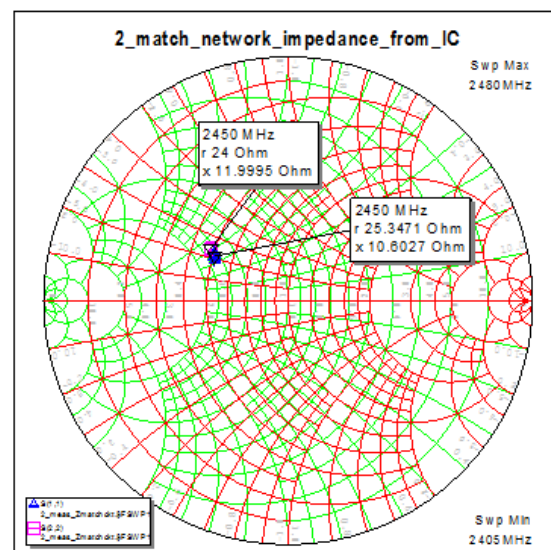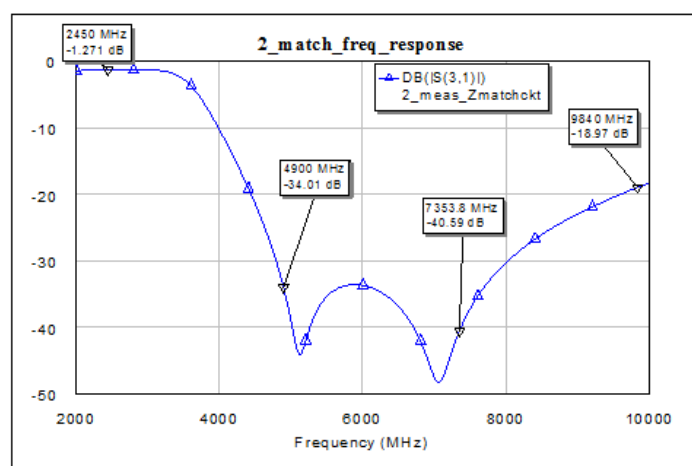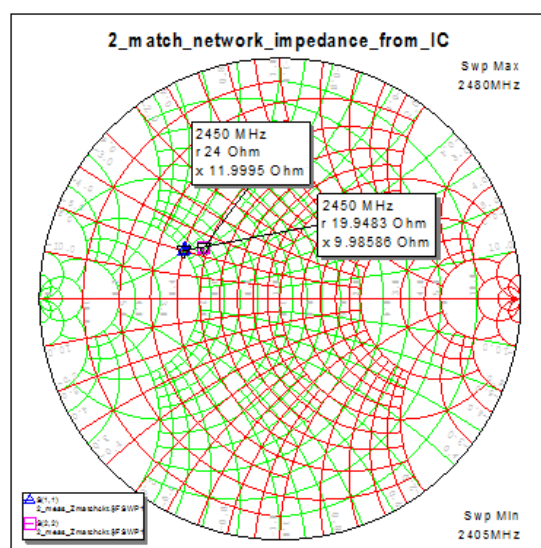
Figure 4.6. Steps 1 and 2 of the Design: Setting C1 to Have Self-Resonance at the Third Harmonic and Setting the Tline Length to Get Good Impedance at the 2G4RF_IOP Pin

Figure 4.7. Characteristic of the Final EM Tuned Tline Match

Appendix 4.2 Bench Measurements and Tuning

The impedance at the TX pin and the transfer characteristic are measured in the same way as the pure lumped element ladder matches. See 3.5 Bench Tuning and Measured Results. Unfortunately, the EM simulated and measured results are different. Typically, the C0 and C1 self-resonances are at higher frequencies in real life and the harmonic suppression is not high enough. With increased C0 and C1 values the self-resonances can be shifted down close to the 2nd and 3rd harmonic frequencies. The optimum C0 and C1 values here are around 3–3.3 pF and 1.1–1.2 pF, respectively. Additionally, a higher L0 is needed to have the L0-C0 parallel resonance, which means that the insertion loss needs to be minimum at the fundamental frequency

Figure 4.8 Measured Characteristic of the Tline Match Given in Above Table on page 35 shows the measured impedance and the transfer characteristic of the bench tuned match with C1=1.2 pF, C0=3.3 pF, L0=1.5 nH, and Tline length=3.5 mm. The applied SMD elements are listed in Table 4.1 Element Values of the Final Bench Tuned Tline Match with 3.5 mm Tline Length on page 35. For the two element low BOM match where no transmission line and no C1 capacitor is applied, the L0 and C0 values are identical to the values given for the Tline match.

Table 4.1. Element Values of the Final Bench Tuned Tline Match with 3.5 mm Tline Length

Tline Matching Network				
Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
L0	1.5 nH	±0.1 nH	LQG15HS1N5B02	Murata
C0	3.3 pF	±0.1 pF	GRM1555C1H3R3BA01	Murata
C1	1.2 pF	±0.1 pF	GRM1555C1H1R2BA01	Murata

As shown in part A of the figure below, the impedance at the fundamental frequency is 20 + j12 Ω, which is close to the optimum 23 + j11.5 Ω. Also, second and third harmonic suppression is around or higher than 40 dB, which yields FCC compliant harmonic levels with large margin at a 50 Ω termination. Note that the optimum value of the parallel C0 and C1 capacitors depends on the quality of their grounding. In the Silicon Labs reference layout, the parasitics of the ground connections are minimized by connecting the discretes directly to a large ground metal at the top layer and to the unified inner ground layer beneath it with many parallel vias. Silicon Labs recommends applying the same good RF grounding in customer layouts. Otherwise, slight C0 and C1 value variation/tuning may be necessary with the L0.
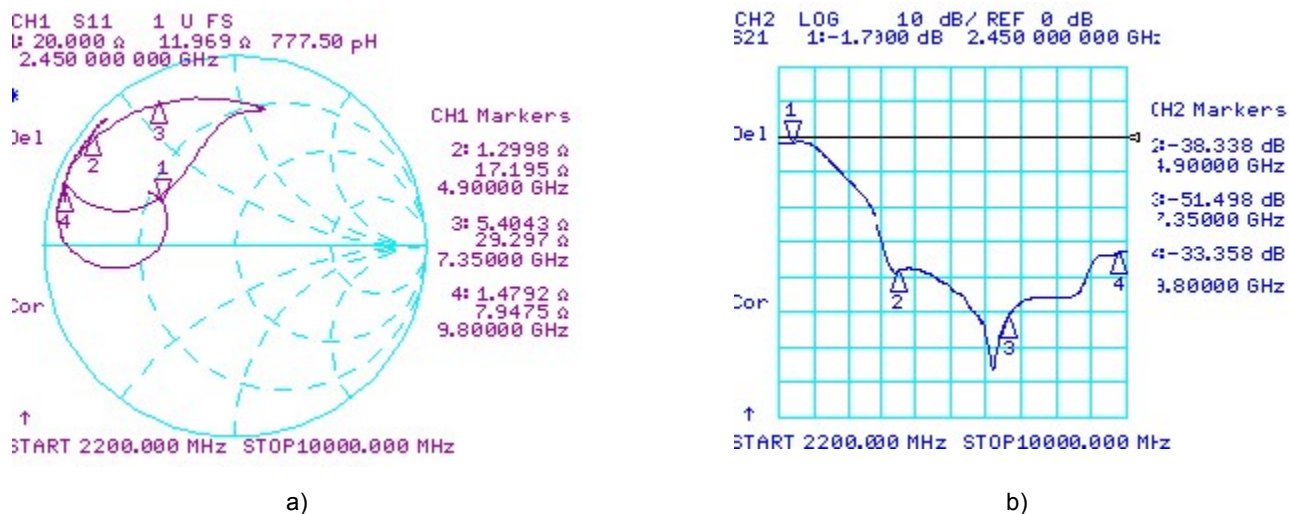

a)

b)

Figure 4.8. Measured Characteristic of the Tline Match Given in Above Table

Typical measured 10 dBm (with PAVDD fed from DCDC) and 20 dBm spectrum plots with the 7x7 mm 48 pin dual band EFR32 version, denoted by BRD4151A, in the middle of the band, 2.45 GHz, are shown in Figure 4.11 Measured Spectrum Plots of the Dual Band EFR32 Version (BRD4151A) with Tline Match at a) 10 dBm Power Level (DCDC on) and with 20 dBm Power Level on page 37, respectively. Measured 20 dBm, middle band Tline match spectrum plots with the 7x7 mm 48 pin, denoted by BRD4101A, and 5x5 mm 32 pin, denoted by BRD4111A, 2.4 GHz single band EFR32 versions are shown in Figure 4.12 Measured Spectrum Plots of the Single Band EFR32 Versions with Tline Match at 20 dBm Power State a) 7x7 mm (BRD4101A), b) 5x5 mm (BRD4111A) on page 37, respectively.

The BRD41XX type boards applies the UFL RF connector and a UFL-SMA transition. These two elements cause approximately 0.5 dB additional attenuation. Therefore, the real delivered power is approximately 0.5 dB higher.

The main conclusions are as follows:
1. The Tline match has nearly the same fundamental power, harmonic levels, and current consumption as the ladder four-element lumped element match (see 3.5 Bench Tuning and Measured Results), but with a lower cost.
2. The Tline match complies with the U.S. FCC (-41.2 dBm EIRP) and EU ETSI (-30 dBm EIRP) harmonic limits with large (>10 dB) margin at ~ 20 dBm power levels and below.
3. Different EFR32 package versions can be operated with the same Tline match without a significant effect on the output spectrum. The difference is usually less than 0.5 dB, which is less than the chip-to-chip variation.

The 2.4 GHz Tline matches are measured on eight boards with each EFR32 package versions to have more reliable test data. Figure 4.9 Measured Results of the Bench Tuned 2.4 GHz Tline Matches in TX Mode with Different EFR32 Packages on page 36 shows the test results on maximum power state. After compensating the UFL connector+SMA transition loss, the real delivered power is approximately 0.5dB higher.

BRD4151A, PAVDD=3.3V, 20dBm power state				BRD4101A, PAVDD=3.3V, 20dBm power state				BRD4111A, PAVDD=3.3V, 20dBm power state			
Pout [dBM]	2nd [dBM]	3rd [dBm]	I [mA]	Pout [dBM]	2nd [dBM]	3rd [dBM]	I [mA]	Pout [dBM]	2nd [dBM]	3rd [dBM]	I [mA]
18.95	-54	-54	127.5	19.15	-50	-55	134.3	19.1	-52	-60	127.4
18.95	-56	-60	129.5	18.85	-55	-55	134.2	19.5	-51	-60	134.1
18.9	-55	-55	126.2	19.3	-54	-54	137.3	19.2	-49	-60	129.3
19.05	-54	-58	131	19.4	-54	-55	136	19.2	-52	-60	129.6
19.3	-53	-55	131.3	19.3	-50	-55	131.6	19.2	-48	-60	131.2
19.25	-53	-60	130.9	19.15	-54	-55	133.5	19.5	-50	-60	135
19.1	-53	-55	143.3	19.2	-54	-55	132.3	18.9	-60	-60	127.2
19	-52	-55	128.9	19.35	-50	-55	135	19.2	-50	-60	131.5
19.1	**-53.8**	**-56.5**	**131.1**	**19.2**	**-52.6**	**-54.9**	**134.3**	**19.2**	**-51.5**	**-60.0**	**130.7**

Figure 4.9. Measured Results of the Bench Tuned 2.4 GHz Tline Matches in TX Mode with Different EFR32 Packages

The fundamental power second and third harmonic variations across the 2.4–2.48 GHz band are also shown in Appendix 1. According to Appendix 1. PA Optimum Impedance Determination, the fundamental variation is less than 0.5 dB, and the harmonics are far below the regulation (ETSI and FCC) limits.

The minimal BOM two-element match (with L0-C0 parallel resonator pair) for low-power regimes (<+13 dBm) are also measured on eight boards for each package versions (7x7 mm 48-pin dual band BRD4152A, 7x7 mm 48-pin 2.4 GHz BRD4102A, 5x5 mm 32-pin 2.4 GHz BRD4112A). Here, the PA is fed from 1.8 V generated by the internal dc-dc converter. Figure 4.10 Measured Results of the 2.4 GHZ Minimal BOM Low-Power Matches in TX Mode with Different EFR32 Packages on page 36 the ~13 sdBm results at middle band (2.45 GHz).

| BRD4152A, PAVDD=1.8V DCDC, 13dBm				BRD4102A, PAVDD=1.8V DCDC, 13dBm				BRD4112A, PAVDD=1.8V DCDC, 13dBm			
Pout [dBm]	2nd [dBm]	3rd [dBm]	I [mA]	Pout [dBm]	2nd [dBm]	3rd [dBm]	I [mA]	Pout [dBm]	2nd [dBm]	3rd [dBm]	I [mA]
12.8	-53	-48	49.9	13.2	-64	-45	49.9	13.45	-60	-47	50.4
13.1	-56	-47	49.7	13.4	-63	-45	51.1	13.5	-63	-51	50.9
13	-54	-46	49.6	13.3	-61	-46	51.2	13.5	-63	-50	51.5
12.75	-55	-48	48.4	13.3	-65	-47	50.6	13.4	-59	-51	51.4
12.7	-59	-51	47.8	13.4	-59	-46	52	13.1	-55	-51	49.6
12.85	-59	-48	48.9	13.3	-61	-47	51.6	13.4	-63	-51	50.6
12.65	-60	-49	49.4	13.55	-66	-44	52.3	13.15	-58	-51	50.5
13.05	-60	-48	48.8	13.55	-54	-45	53.7	13	-50	-51	49.3
12.9	**-57.0**	**-48.1**	**49.1**	**13.4**	**-61.6**	**-45.6**	**51.6**	**13.3**	**-58.9**	**-50.4**	**50.5**

Figure 4.10. Measured Results of the 2.4 GHZ Minimal BOM Low-Power Matches in TX Mode with Different EFR32 Packages

As can be seen, the two-element minimal BOM matches comply both with the ETSI and FCC regulations up to 13 dBm power level.

Note that conducted spectrum plots are measured with the wideband 50 Ω termination of the Spectrum Analyzer. Different termination impedance at the harmonics generated by a real antenna+connecting Tline combination may result in much higher harmonic levels on the antenna.
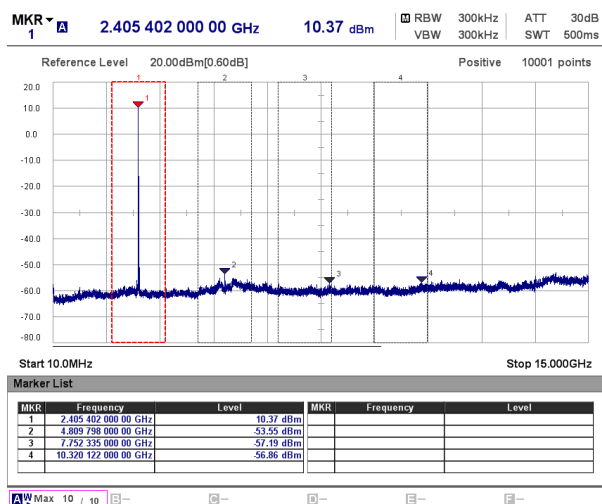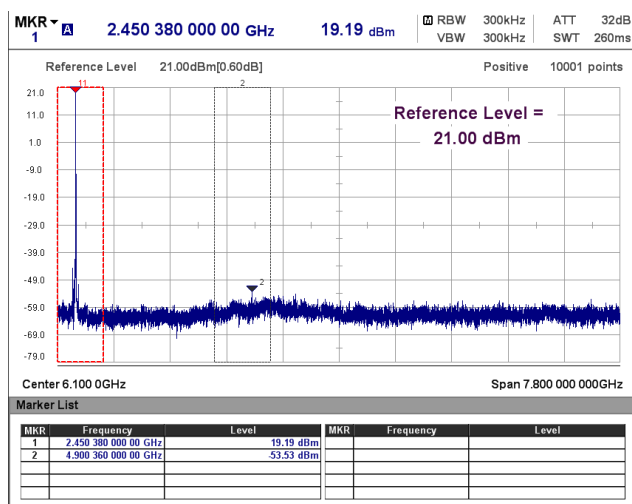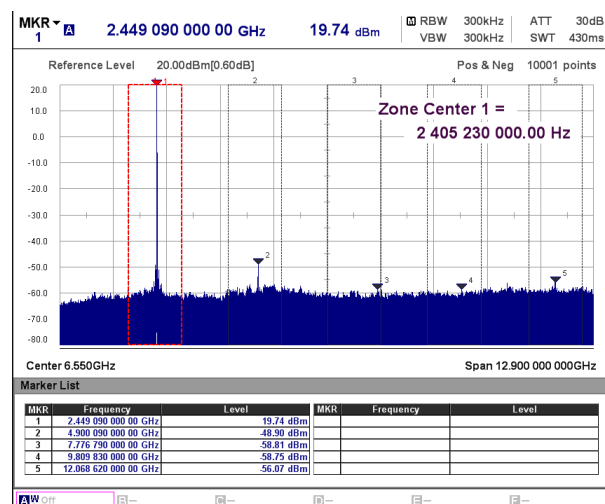
a)
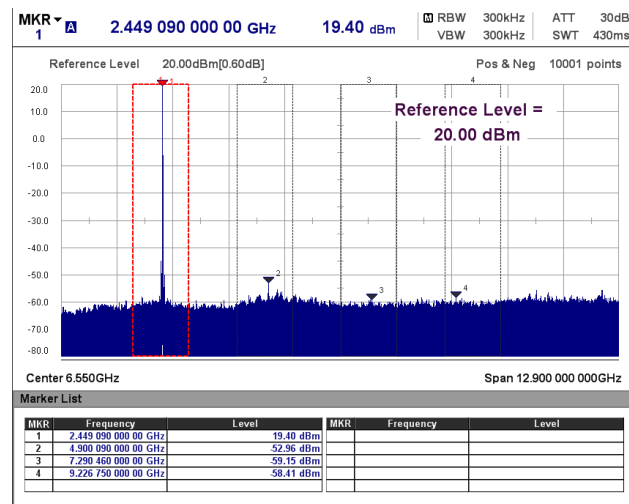
b)

Figure 4.11. Measured Spectrum Plots of the Dual Band EFR32 Version (BRD4151A) with Tline Match at a) 10 dBm Power Level (DCDC on) and with 20 dBm Power Level

a)

b)

Figure 4.12. Measured Spectrum Plots of the Single Band EFR32 Versions with Tline Match at 20 dBm Power State a) 7x7 mm (BRD4101A), b) 5x5 mm (BRD4111A)

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