AN930.2: EFR32 Series 2 2.4 GHz Matching Guide

The EFR32 Series 2 devices include chip variants that provide 2.4 GHz operation. In addition, the EFR32xG28 chips offer both 2.4 GHz and sub-GHz operation. The EFR32 Series 2 devices are available in various QFN packages, while the EFR32xG24 and EFR32xG27 devices offer options for WLCSP packages as well. This application note describes the matching techniques applied to the EFR32 Series 2 Wireless Gecko Portfolio in the 2.4 GHz band.

For information on PCB layout requirements for proper 2.4 GHz operation, refer to application note, AN928.2: EFR32 Series 2 Layout Design Guide. The sub-GHz matching network design details are discussed in application note, AN923.2: EFR32 Series 2 sub-GHz Matching Guide.

KEY POINTS

- Description of the applied 2.4 GHz matching networks and techniques for the EFR32 Series 2 devices
- Detailed discussion of the design steps and design examples
- Measured TX fundamental and harmonic performance
- Measured receive sensitivity values

1. Device Compatibility

This application note supports the following devices:

EFR32 Wireless Gecko Series 2:

- EFR32MG21
- EFR32BG21
- EFR32MG22
- EFR32BG22
- EFR32FG22
- EFR32MG24
- EFR32BG24
- EFR32MG27
- EFR32BG27
- EFR32FG28
- EFR32ZG28
- EFR32SG28

Note: The part number EFR32xG21 includes EFR32xG21-B and EFR32xG21-C, which are different revisions of the SoC.

2. Introduction

This application note is intended to help users achieve the best 2.4 GHz RF match for targeted applications. It describes the details of matching network design procedures and presents additional test results.

Thorough derivations of four different matching options are presented for EFR32xG21:

- 4-element discrete LC match for up to 0 dBm power levels
- 3-element discrete LC match for up to +10 dBm power levels
- 5-element discrete LC match for up to +20 dBm power levels
- 4-element combined discrete LC match for both +10 and 0 dBm power levels

4-element discrete LC matches for up to +6 dBm power levels are also presented for EFR32xG22. Furthermore, a 5-element discrete matching network is shown for the EFR32xG24 parts for a combined 0 and +10 dBm PA match, while another 5-element match is presented for +20 dBm power level. Also, EFR32xG27 has 4-element discrete LC matches presented. The EFR32xG28 devices have a 4-element discrete LCLC ladder matching circuit with an additional series dc-blocking capacitor.

The 4x4 mm, 32-pin 2.4 GHz-only version's package pinouts are shown in the figures below for the EFR32xG21, EFR32xG22, and EFR32xG27 parts. The 5x5 mm QFN40 version's package pinouts are also shown for the EFR32xG24 parts. The EFR32xG28 is shown with the dual-band version QFN48 package. The 2.4 GHz RF I/O pins are highlighted with a red box.

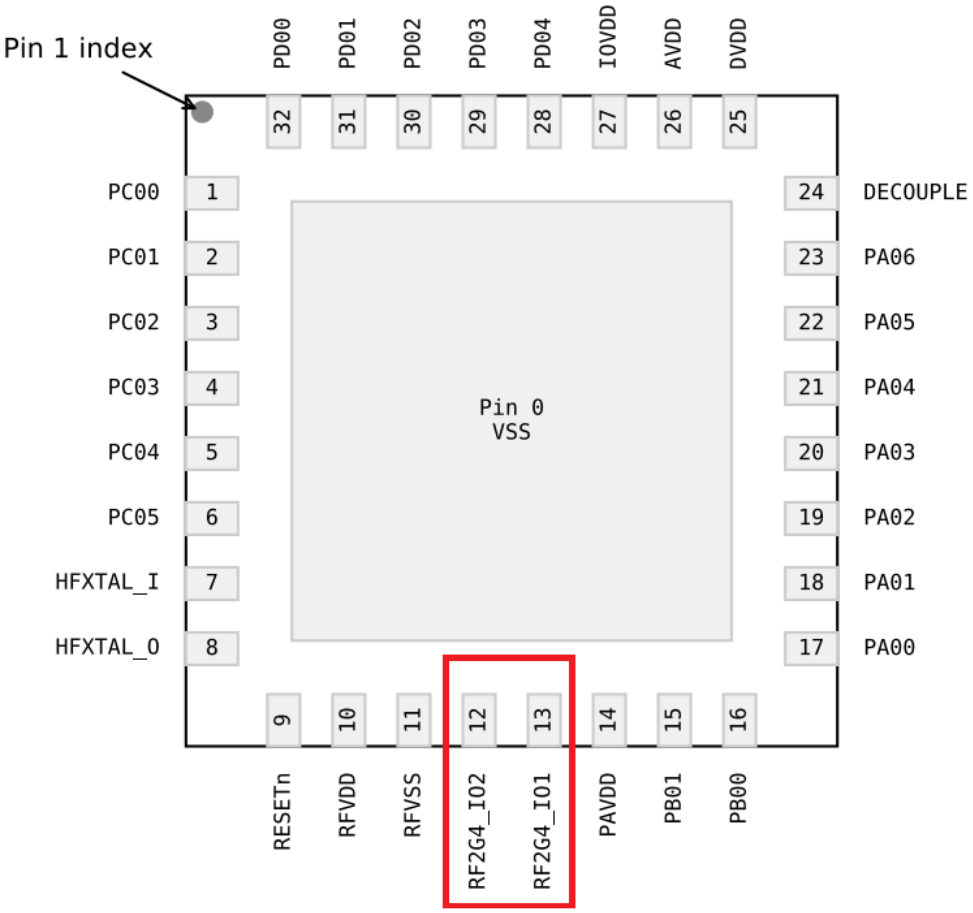

Figure 2.1. EFR32xG21 QFN32 (RF I/O Pins Highlighted)

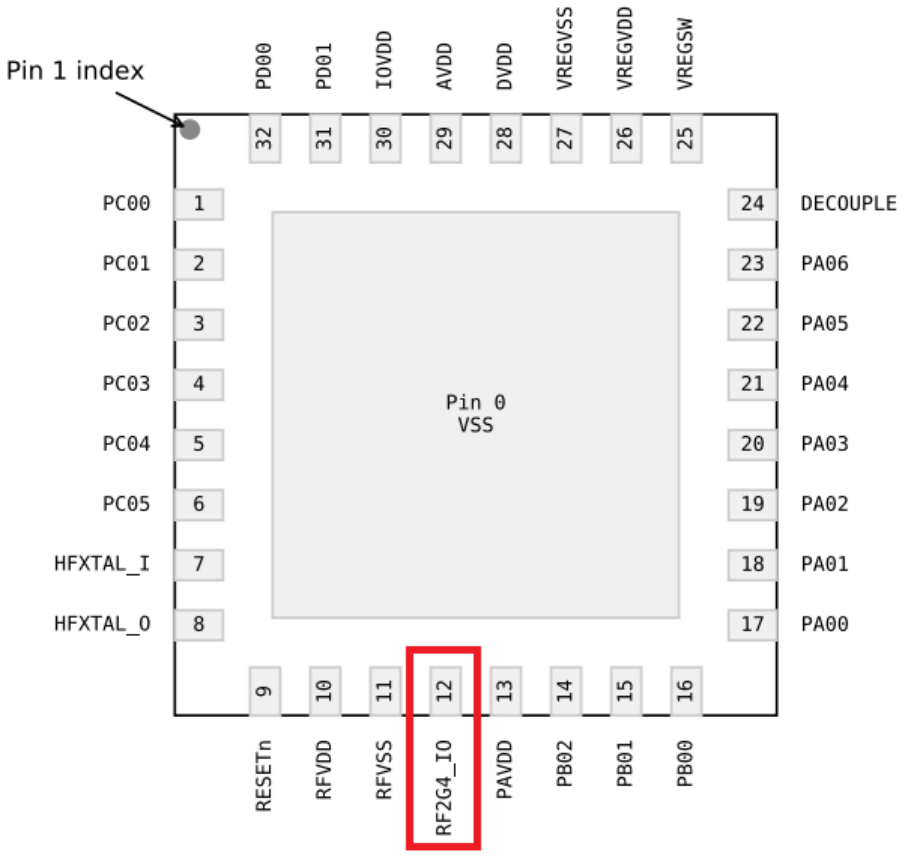

Figure 2.2. EFR32xG22 QFN32 (RF I/O Pin Highlighted)

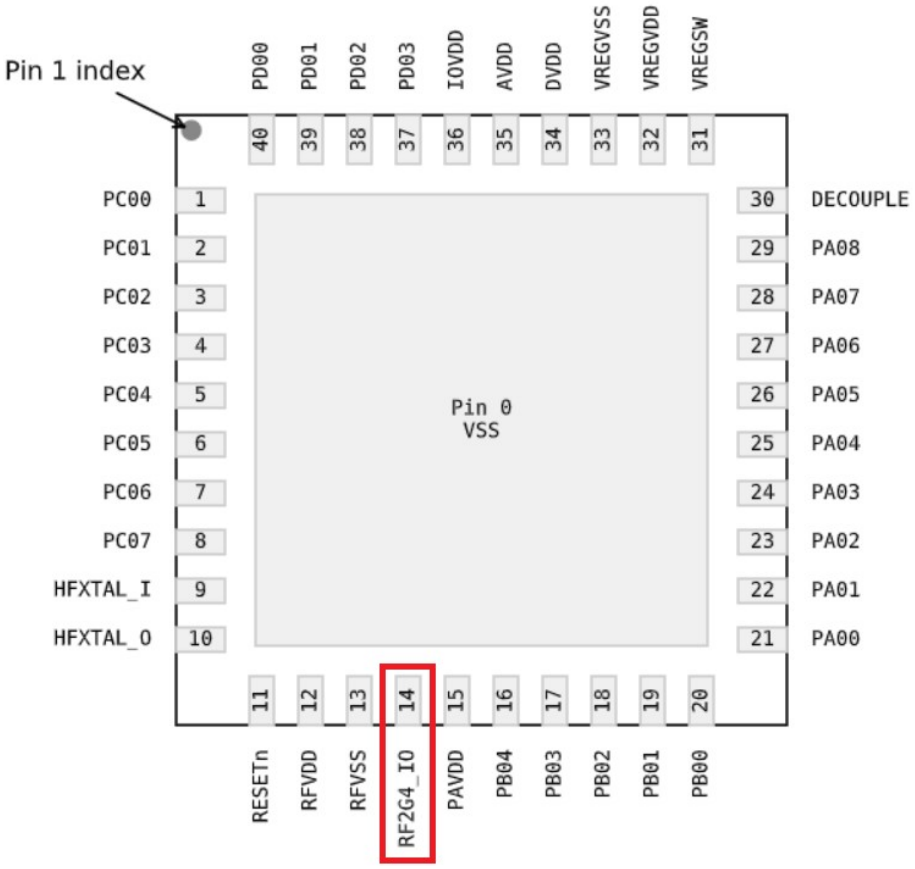

Figure 2.3. EFR32xG24 QFN40 (RF I/O Pin Highlighted)

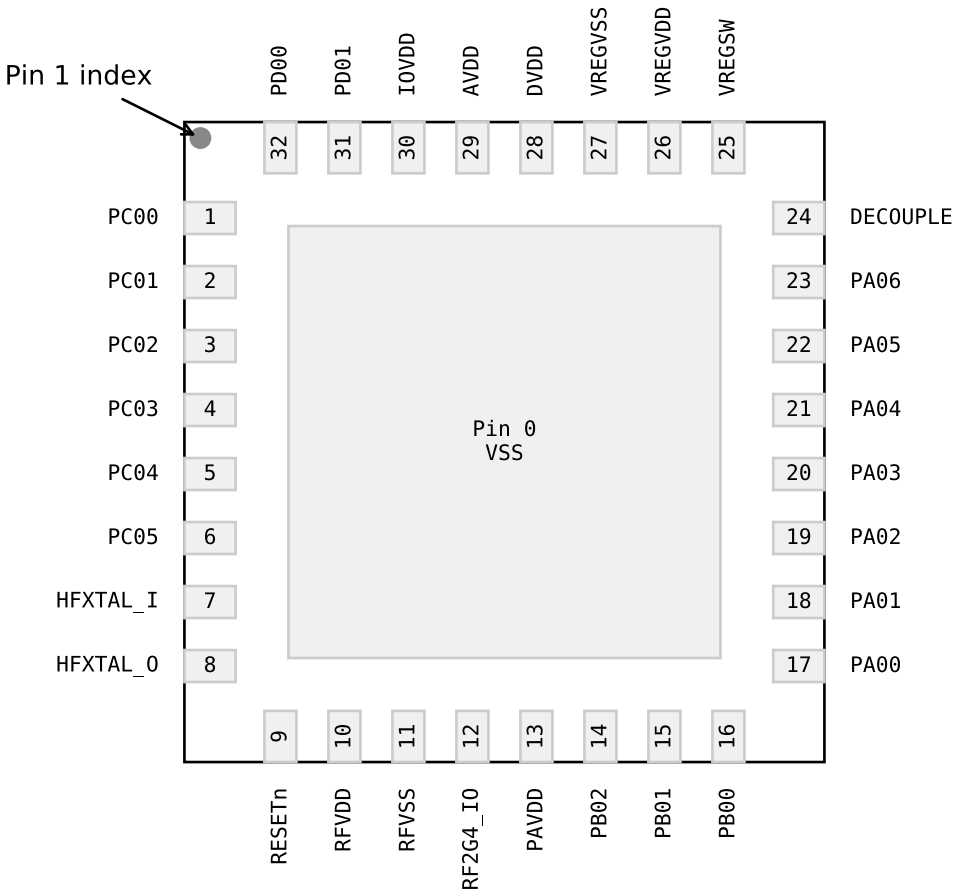

Figure 2.4. EFR32xG27 QFN32 with Buck DC-DC (RF I/O Pin Highlighted)

Note: The EFR32xG27 devices are available with boost or buck dc-dc capabilities. The figure above shows the device pinout for the QFN32 with buck dc-dc version. For further details on pin definition for the different variants, refer to the EFR32MG27 or EFR32BG27 data sheets.

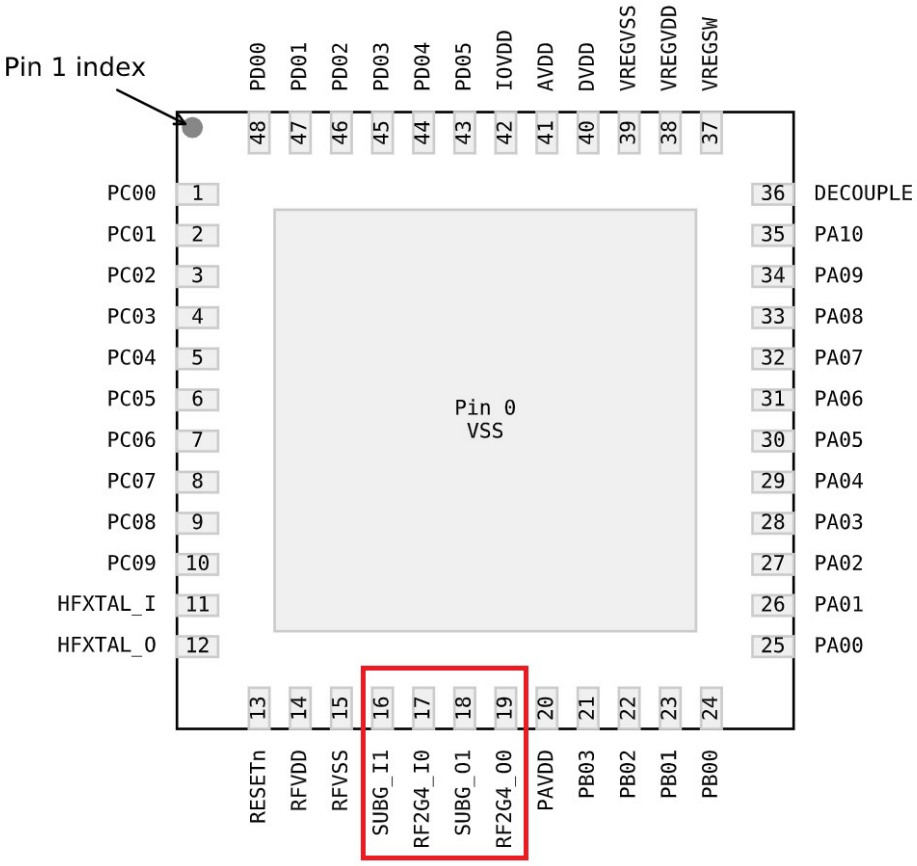

Figure 2.5. EFR32xG28 QFN48 Dual-Band (Sub-GHz and 2.4 GHz)

Note: The EFR32xG28 devices are available with the following chip variant options: two +14 dBm sub-GHz PAs; one +14 dBm sub-GHz PA and one +10 dBm BLE 2.4GHz PA; two +20 dBm sub-GHz PAs; one +20 dBm sub-GHz PA, and one +10 dBm BLE 2.4GHz PA. The figure above shows the pinout of the dual-band variants.

2.1 Related Literature

Related documentation includes:

- AN928.2: EFR32 Series 2 Layout Design Guide
- AN923.2: EFR32 Series 2 sub-GHz Matching Guide
- AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations

3. RF Architecture Overview

3.1 EFR32xG21 RF Front-End Overview

The EFR32 Series 2 xG21 chip family has 2.4 GHz RF front-ends only. The 2.4 GHz RF front-end architecture is shown in the figure below. The 2.4 GHz antenna interface consists of two pins (RF2G4_IO1 and RF2G4_IO2) that interface directly to the on-chip BALUN.

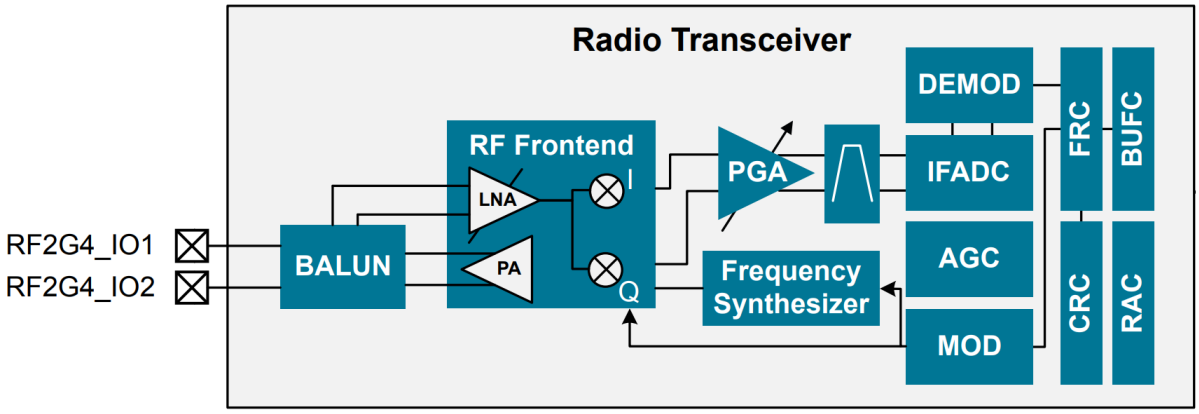

Figure 3.1. 2.4 GHz RF Front-end Configuration

Several changes compared to the EFR32 Series 1 chip variants are highlighted below:

- New RF front-end topology: Three PAs included that require an optimal load impedance for each TX power level, i.e., different matches are required per max TX power.
- Power supply scheme: There is no on-chip DCDC converter available. Optimized for mains-power applications.
- Pre-Regulator for the Power Amplifiers: Linear regulator with an input of PAVDD and output of PA blocks. Regulates to a target voltage when PAVDD > Vtarget. Follows supply with a ~30 mV offset when PAVDD ≤ Vtarget (and PA power will trail off also).
  - For +10 and 0 dBm PA modes: Vtarget = 1.8 V.
  - For +20 dBm PA mode: Vtarget = 3.3 V.
- RFSENSE removed, instead a wide-band power sensing block introduced for better out-of-band blocker detection and coexistence performance.

The on-chip part of the front-end comprises three PA structures optimized for the TX power levels of 0, 10, and 20 dBm, two differential LNAs, and an integrated balun. Each PA is biased through the PAVDD pin. Externally, a single-ended matching network and harmonic filtering are required.

- Differential Class-AB mode PA and an internal balun for TX power of +20 dBm
- Single-ended Class-D mode PA for TX power of +10 dBm
- Single-ended Class-D mode PA for TX power of 0 dBm
- Two LNAs
- Two RF IO ports available: Internal switches ground one of the two sides to create single-ended inputs / outputs on either RFIO pin.

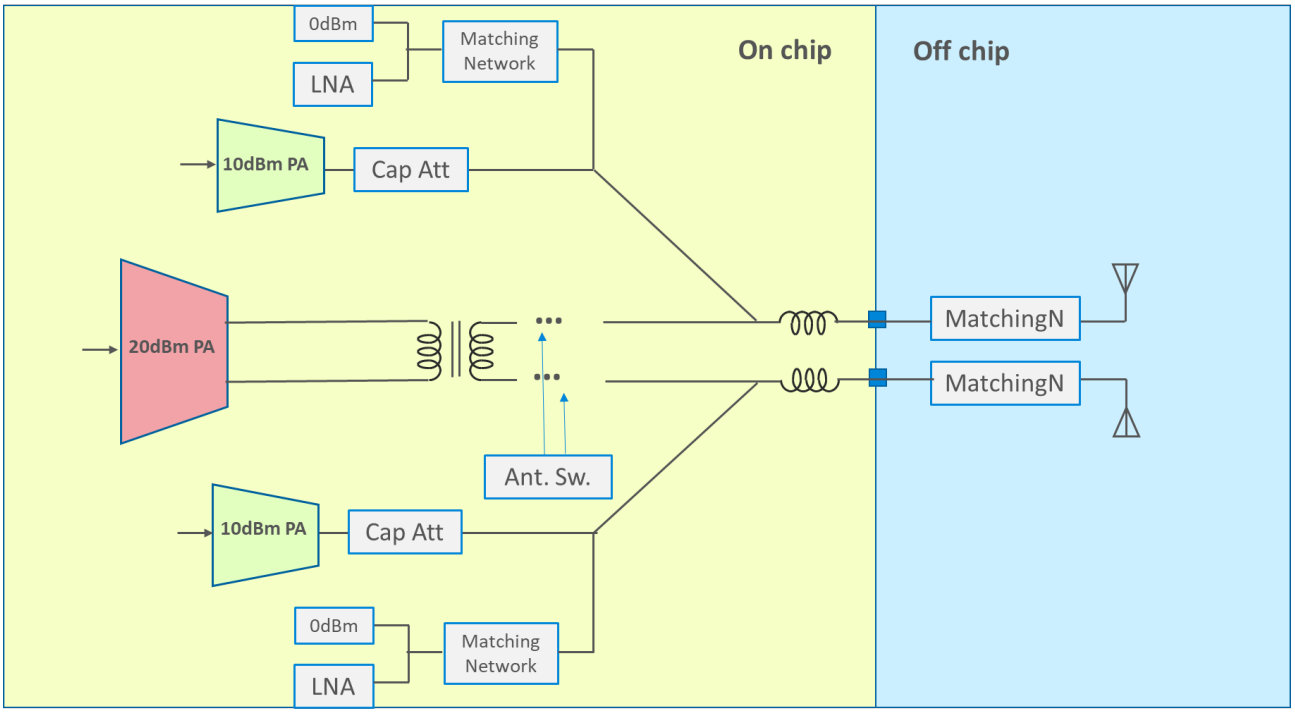

Figure 3.2. 2.4 GHz RF Front-end Block Diagram

3.2 EFR32xG22 RF Front-End Overview

The EFR32 Series 2 xG22 chip family has 2.4 GHz RF front-ends only. The radio subsystem is shown in the figure below. The RF front-end consists of an integrated LNA and two separate PAs with an internal switch to select between them, while one RF IO port is available (RF2G4_IO) at a chip pin.

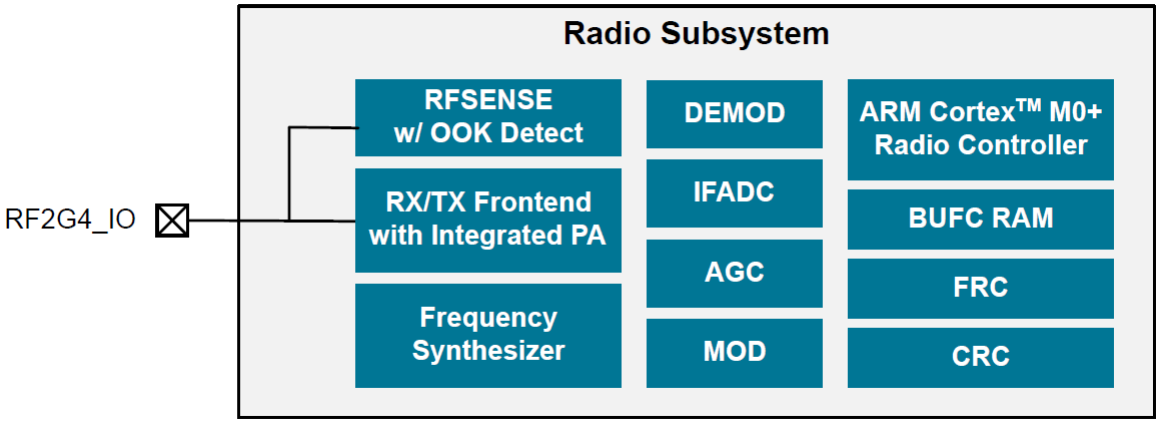

Figure 3.3. EFR32xG22 Radio Subsystem

A few highlights on the RF front-end blocks:

- Two separate Class-D PAs, optimized for maximum TX power levels of 0 and +6 dBm.
  - Each PA is biased through the PAVDD pin with an internal regulator targeting 1.6 and 1.62 V for the 0 and +6 dBm PA, respectively.
  - Externally, a single-ended matching network and harmonic filtering are required
- Power supply scheme: An on-chip, dc-dc converter is available, so this chip variant is optimized for low-power applications with high efficiency.

3.3 EFR32xG24 RF Front-End Overview

The on-chip part of the front-end comprises three PA structures optimized for the TX power levels of 0, 10, and 20 dBm, a differential LNA, and an integrated balun. Each PA is biased through the PAVDD pin. On the chip package 1 RF I/O port is available. Externally, a single-ended matching network and harmonic filtering are required. Two bond-out options as chip variants are available, one for +20 dBm only, while another one with both 0 and +10 dBm PAs available where an internal switch is controlled internally to select between them.

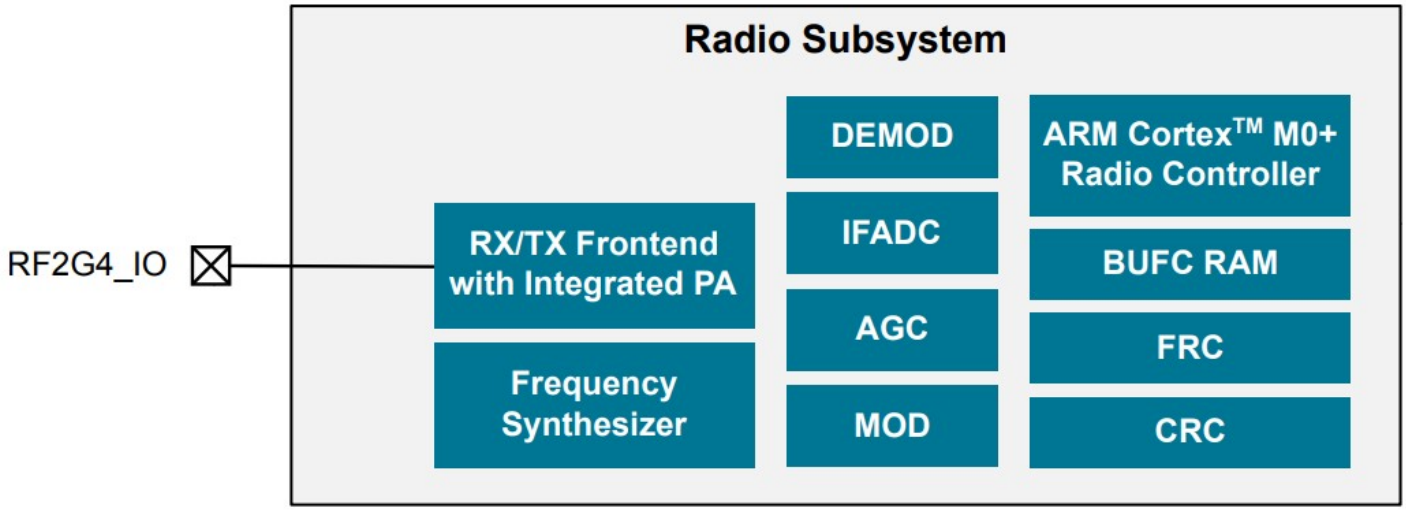

Figure 3.4. EFR32xG24 Radio Subsystem

A few highlights on the RF front-end blocks:

- Class AB or Class-D PA, optimized for different maximum TX power levels depending on the chip variant:
  - QFN40/48 +20 dBm PA: Differential Class AB mode PA and an internal balun with an internally regulated PA (output stage) voltage of 3.2 V
  - QFN40/48 +10 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.675 V
  - QFN40/48 0 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.64 V
  - WLCSP42 +4 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.675 V
  - WLCSP42 0 dBm PA: Single-ended Class D mode PA with an internally regulated PA (output stage) voltage of 1.64 V
- Power supply scheme: An on-chip, dc-dc converter is available, so this chip variant is also optimized for low-power applications with high efficiency.

3.4 EFR32xG27 RF Front-End Overview

The EFR32 Series 2 xG27 chip family has 2.4 GHz RF front-ends only. The radio subsystem is shown in the figure below. The RF front-end consists of an integrated LNA and two separate PAs with an internal switch to select between them, while one RF IO port is available (RF2G4_IO) at a chip pin.

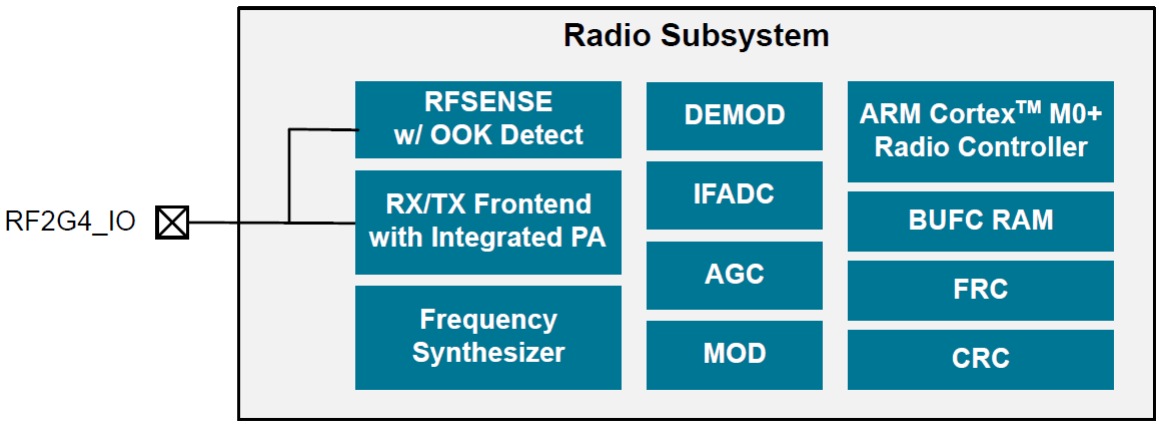

Figure 3.5. EFR32xG27 Radio Subsystem

A few highlights on the RF front-end blocks:

- Two separate Class-D PAs, optimized for different maximum TX power levels depending on the chip variant:
  - QFN32/40 with buck dc-dc converter: 0 dBm and +8 dBm
  - QFN32/40 with boost dc-dc converter: 0 dBm and +6 dBm
  - WLCSP39 with a buck and a boost dc-dc converter: 0 dBm and +4 dBm
- Each PA is biased through the PAVDD pin with an internal regulator targeting 1.6 and 1.62 V for the 0 dBm and high-power PA, respectively.
- Externally, a single-ended matching network and harmonic filtering are required.
- Power supply scheme: An on-chip, dc-dc converter is available (buck, boost, or both, depending on the package), so these chip variants are optimized for low-power applications with high efficiency.

3.5 EFR32xG28 RF Front-End Overview

The sub-GHz and 2.4 GHz LNA and PA circuits in the EFR32xG28 parts are single-ended and are not tied together inside the chip. Two separate TX and two separate RX RF pins are available at chip pins. These four pins are adjacently located, regardless of the chip variant. The RF matching circuit must provide for connecting the TX and RX signal paths together, external to the RFIC. Based on the selected OPN, sub-GHz-only and dual-band (sub-GHz and 2.4 GHz) variants are available. The sub-GHz-only variant provides 2-2 sub-GHz TX/RX ports similarly as EFR32xG23, while the dual-band variant provides 1-1 sub-GHz TX/RX and 1-1 2.4 GHz TX/RX ports.

The dual-band variant's antenna interface consists of a sub-GHz and a 2.4 GHz single-ended input pin (SUBG_I1, RF2G4_I0) that interface directly to sub-GHz and 2.4 GHz LNAs, respectively, and a sub-GHz and a 2.4 GHz single-ended output pin that interface directly to the sub-GHz +14 dBm or +20 dBm PA (SUBG_O1) and to the 2.4 GHz +10 dBm PA (RF2G4_O0), respectively. EFR32xG28 parts are available either with the +14 dBm (LPA) or +20 dBm (HPA) sub-GHz Class-D PAs, these are internally bonded options so different OPN part numbers are used for the chip variants with different maximum TX power levels. The 2.4 GHz PA is a +10 dBm Class-D PA optimized for BLE applications (with constant envelope modulations).

The sub-GHz-only variant's antenna interface consists of two single-ended input pins (SUBG_I0 and SUBG_I1) that interface directly to two LNAs and two single-ended output pins that interface directly to two +14 dBm or +20 dBm PA (SUBG_O0 and SUBG_O1). Integrated switches select either SUBG_O0 or SUBG_O1, SUBG_I0 or SUBG_I1 to be the active paths. EFR32xG28 parts are available either with the +14 dBm (LPA) or +20 dBm (HPA) sub-GHz Class-D PAs, these are internally bonded options so different OPN part numbers are used for the chip variants with different maximum TX power levels. The sub-GHz PA matching procedure and details are discussed in application note, AN923.2: EFR32 Series 2 sub-GHz Matching Guide.

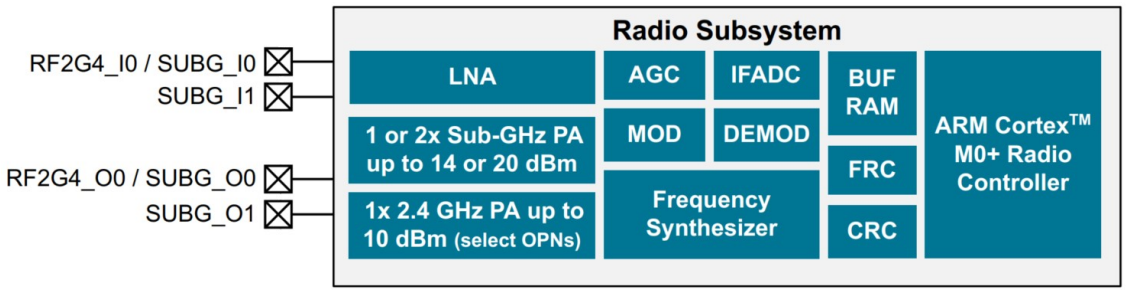

Figure 3.6. EFR32xG28 Radio Subsystem

- Sub-GHz +14/20 dBm Class-D PA and 2.4GHz +10 dBm Class-D PA, depending on the chip variant.
- On-chip DCDC converter is available with a typical +1.8 V output.
- Each PA is biased through the PAVDD pin with an intenal regulator targeting 1.65 V for the sub-GHz +14 dBm and 2.4 GHz +10 dBm PAs, while 3.0-3.15 V for the sub-GHz +20 dBm PA.
- Externally, single-ended PA and LNA matching networks and TX harmonic filtering are required.

4. 2.4 GHz RF Matching Design Steps

2.4 GHz RF matching design for EFR32 chips consists of the following steps:

1. Determine the optimum termination impedance for the PA. Note that different matching topologies are recommended for different TX power levels as shown in the Introduction section.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the pcb have a major effect, so tuning/optimization of the design is required. Here an optional EM simulation can be done, but simulations with well-estimated pcb parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

4.1 Determining the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the RF2G4_IO1/2 pin if 50 Ω termination is applied at the antenna port.

The RF2G4_IO1/2 RF port termination determines the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX mode. In addition, proper harmonic suppression and good RX sensitivity in reception mode are required.

4.1.1 EFR32xG21 Optimum PA Load Impedance

The design target of optimum load impedance looking from the PA to the antenna is 14 + j5 Ω at the PA. However, the optimum termination impedance for both delivering the desired power and achieving the best PA efficiency in TX mode is determined by load-pull testing. The optimum termination impedance at the chip pin is determined for each PA of the EFR32xG21 parts and it slightly differs for the different power levels, i.e., for the +20, +10, and 0 dBm PAs, and also differs from the design target at the PA due to bonding wire inductances and parasitics. This termination impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load. The optimum termination impedance at chip RF2G4_IO pin is the following:

- For the **+20 dBm** PA: Zload_opt = **12.6 - j11 Ω**
- For the **+10 dBm** PA: Zload_opt = **12.2 - j8.3 Ω**
- For the **0 dBm** PA: Zload_opt = **17.4 + j3.9 Ω**

The load-pull curves for each PA are shown in 6. Appendix 1 PA Optimum Termination Impedance on EFR32xG21.

Applications with one antenna typically require using only one of the RF IO ports available on the EFR32xG21 parts, in which case the recommended active RF IO port is **RF2G4_IO2**. Because this pin has a shorter on-chip, internal connection to the PA blocks so slightly lower parasitics appear on this pin.

The proper impedance at one of the single-ended RF2G4_IO pins also depends on the loading of the other RF2G4_IO pin. To keep its effect negligible, for applications with one antenna with both +10 and +20 dBm PAs, it is recommended to directly tie the un-used RF2G4_IO pin back to the center GND pad of the chip. However, the 0 dBm PA requires to be DC blocked externally so the method described for the +10 and +20 dBm PAs doesn't work. The 0 dBm PA recommended match includes a series capacitor in the RF path but for proper operation a DC-blocking 0.5pF capacitor to GND needs to also be used on the unused RF port. Silicon Labs' reference radio boards are suitable and optimized to be used with the +10 and +20 dBm PAs because of the short between the chip pin and center GND pad under the chip. More detailed information about proper layout design can be found in application note, "AN928.2: EFR32 Series 2 Layout Design Guide".

In real radio links, the TX power and the receiver sensitivity together (i.e., the link budget) determine the range. So, with the applied TX termination impedance, the impedance match in RX mode should also be acceptable. Fortunately, the RX sensitivity is quite immune to impedance variations. The sensitivity variation is less than 0.5 dB if the termination changes from 50 Ω to the PA optimum impedance (Zload_opt) given above.

4.1.2 EFR32xG22 Optimum PA Load Impedance

The design target of optimum load impedance looking from the PA to the antenna is 50 Ω at the PA for both 0 and +6 dBm PA. However, the optimum termination impedance at the chip pin determined for each PA of the EFR32xG22 parts differs from the design target at the PA due to bonding wire inductances and parasitics. Also, the output match plus low-pass filter (LPF) section is designed to enhance the suppression of the 2nd- and 3rd-order harmonics. Thus, the optimum termination impedance at the chip pin is about **37 + j5 Ω** for both 0 and +6 dBm PA and this impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load.

Because the optimum termination impedance is the same for both 0 and +6 dBm PA, the matching network is also identical for these different power levels. Silicon Labs provides radio boards with one matching network applied, however, the series dc-blocking capacitor in the match plus LPF section must be needed only when the 0 dBm PA is being utilized.

4.1.3 EFR32xG24 Optimum PA Load Impedance

The optimum PA load impedance values are listed below in this section for each PA and chip variants. The impedance values are given at the chip pin looking into the RF matching network.

QFN packages (simulated):

- For both **+10 dBm/0 dBm PA**: Zpin = **17.7 - j2.3 Ω**
- For the **+20 dBm PA**: Zpin = **22.6 - j12.4 Ω**

WLCSP package (measured):

- For both **+4 dBm/0 dBm PA**: Zpin = **20.6 + j8.2 Ω**

Zpin impedance values are compromised to provide the possible highest TXP, power efficiency and best RX sensitivity, while ensuring sufficient margins to pass radiated emissions across global RF regulatory standards.

4.1.4 EFR32xG27 Optimum PA Load Impedance

The design target of optimum load impedance from the PA to the antenna is 50 Ω at the PA for both the 0 dBm and high-power PA of all package variants. However, the optimum termination impedance at the chip pin determined for each PA of the EFR32xG27 parts differs from the design target at the PA due to bonding wire inductances and parasitics. Also, the output match plus low-pass filter section is designed to enhance the suppression of the 2nd- and 3rd-order harmonics. Additionally, the differences in packaging (QFN vs. WLCSP) introduces slightly different termination conditions. The optimum PA load impedance values are listed below in this section for each PA and chip variants. The impedance values are given at the chip pin looking into the RF matching network.

QFN packages with buck/boost dc-dc converter (simulated):

- For both **high-power/0 dBm PA**: Zpin = **37 + j5 Ω**

WLCSP package (measured):

- For both **+4 dBm/0 dBm PA**: Zpin = **29 + j4.4 Ω**

Because the optimum termination impedance is the same for both the 0 dBm and high-power PA, the matching network is also identical for these different power levels per package type. Silicon Labs provides radio boards with one matching network applied per package type; however, the series dc-blocking capacitor in the match plus LPF section must be needed only when the 0 dBm PA is being utilized.

4.1.5 EFR32xG28 Optimum PA/LNA Load Impedance

The optimum 2.4 GHz PA load impedance value is listed below in this section. The impedance value is given at the chip pin looking into the RF matching network.

2.4 GHz +10 dBm PA: Zpin = **8.5 – j11.5 Ω**

Zpin impedance value is compromised to provide the possible highest TXP and power efficiency, while ensuring sufficient margins to pass radiated emissions across global RF regulatory standards.

The RX matching network for the LNA needs to ensure the possible highest voltage gain in the RX path, while resonating the internal CLNA=~1.2 pF capacitance out. The reference RX match converts the 50 Ω antenna impedance up to around 200 Ω to the RX pin.

4.2 Choosing the RF Matching Topology

The second step of the matching design procedure is to choose the appropriate RF matching topology.

In addition to creating an optimum termination impedance on the IC side, the matching solution must exhibit sufficiently robust harmonic filtering characteristics to comply with emissions standards. There are many different types of RF matching topologies. Separate matching and harmonic filtering sections can be utilized, or they can be combined in one circuit. To minimize the number of elements, all matches presented here are of the combined type, with low-pass circuits employed for their inherent harmonic suppression characteristics.

Four 2.4 GHz matching topologies for EFR32xG21 are presented here:

- 4-element discrete LC match for the 0 dBm PA, i.e., for power levels equal or below 0 dBm
- 4-element combined discrete LC match for both 0 and +10 dBm PA, i.e., for power levels equal or below +10 dBm
- 3-element discrete LC match for the +10 dBm PA, i.e., for power levels equal or below +10 dBm, but not suitable to operate with the 0 dBm PA (i.e., equal or below 0 dBm the required PA to be used is still the +10 dBm PA which has less power efficiency at that lower power range)
- 5-element discrete LC match for the +20dBm PA, i.e., for power levels equal or below +20 dBm (not suitable to operate with the 0 dBm PA)

For EFR32xG22, 4-element discrete LC matches are provided that are optimized for both 0 and +6 dBm PA, i.e., for any power level available with this part. The EFR32xG24 family of SoCs requires a 5-element discrete LC match for a combined 0 and +10 dBm PA match, and a different 5-element discrete LC match for the +20 dBm PA.

For EFR32xG27, separate 4-element discrete LC matches are provided for the QFN and WLCSP packages that are optimized for both the 0 dBm and high-power PA.

For EFR32xG28 (which has separate TX and RX pins), a so-called direct-tie TX/RX match is presented where the separate TX and RX matches are directly connected to each other. The +10 dBm PA match is a 4-element LCLC ladder match with an additional series dc-blocking capacitor, while the LNA match is a 2-element match (shunt inductor plus a series trace). Here, the direct-tie matching network design principles are the same as discussed in the application note, AN923.2: EFR32 Series 2 sub-GHz Matching Guide. Furthermore, the matching network in the 2.4 GHz path consists of an RF switch after the direct-tie point. This switch shunts the output to the GND through a 50-ohm resistor when the EFR32xG28 transmits at the sub-GHz frequencies. This is required to avoid any unwanted harmonic radiation in or close to the 2.4 GHz frequency band from the 2.4 GHz path after coupling between the two RF paths. For more details, refer to the application note, AN1409: EFR32xG28 Sub-GHz and 2.4 GHz Dual-Band Requirements.

4.3 Initial Design with Ideal, Loss-Free Elements

After choosing the appropriate topology for the application based on the TX power level requirements, the third step of the matching design procedure is to generate a lumped element schematic of the match with ideal loss-free elements and without PCB parasitics.

The matching circuit should show an input impedance of *Zload_opt* at the RF IO port of the chip while it is terminated by 50 Ω load at its output (ANT port). The impedance procedure is shown in the next sections, where, for simplification, the matching design is started from a termination impedance (*ZL*) which is the complex conjugate of the *Zload_opt* impedance. The reason is that the matching network will show the required *Zload_opt* impedance at its RF port only if it is perfectly matched there to a termination impedance which is the complex conjugate of the *Zload_opt* impedance.

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free ideal capacitors and inductors are used, and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization.

4.4 Design with Parasitics and Losses

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the used SMD components and also the PCB parasitic effects need to be taken into account during the matching network design. The SMD components at these high-frequency ranges behave as a resonator. A capacitor can be realized by a series RLC resonant circuit, meanwhile an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L-C components, and can have considerable series parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. For more details on the SMD parasitic descriptions and the rough estimation of PCB parasitics, refer to the application note, AN930.1: EFR32 Series 1 2.4 GHz Matching Guide, and the SMD manufacturer website at www.murata.com, in regards to the appropriate SMD equivalent circuits.

The SMD components with different sizes have different parasitics, so it is also important to calculate with the appropriate values. Silicon Labs reference designs use **SMD 0201** components.

The PCB parasitics also have effects on the RF performance versus tuned component values of the matching network. Silicon Labs reference design matching network component values are typically given with a 4-layer PCB with a separation of about 300 µm between the top (component-side) and first inner layer. This distance mostly determines the parasitics capacitance and via inductance, which influences the return-path impedance between the matching network and chip GND (especially at the harmonics). Also, the series trace placed between the chip pin and matching network is part of the match, the dimensions of which should be followed carefully from Silicon Labs reference designs. Refer to AN928.2: EFR32 Series 2 Layout Design Guide for more layout details.

In the case of using different PCB stack-up (e.g. 2-layer PCB with board thickness > 300 um), the matching network component values need tuning to keep the RF performance values, especially the harmonic suppressions.

The recommended matching network for the RF port(s) of each part is shown in the section Recommended Matching Networks. The circuit provides the optimum impedance load for the EFR32xG2x part while ensuring sufficient harmonic suppression. Some of the shunt capacitors are tuned to have self-resonances at the frequency ranges falling close to TX harmonics and therefore, they provide enhanced attenuation at specific harmonics. The impedance transformation procedure for each PA of EFR32xG21 is shown in the Smith Chart figures below.

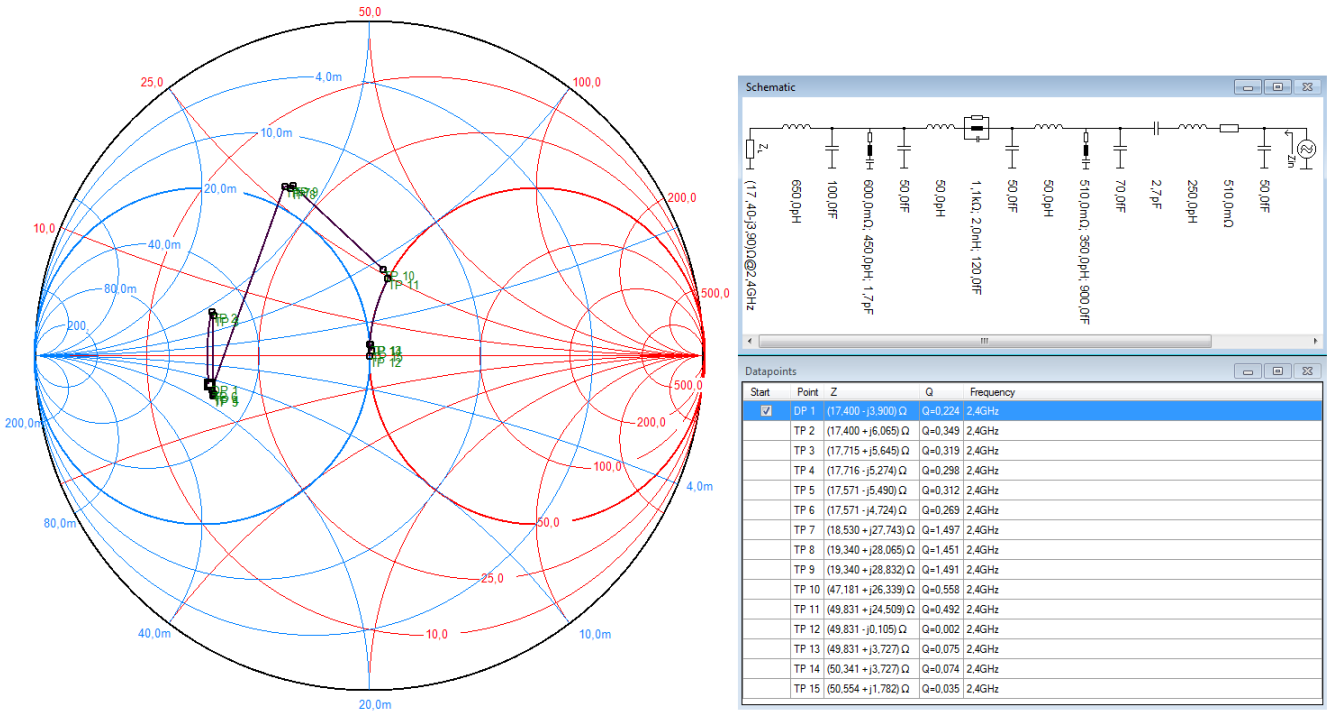

Figure 4.1. EFR32xG21 4-element Match with SMD and PCB Layout Parasitics Tuned for the 0 dBm Power Level Optimum

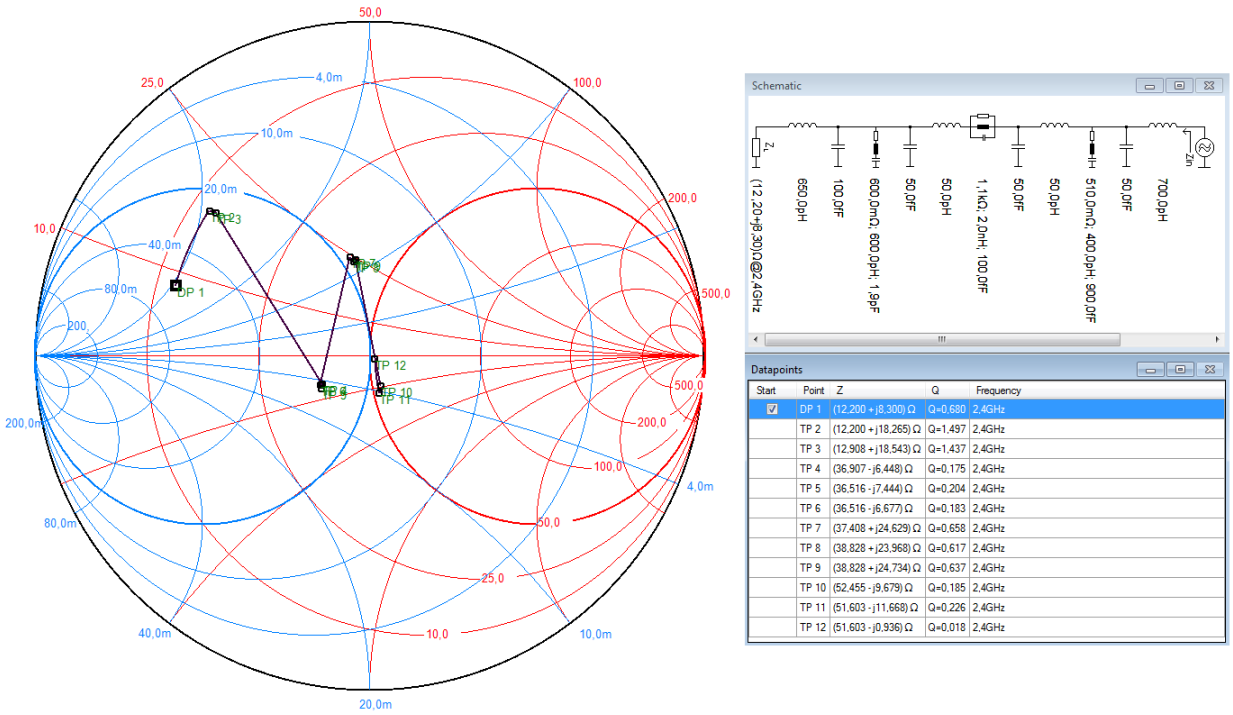

Figure 4.2. EFR32xG21 3-element Match with SMD and PCB Layout Parasitics Tuned for the 10 dBm Power Level Optimum

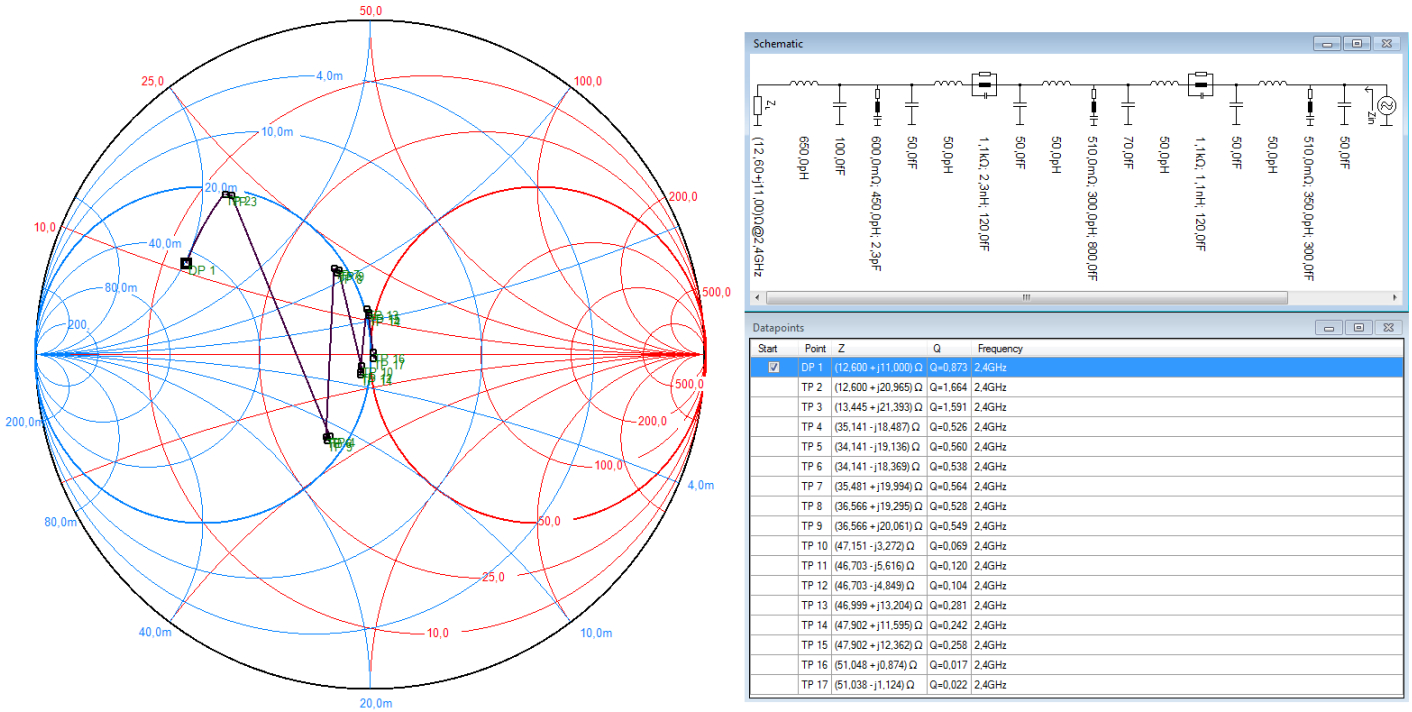

Figure 4.3. EFR32xG21 5-element Match with SMD and PCB Layout Parasitics Tuned for the 20 dBm Power Level Optimum

4.5 Simulation Example on the 5-element Match for +20 dBm Power Level on EFR32xG21

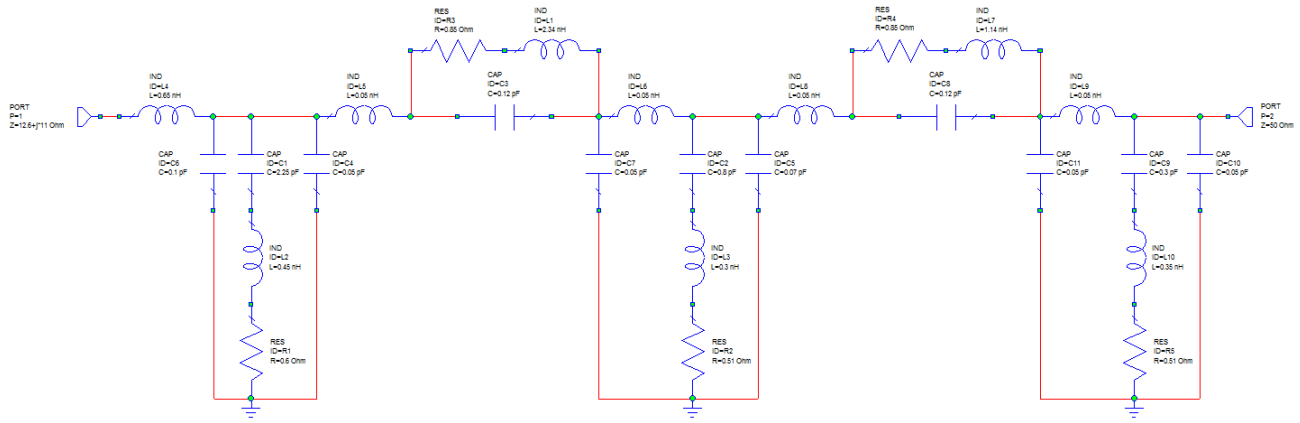

Figure 4.4. Discrete Schematic Model of 5-element Match with SMD and PCB Layout Parasitics

Port 1 (left-hand side-end) is the RF2G4_IO chip port/pin where the port impedance (*ZL*) should be set for the complex conjugate of optimum load impedance (*ZL=Zload_opt**), while the Port 2 (right end) is the 50-ohm antenna port.

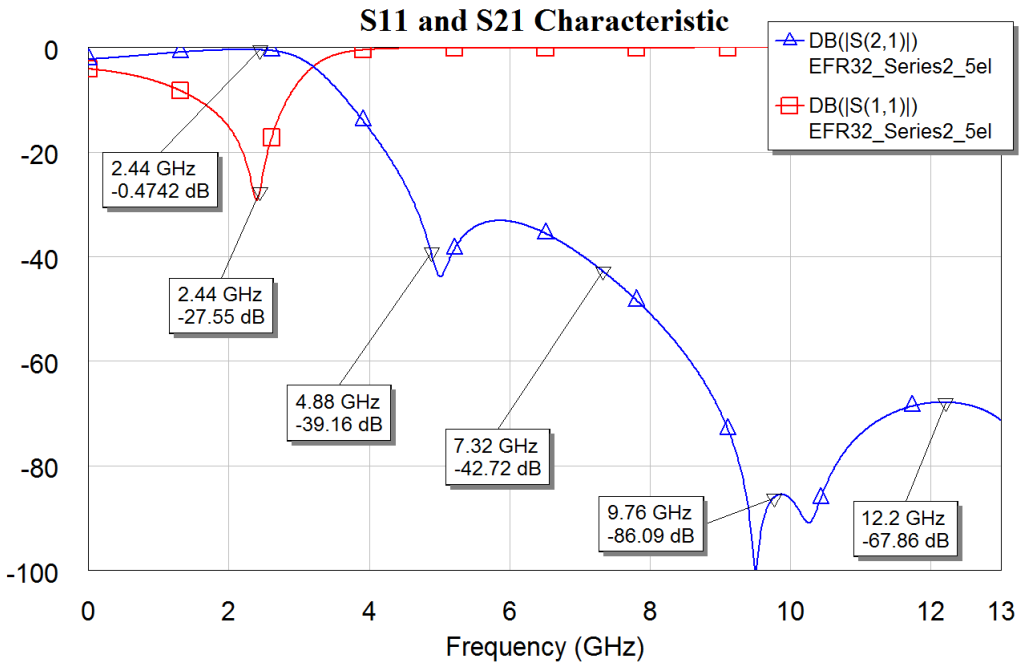

Figure 4.5. S11 and S21 Characteristics of 5-element Match for 20 dBm Power Level Optimum

5. Recommended Matching Networks

5.1 EFR32xG21 Matching Networks

The part number EFR32xG21 includes EFR32xG21-B and EFR32xG21-C, which are different revisions of the SoC.

5.1.1 Recommended Matching Network for the 0 dBm PA

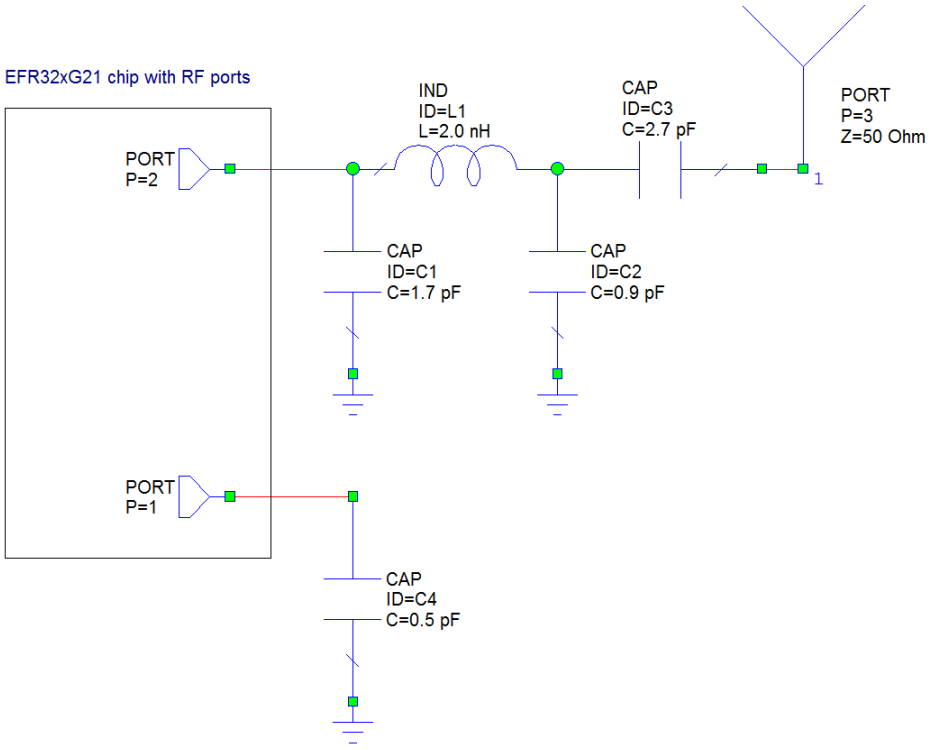

Figure 5.1. Matching Network Schematic for the 0 dBm PA

It is recommended to use this matching network shown above when the maximum transmitting power requirement is 0 dBm (TX power ≤ 0 dBm), i.e., the application utilizes the 0 dBm PA to achieve the possible best efficiency at that low power regions. Due to the highly optimized power efficiency, the need of 4-element matching network here is mostly driven by the harmonic suppression requirements. The unused RF2G4_IO pin needs to be grounded via an (DC-blocking) 0.5 pF capacitor.

Table 5.1. Final SMD Values for the 0 dBm PA (4-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.7 pF	± 0.5 %	GRM0335C1H1R7WA01D	Murata
L1	2.0 nH	± 0.1 nH	LQP03HQ2N0B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata
C3	2.7 pF	± 0.5 %	GRM0335C1H2R7WA01D	Murata
C4	0.5 pF	± 0.05 pF	GRM0335C1HR50WA01D	Murata

5.1.2 Recommended Matching Network for the +10 dBm PA

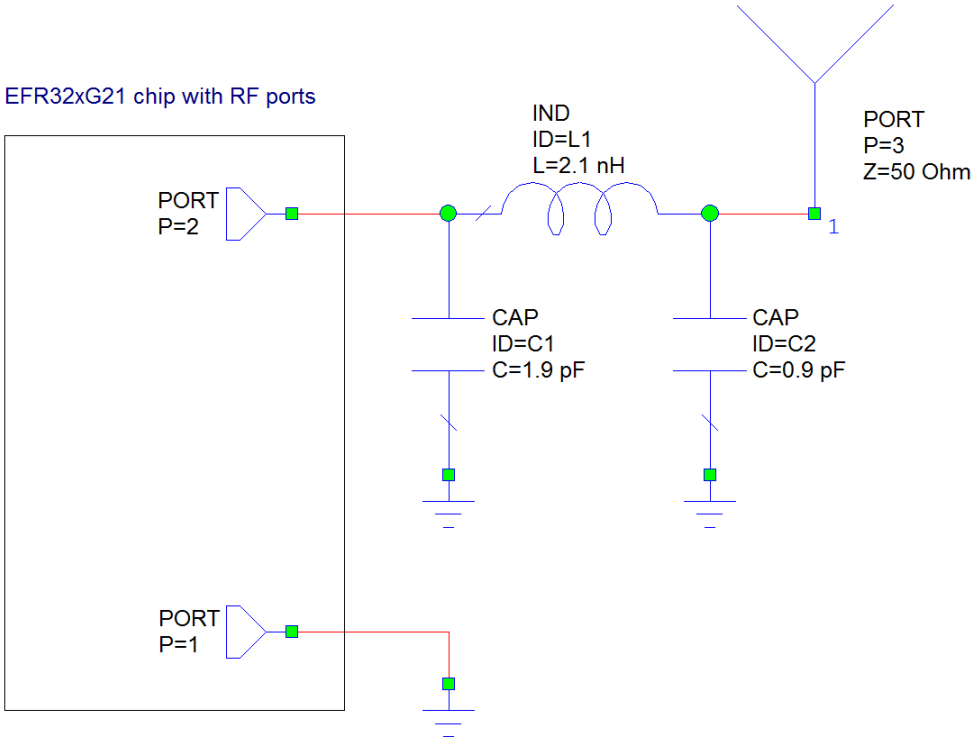

Figure 5.2. Matching Network Schematic for the +10 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +10 dBm (0 dBm < TX power ≤ +10 dBm), i.e., the application utilizes the +10 dBm PA to achieve the possible best efficiency at that power level state. The unused RF2G4_IO pin can be grounded directly. Make a short from the pin back to the center exposed pad of the part under the chip.

Table 5.2. Final SMD Values for the +10 dBm PA (3-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.5 %	GRM0335C1H1R9WA01D	Murata
L1	2.1 nH	± 0.1 nH	LQP03HQ2N1B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata

5.1.3 Recommended Combined Matching Network for Both 0/10 dBm PA

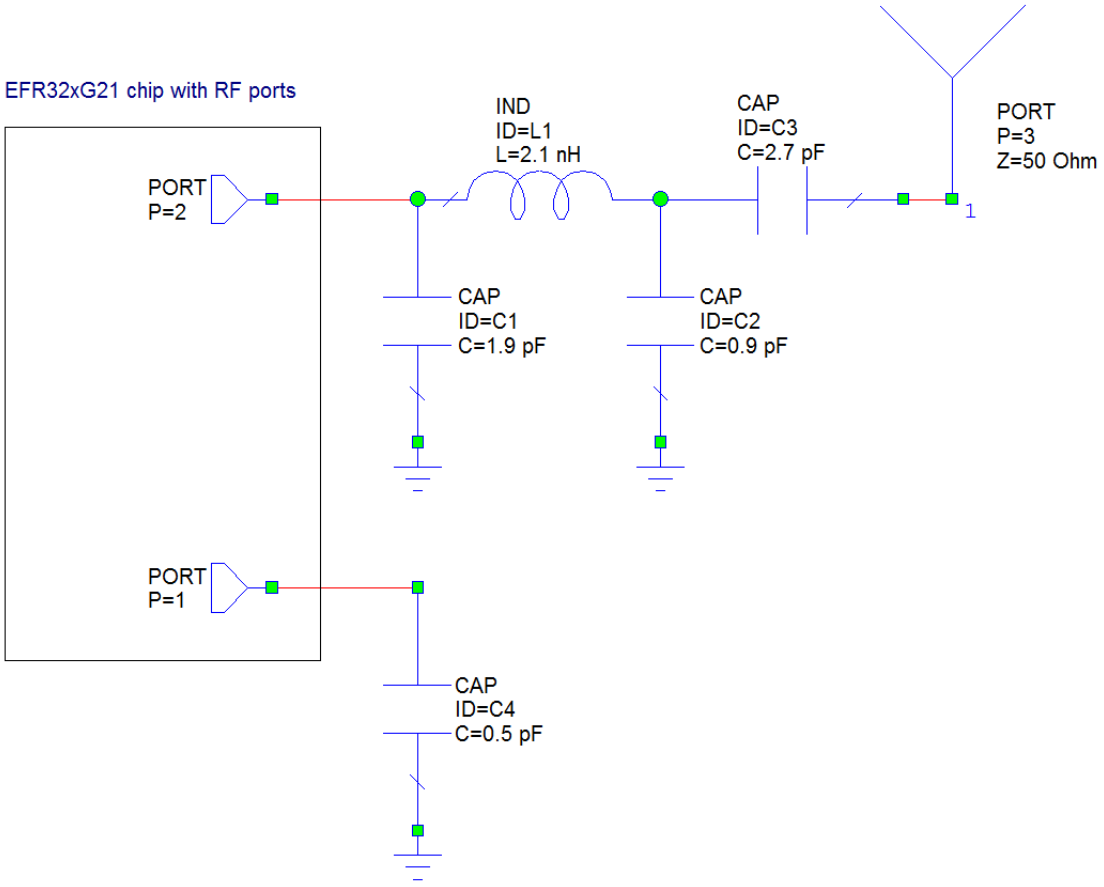

Figure 5.3. Combined Matching Network Schematic for both 0 and +10 dBm PA

Use the matching network shown above when the maximum transmitting power requirement is +10 dBm (TX power ≤ +10 dBm). Use 0 dBm PA for the best power efficiency equal or below 0 dBm. Ground the unused RF2G4_IO pin via an (DC-blocking) 0.5 pF capacitor.

Table 5.3. Final SMD Values for the 0/10 dBm PA Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.5 %	GRM0335C1H1R9WA01D	Murata
L1	2.1 nH	± 0.1 nH	LQP03HQ2N1B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata
C3	2.7 pF	± 0.5 %	GRM0335C1H2R7WA01D	Murata
C4	0.5 pF	± 0.05 pF	GRM0335C1HR50WA01D	Murata

5.1.4 Recommended Matching Network for the +20 dBm PA

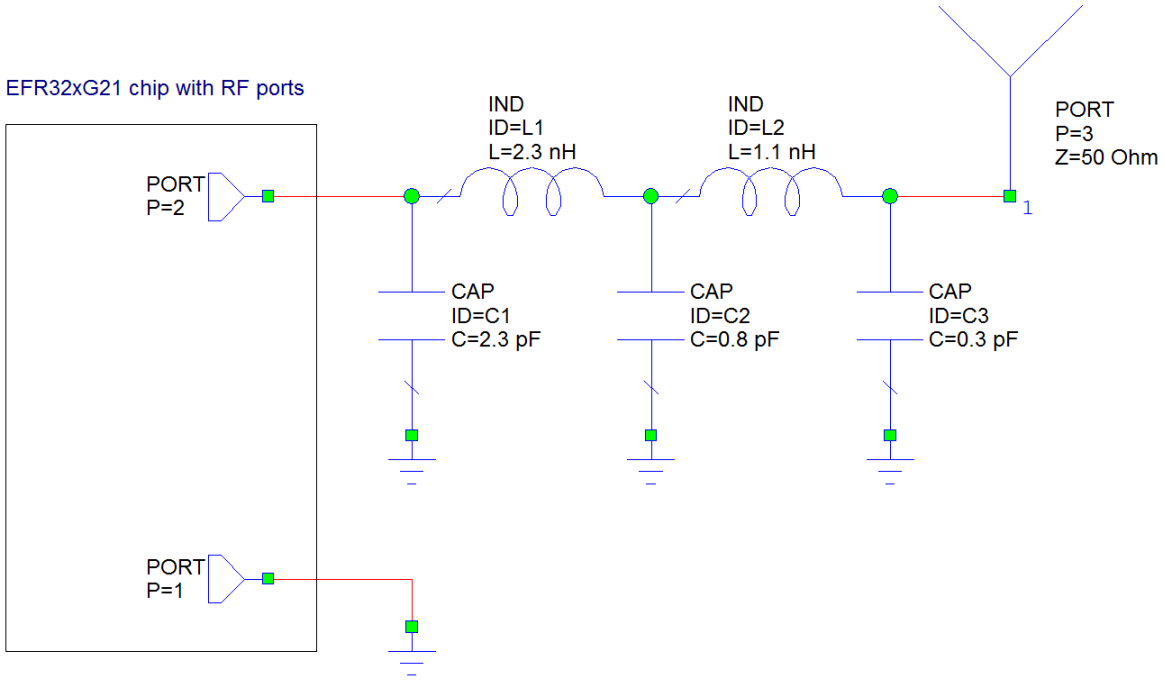

Figure 5.4. Matching Network Schematic for the +20 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +20 dBm (+10 dBm < TX power ≤ +20 dBm), i.e., the application utilizes the +20 dBm PA to achieve the possible highest TX power level available. Due to the optimized power efficiency, the need for 5-element matching network here is mostly driven by the harmonic suppression requirements. The unused RF2G4_IO pin can be grounded directly. Make a short from the pin back to the center exposed pad of the part under the chip.

Table 5.4. Final SMD Values for the +20 dBm PA (5-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01D	Murata
L1	2.3 nH	± 0.1 nH	LQP03HQ2N3B02D	Murata
C2	0.8 pF	± 0.05 pF	GRM0335C1HR80WA01D	Murata
L2	1.1 nH	± 0.05 nH	LQP03HQ1N1W02D	Murata
C3	0.3 pF	± 0.05 pF	GRM0335C1HR30WA01D	Murata

5.1.5 Measurement Results

Table 5.5. Measurement Results for Each Power Level (PA), Avg., Conducted

Match	PA	RX Sensitivity [dBm]	TX Power [dBm]	PA Current [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
0 dBm	0 dBm	-96.4	-0.3	4.3	-60.1	-64.2	-67.9	-60.9
+10 dBm	+10 dBm	-96.5	10.6	29.9	-47.7	-48.8	-48.0	-48.0
0 / 10 dBm	0 dBm	-96.4	-0.4	4.3	-62.1	-68.8	-68.8	-68.8
0 / 10 dBm	+10 dBm	-96.4	10.4	29.9	-62.1	-49.5	-68.1	-45.5
+20 dBm	+20 dBm	-96.3	20.2	178.1	-55.4	-51.5	-52.1	-52.1

RX Sensitivity test conditions: 1Mbps BLE PHY (MSK), BER < 0.1%.

5.2 EFR32xG22 Matching Networks

This section provides matching networks recommended for use with the EFR32xG22 with different layout approaches. It is important to emphasize that the tuned matching component values strongly depend on the layout drawing and so it is recommended to follow the layout guidelines as documented in AN928.2: EFR32 Series 2 Layout Design Guide.

There are two different matching and layout concepts designed for EFR32xG22:

1. Existing layout concept: This layout approach utilizes a short GND trace connection between the first shunt matching capacitor and RFVSS ground pin of the chip, and that first shunt matching capacitor is not connected to any via or component-layer GND pour (except for the exposed chip pad through the RFVSS pin). The second shunt matching capacitor is grounded through a single via to an inner layer's GND plane. Also, there is about 70 mils of total copper keep-out on the component-layer GND pour around the RF matching circuit.
2. Generic layout concept: This layout concept follows more generic RF layout guidelines and no special or unique approach is applied. The shunt matching capacitors are connected to the component-layer GND pour with multiple stitching vias as well and there is about 11 mils of copper keep-out between the matching components and the top layer's GND plane.
3. Pi matching concept: This matching concept utilizes three SMD components in a Pi structure with two shunt capacitors and one series inductor between the two capacitors. Historically, this type of matching concept was initially designed for the EFR32xG22 parts and radio boards are available with this Pi matching configuration (on the existing layout concept). This Pi matching network on the generic layout concept provides good radiated harmonic margins on PCB stack-up configurations when the gap between the top and first inner GND layer is small, i.e., < 150 um.
4. T matching concept: This matching concept utilizes three SMD components in a T structure with two series inductors and one shunt capacitor between the two inductors. This is the most recent matching network designed for the EFR32xG22 parts. Because the first component in the match from the chip is a series inductor, the match provides a high impedance load at the harmonics, and thus good harmonic suppression is achieved. However, there is no issue with the GND coupling between matching elements since there is only one shunt capacitor in the match. It is recommended to connect this single shunt capacitor in the match to the PAVDD side of the GND plane on the top layer. T match is less sensitive to the layout variants, but tested when following the generic layout concept on PCB stack-up configurations when the gap between the top and first inner GND layer is equal with or smaller than 0.8 mm. The best radiated harmonic margin was achieved when utilizing the T-match on Silicon Labs 2- and 4-layer reference boards.

The EFR32xG22 data sheet provides a suggested Pi matching network with the existing layout approach. All data sheet parameters are captured with this configuration. This solution provides excellent conducted RF performance, but it has a drawback: the radiated 5th harmonic can be marginal in FCC certifications. To ensure margins on the radiated 5th harmonic, it is especially important to place the first shunt matching capacitor very close to the chip pins and follow the reference radio board's PCB stack-up. Also, Silicon Labs reference radio boards are available with the existing layout concept.

Silicon Labs recommends following the generic layout concept. This solution is more robust and has bigger margins on the radiated harmonics. The RF performance when following this layout approach is not as sensitive to the PCB stack-up, component spreading, and layout parasitics as the existing layout concept. Additionally, the T-match appears to have better harmonic margins (both conducted and radiated) when using standard PCB stack-up configurations (top and GND layer distance is between 0.15 and 0.8 mm), and also appears to be more robust against different layout concepts.

The EFR32xG22 part is capable of transmitting at the output power level up to +8 dBm. However, higher than +6 dBm TX power output will result in higher current consumption and harmonic levels, and the +8 dBm TXP is not guaranteed over temperature and process variations. Please work with your local Silicon Labs Sales contact to request AN1353-NDA EFR32xG22 8 dBm Use Case Recommendations for more details.

5.2.1 Data Sheet Pi Matching Network Recommendation for Following the Existing Layout Concept

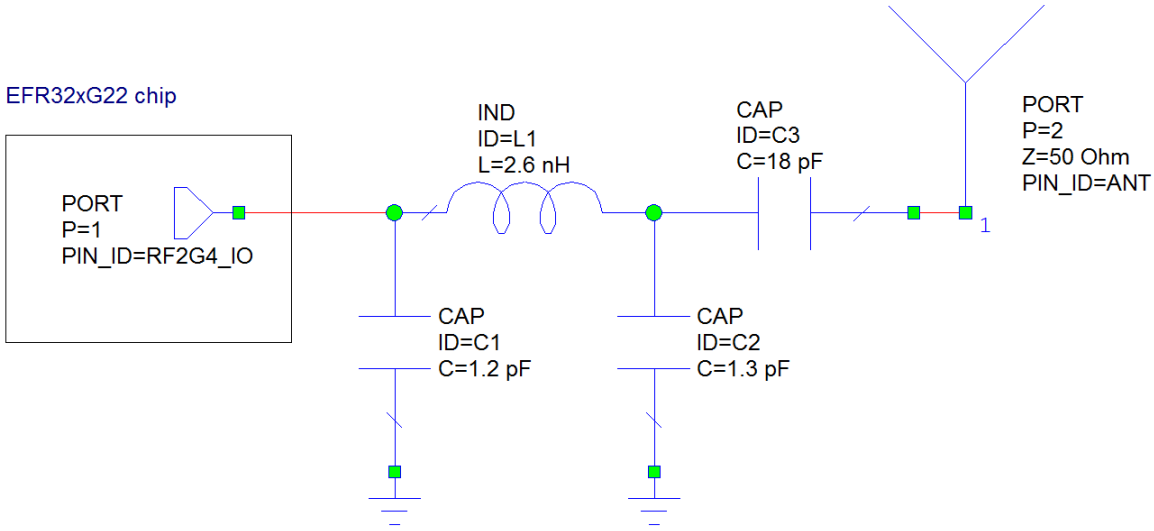

Figure 5.5. Pi Matching Network Schematic Following Existing Layout Concept

Use the matching network shown above with EFR32xG22 for any achievable power level when following the existing layout concept. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm, i.e., simultaneously optimized with the 0 and +6 dBm PA as well.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

Table 5.6. Final SMD Values for the 0/6 dBm PA Pi-Match on a 4-layer PCB when Following the Existing Layout Concept

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.2 pF	± 0.05 pF	GRM0335C1H1R2WA01D	Murata
L1	2.6 nH	± 0.1 nH	LQP03HQ2N6B02	Murata
C2	1.3 pF	± 0.1 pF	GRM0335C1H1R3BA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.2 Recommended Pi Matching Network for Following the Generic Layout Concept

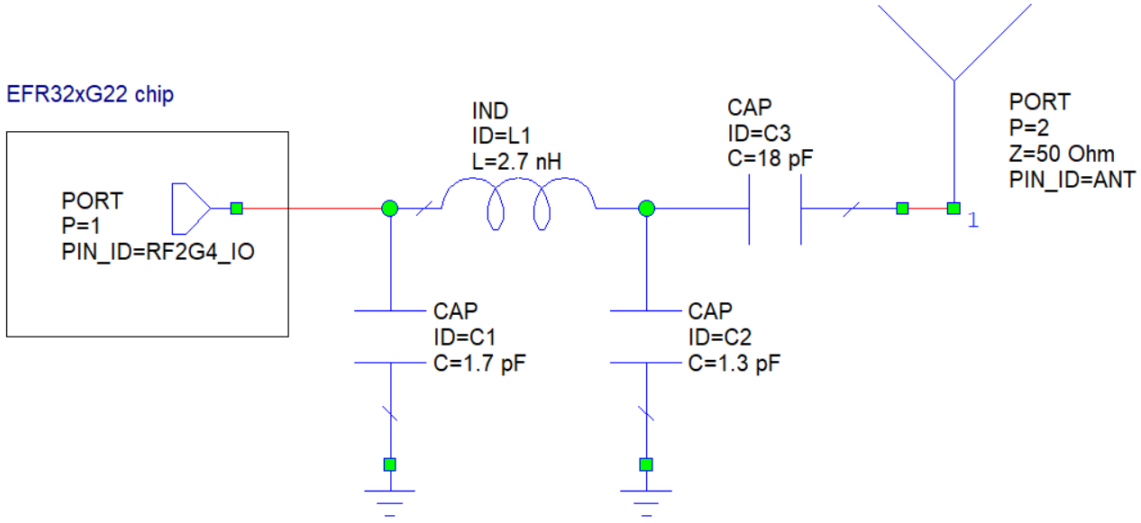

Figure 5.6. Recommended Pi Matching Network Schematic Following the Generic Layout Concept

Use the matching network shown above with EFR32xG22 for any achievable power level on a 2- or more layer PCB where the gap between the top and first inner layer (or bottom layer for 2-layer PCB) is a maximum of 800 µm while following the generic layout concept discussed above. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm. The matching network is simultaneously optimized for both the 0 and +6 dBm PA.

The matching network component values are optimized for PCB stack-up configurations with a separation of maximum 800 µm (32 mils) between the top and first inner layer (or bottom layer for 2-layer PCB). Tested with the standard radio board stack-up with a 0.3 mm gap between the top and first inner layer, with a 4-layer PCB with 0.07 mm gap between the top and first inner layer, and with a 2-layer 32 mils (0.8 mm) thick PCB.

Table 5.7. Final SMD Values for the 0 / 6 dBm PA Pi-Match when Following the Generic Layout Concept

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.7 pF	± 0.1 pF	GRM0335C1H1R7BA01D	Murata
L1	2.7 nH	± 0.1 nH	LQP03TN2N7B02D	Murata
C2	1.3 pF	± 0.1 pF	GRM0335C1H1R3BA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.3 Recommended T Matching Network

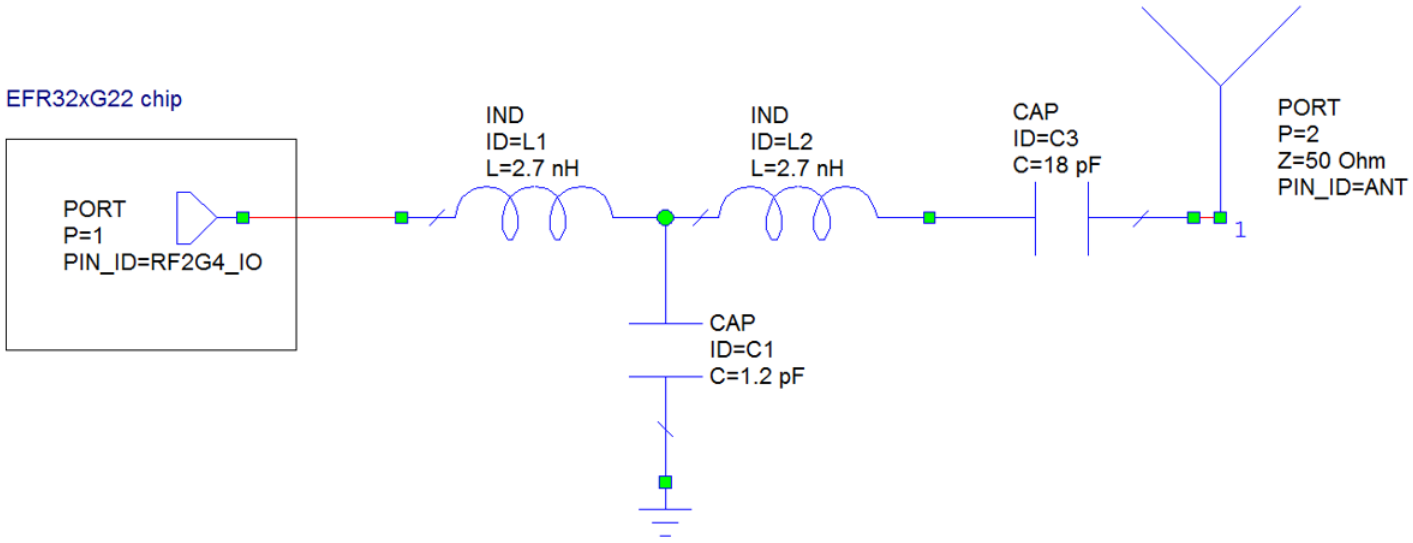

Figure 5.7. Recommended T Matching Network Schematic

Use the matching network shown above with EFR32xG22 for any achievable power level on a 2- or more layer PCB where the gap between the top and first inner layer (or bottom layer for 2-layer PCB) is a maximum of 800 µm while following the generic or existing layout concept discussed above. (Silicon Labs provides performance data when following the generic layout concept). The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +6 dBm. The matching network is simultaneously optimized for both the 0 and +6 dBm PA.

The matching network component values are optimized for PCB stack-up configurations with a separation maximum of 800 µm (32 mils) between the top and first inner layer (or bottom layer for 2-layer PCB). The matching network is tested with the standard radio board stack-up with a 0.3 mm gap between the top and first inner layer and with a 2-layer 32 mils (0.8 mm) thick PCB.

Table 5.8. Final SMD Values for the 0/6 dBm PA T-Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
L1	2.7 nH	± 0.1 nH	LQP03TN2N7B02D	Murata
L2	2.7 nH	± 0.1 nH	LQP03TN2N7B02D	Murata
C1	1.2 pF	± 0.1 pF	GRM0335C1H1R2BA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.2.4 Measurement Results

Table 5.9. Measurement Results for Each Power Level (PA), Avg., Conducted

Layout and Matching Concept	PA	PCB	RX Sensitivity [dBm] [1]	TX Power [dBm]	Current Cons. [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
Existing Pi	0 dBm	4-layer	-98.4	0.2	4.6	-57.1	-62.7	-70 [2]	-70 [2]
Existing Pi	+6 dBm	4-layer	-98.4	6.0 [3]	8.7	-52.0	-46.1	-66.5	-64.8
Generic Pi	+6 dBm	4-layer	-98.5	6.0 [3]	8.9	-54.9	-39.0	-70 [2]	-53.4
Generic Pi	+6 dBm	2-layer	-98.3	6.0 [3]	8.9	-65.0	-36.0	-56.0	-43.0
Generic Pi	0 dBm	2-layer	-98.3	-0.2	4.7	-53.2	-58.5	-70 [2]	-70 [2]
Generic T	+6 dBm	4-layer	-98.3	6.0[3]	8.8	-43.6	-49.8	-70.6	-60.3
Generic T	0 dBm	4-layer	-98.3	0.3	5.0	-54.3	-64.4	-73.1	-71.4
Generic T	+6 dBm	2-layer	-98.4	6.0[3]	8.8	-44.0	-59.0	-67.0	-56.0
Generic T	0 dBm	2-layer	-98.4	0.5	5.2	-59.2	-69.2	-72.7	-72.1

Note:

1. Test conditions: 1 Mbps BLE PHY (MSK), BER < 0.1%.
2. Under SA noise floor.
3. Tested at +6 dBm power level.

5.3 EFR32xG24 Matching Networks

5.3.1 Recommended Combined Matching Network for QFN Packages for Both 0/10 dBm PA

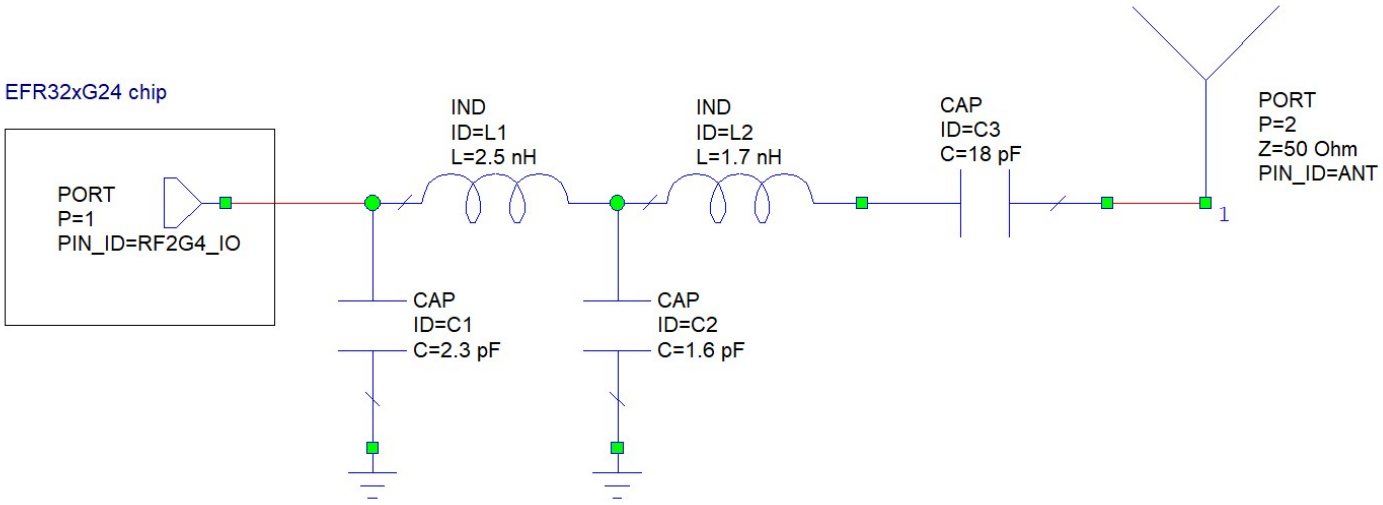

Figure 5.8. Combined Matching Network Schematic for both 0 and +10 dBm PA

Use the matching network shown above with EFR32xG24 for a maximum transmitting power requirement of +10 dBm. The series dc-blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +10 dBm, i.e., simultaneously optimized with the 0 and +10 dBm PA as well.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

Table 5.10. Final SMD Values for the 0/10 dBm PA Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01	Murata
L1	2.5 nH	± 0.05 nH	LQP03HQ2N5W02	Murata
C2	1.6 pF	± 0.05 pF	GRM0335C1H1R6WA01	Murata
L2	1.7 nH	± 0.05 nH	LQP03HQ1N7W02	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01	Murata

5.3.2 Recommended Matching Network for QFN Packages for the 20 dBm PA

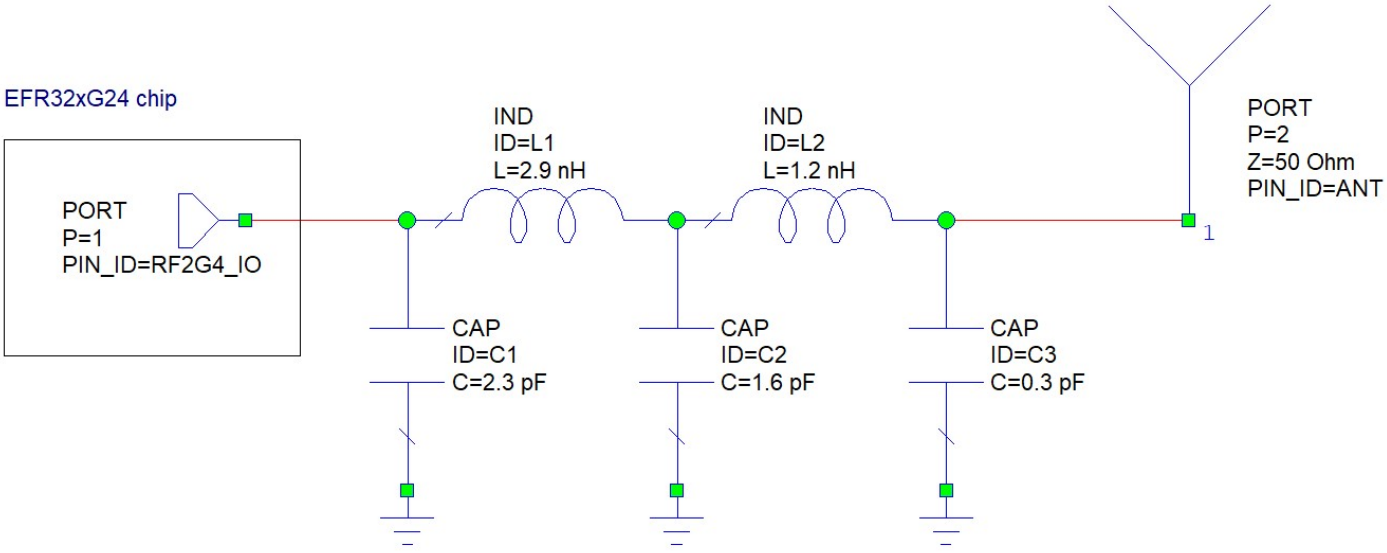

Figure 5.9. Matching Network Schematic for the +20 dBm PA

Use the matching network shown above with EFR32xG24 for a maximum transmitting power requirement of +20 dBm, i.e. the matching network is optimized for the +20 dBm PA.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

Table 5.11. Final SMD Values for the 20 dBm PA Match

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01	Murata
L1	2.9 nH	± 0.1 nH	LQP03HQ2N9B02	Murata
C2	1.6 pF	± 0.05 pF	GRM0335C1H1R6WA01	Murata
L2	1.2 nH	± 0.05 nH	LQP03HQ1N2W02	Murata
C3	0.3 pF	± 0.05 pF	GRM0335C1HR30WA01D	Murata

5.3.3 Recommended Matching Network for WLCSP package for the 0/4 dBm PA

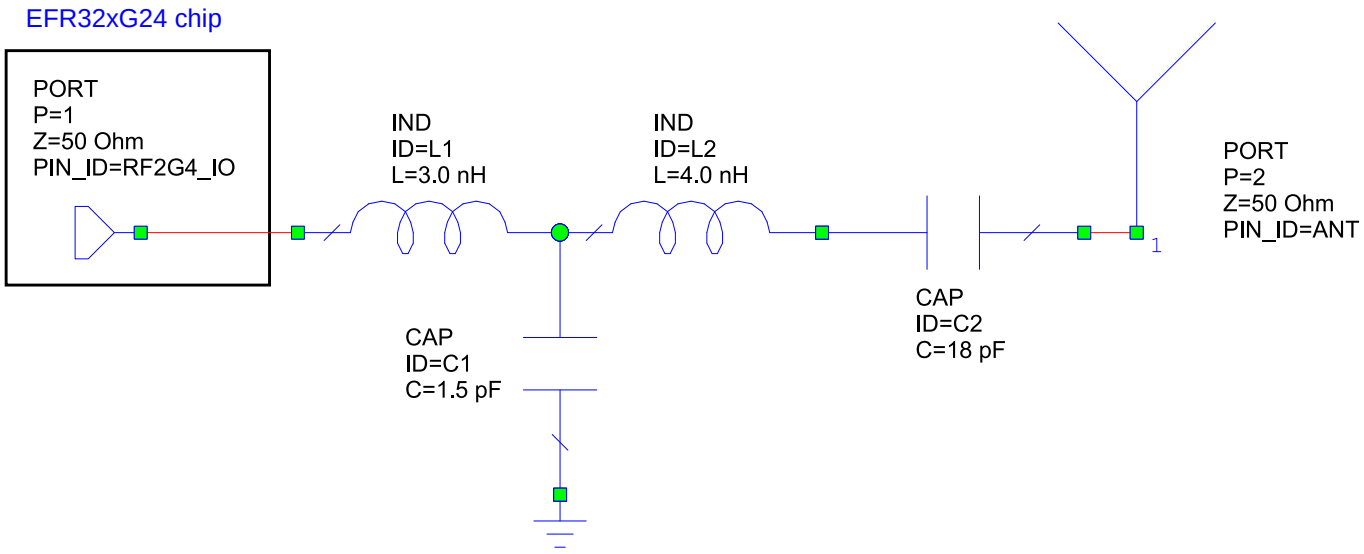

Figure 5.10. Matching Network Schematic for the WLCSP package for the 0/4 dBm PA

Use the matching network shown above with EFR32xG24 WLCSP package for a maximum transmitting power requirement of +4 dBm. The series dc blocking capacitor (C2) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +4 dBm. The matching network is simultaneously optimized for both the 0 dBm and the high-power PA.

The matching network component values are optimized for a 4-layer PCB with a separation of 100 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 100 µm.

Table 5.12. Final SMD Values for the 0/+4 dBm Matching Network for WLCSP Package

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.5 pF	± 0.05 pF	GRM0335C1H1R5WA01D	Murata
L1	3.0 nH	± 0.1 nH	LQP03HQ3N0B02D	Murata
C2	18 pF	± 2 %	GJM0335C1E180GB01D	Murata
L2	4.0 nH	± 0.1 nH	LQP03HQ4N0B02D	Murata

5.3.4 Measurement Results

Table 5.13. Measurement Results for Each Power Level (PA), Avg., Conducted

Package Type	Match	PA	RX Sens. [dBm]	PA Setting [raw]	TXP [dBm]	Total Current [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
QFN	0 / 10 dBm	0 dBm	-97.9	15	-0.5	4.8	-65.9	-69.6	-92	-91.4
QFN	0 / 10 dBm	10 dBm	-97.9	67	10.1	20.8	-51.3	-53.5	-83.5	-66.1
QFN	20 dBm	20 dBm	-97.9	180	20.2	174.3	-50.3	-61.8	-75.5	-60.7
WLCSP	0 dBm	0 dBm	-98.1	15	0	4.8	-55.7	-75.9	-90.3	-78.3
WLCSP	4 dBm	4 dBm	-98.1	17	4.4	11.1	-51.7	-75.7	-89.5	-75.7

Note:
1. RX Sensitivity test conditions: 1 Mbps BLE PHY (MSK), BER < 0.1%.

5.4 EFR32xG27 Matching Networks

EFR32xG27 is available in both QFN (QFN32/QFN40) and WLCSP (WLCSP39) packages. For both QFN and WLCSP packages, the recommended matching network is a T match (L-C-L) with a series dc blocking capacitor. However, the optimal matching network component values depend on the package type.

5.4.1 Recommended Matching Network for QFN Packages

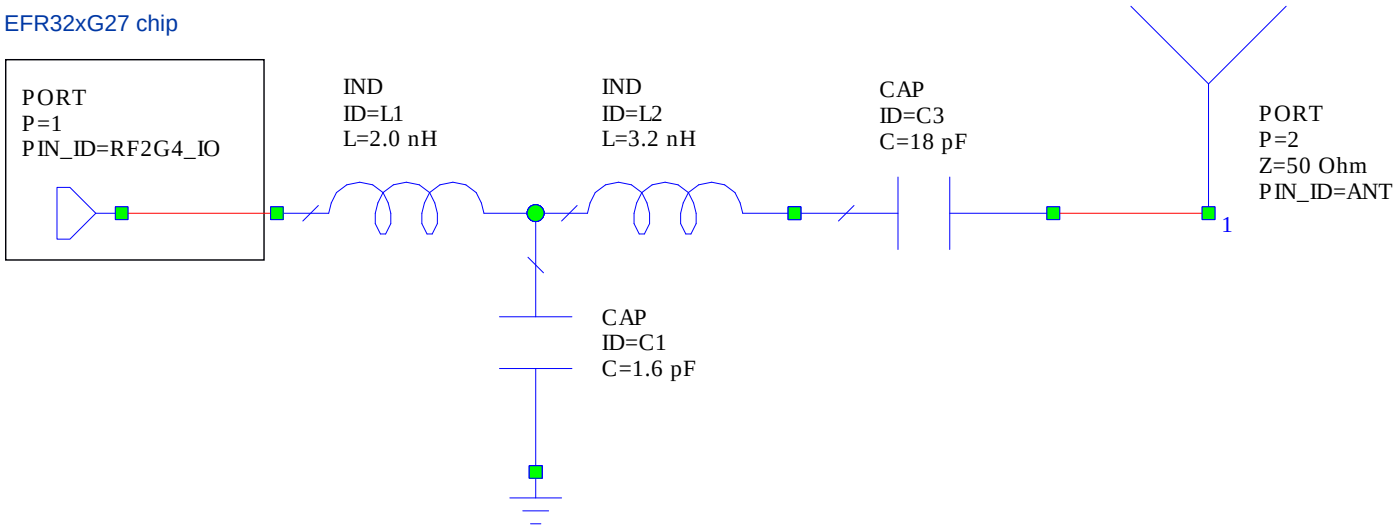

Figure 5.11. Matching Network Schematic for QFN Packages

Use the matching network shown above with EFR32xG27 QFN (QFN32/QFN40) packages for a maximum transmitting power requirement of +8 dBm for the buck and +6 dBm for the boost dc-dc version. The same matching network can be used for both the buck and boost QFN chip variants because the same dc power supply voltage is applied at the PA due to the internal regulator. The series dc blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +8 dBm for the buck and + 6 dBm for the boost version.

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

Table 5.14. Final SMD Values for the 0/+8 and 0/+6 dBm Matching Networks for the Boost and Buck QFN Packages

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
L1	2.0 nH	± 0.2 nH	LQP03TN2N0C02D	Murata
L2	3.2 nH	± 0.2 nH	LQP03TN3N2C02D	Murata
C1	1.6 pF	± 0.05 pF	GRM0335C1H1R6WA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.4.2 Recommended Matching Network for WLCSP Package

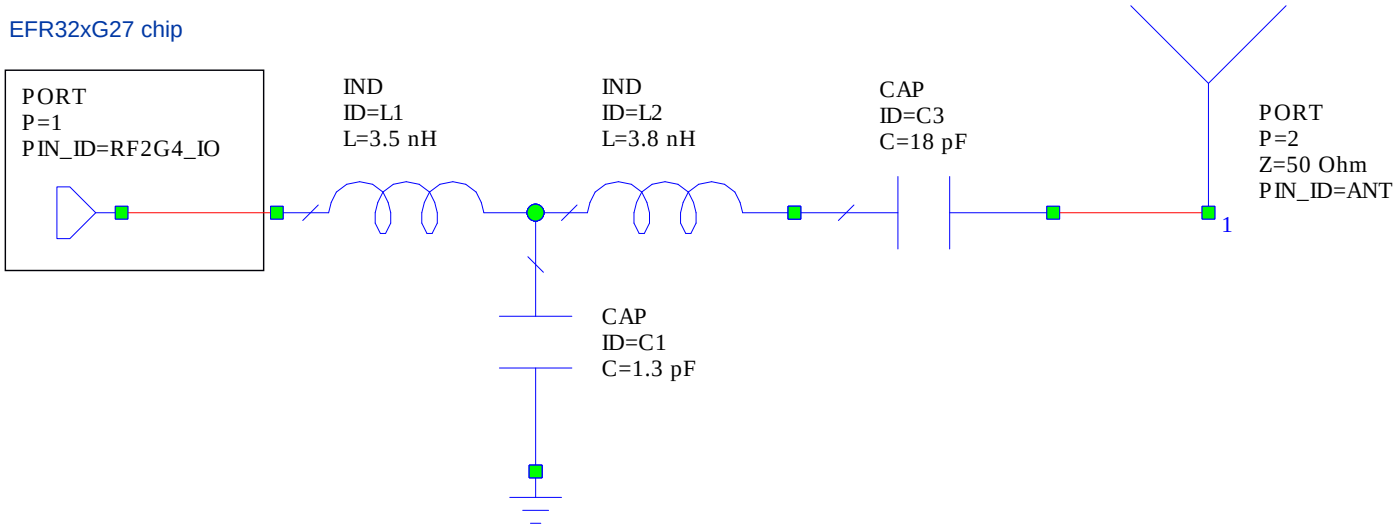

Figure 5.12. Matching Network Schematic for WLCSP Package

Use the matching network shown above with EFR32xG27 WLCSP package for a maximum transmitting power requirement of +4 dBm. The same matching network can be used regardless of the selected dc-dc operation mode (buck or boost) because the same dc power supply voltage is applied at the PA due to the internal regulator. The series dc blocking capacitor (C3) is mandatory when utilizing the 0 dBm PA, but the matching network shown above is optimized for any power level equal or below +4 dBm. The matching network is simultaneously optimized for both the 0 dBm and the high-power PA.

The matching network component values are optimized for a 4-layer PCB with a separation of 100 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 100 µm.

Table 5.15. Final SMD Values for the 0/+4 dBm Matching Network for WLCSP Package

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
L1	3.5 nH	± 0.2 nH	LQP03TN3N5C02D	Murata
L2	3.8 nH	± 0.2 nH	LQP03TN3N8C02D	Murata
C1	1.3 pF	± 0.05 pF	GRM0335C1H1R3WA01D	Murata
C3	18 pF	± 2 %	GJM0335C1E180GB01D	Murata

5.4.3 Measurement Results

Table 5.16. Measurement Results for Each Power Level (PA), Avg., Conducted

Package Type	Match	DC-DC Mode	PA	RX Sens. [dBm]	PA Setting [raw]	TXP [dBm]	Total Current [mA]	H2 max [dBm]	H3 max [dBm]	H4 max [dBm]	H5 max [dBm]
QFN Buck	0/+8 dBm	Buck (default)	0 dBm	-97.9	15	-1.0	4.6	-52.2	-65.0	-72.3	-63.0
			+8 dBm		127	8.0	11.8	-45.2	-56.3	-69.2	-54.5
QFN Boost	0/+6 dBm	Boost (default)	0 dBm	-97.0	15	-0.9	9.4	-58.1	-65.0	-73.1	-63.7
			+6 dBm		63	6.0	19.5	-41.5	-62.0	-70.5	-53.0
WLCSP39	0/+4 dBm	Buck	0 dBm	-98.0	15	0.3	4.6	-51	-70	-90.7	-78
			+4 dBm		40	4.3	8.3	-43.2	-64.7	-90.7	-71.6
	0/+4 dBm	Boost	0 dBm	-97.9	15	0.3	9.3	-52.0	-66.0	-89.9	-79.0
			+4 dBm		40	4.2	16.4	-50.4	-56.6	-90.6	-73.6

Note:
1. RX Sensitivity test conditions: 1 Mbps 500 kHz 2GFSK PHY, BER < 0.1%.

5.5 EFR32xG28 Matching Networks

EFR32xG28 dual-band variants support 2.4 GHz BLE operation up to the TX output power level of +10 dBm.

5.5.1 Recommended Matching Network

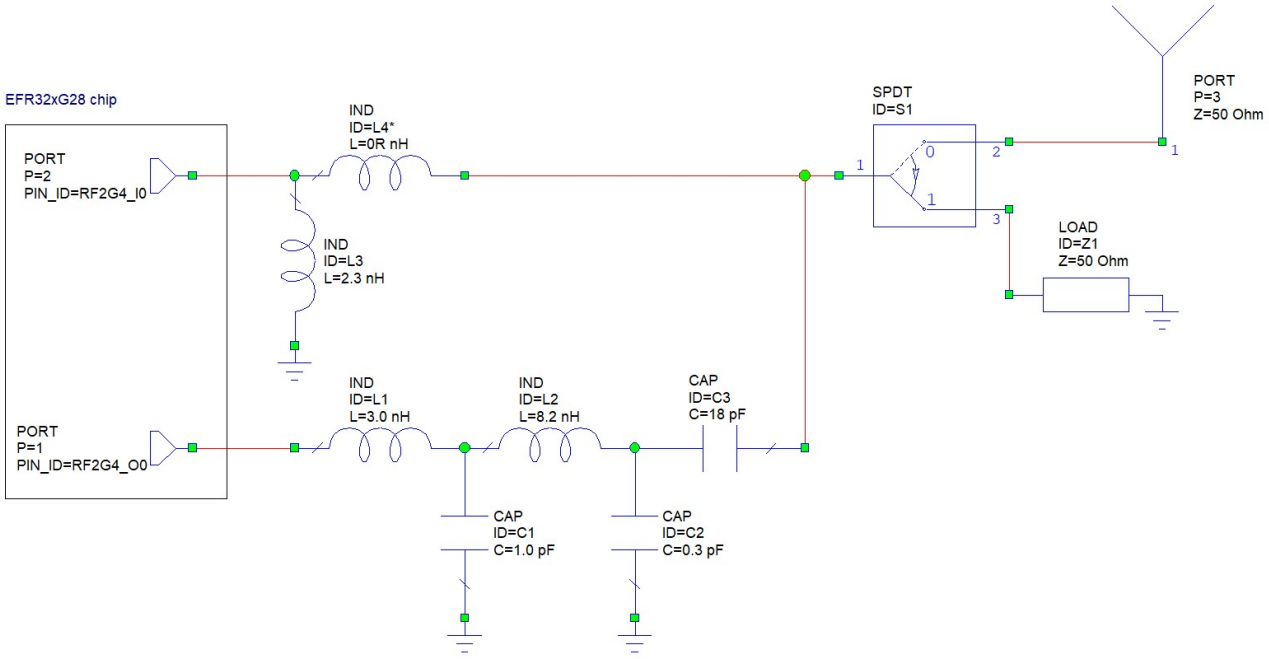

Figure 5.13. Matching Network Schematic for 2.4 GHz

Use the 2.4 GHz matching network shown above with the EFR32xG28 dual-band chip variants for a maximum transmitting power requirement of +10 dBm at the 2.4 GHz frequency. The separate PAVDD pin supplies both internal +10 dBm 2.4 GHz and +14/20 dBm sub-GHz PA and is recommended to feed the PA from the DCDC output (VREGSW). Dual-band variants that require TXP above +14 dBm at the sub-GHz frequencies must have the PAVDD pin connected to the main power supply voltage (e.g., 3.3 V).

The matching network component values are optimized for a 4-layer PCB with a separation of 300 µm between the top (component side) and first inner (GND) layer. These values can be used for a PCB with more layers as well, if the distance between the top (matching circuit component side) and first inner layer is kept close to 300 µm.

L4 series matching inductor in the RX path is replaced by a 0R resistor on the Silicon Labs reference designs. Here, the matching component is basically the RX trace which is connected between the RX pin and TX matching network output, and its inductance is estimated to be around 4 nH. The SPDT switch is supposed to terminate the 2.4 GHz path by a 50 Ω resistor when the EFR32xG28 device transmits at the sub-GHz frequencies.

Table 5.17. Final Component/SMD Values for the +10 dBm 2.4 GHz Matching Network

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
L1	3.0 nH	± 0.1 nH	LQP03HQ3N0B02D	Murata
L2	8.2 nH	± 3 %	LQP03HQ8N2H02D	Murata
L3	2.3 nH	± 0.1 nH	LQP03HQ2N3B02D	Murata
L4	0R		0R resistor	any
C1	1.0 pF	± 0.05 pF	GRM0335C1H1R0WA01D	Murata
C2	0.3 pF	± 0.05 pF	GRM0335C1HR30WA01D	Murata
C3	18 pF	± 2 %	GRM0335C1H180GA01D	Murata
S1	Switch		BGS12WN6E6327XTSA1	Infineon
Z1	50R		50R resistor	any

Table 5.18. Measurement Results at 2.4 GHz, Avg., Conducted

Power Level	DCDC Config.	RX Sens. [dBm]	PA Level [raw]	TXP [dBm]	Total Current [mA]	H2 [dBm]	H3 [dBm]	H4 [dBm]	H5 [dBm]
Nominal	CCM	-95.6	155	10.0	23.15	-50.0	-55.7	-48.5	-57.5
Max.	CCM	-95.6	240	11.4	28.43	-48.7	-57.8	-48.0	-50.0

Note:
1. RX sensitivity test condition: 1 Mbps BLE PHY 37 byte, BER < 0.1 %

6. Appendix 1 PA Optimum Termination Impedance on EFR32xG21

The matching network should present an optimum impedance for the PA at the RF2G4_IO pin for the best RF performance if a 50 Ω termination is applied at the antenna port. The optimum impedance depends on the power level and is also different depending on which internal PA is actively used. The optimum impedances are determined empirically by load-pull methods. The load-pull curves for each PA are shown in the following figures below.

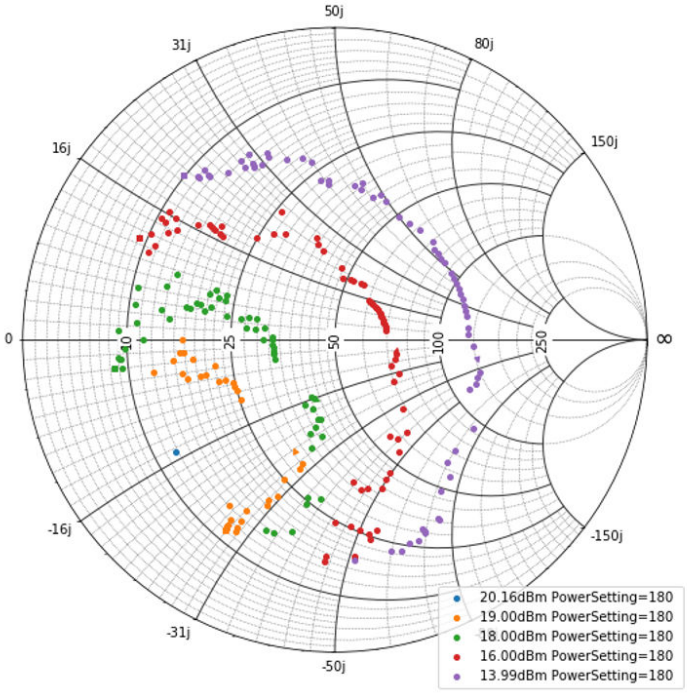

Figure 6.1. Load-pull curves for the 20 dBm PA

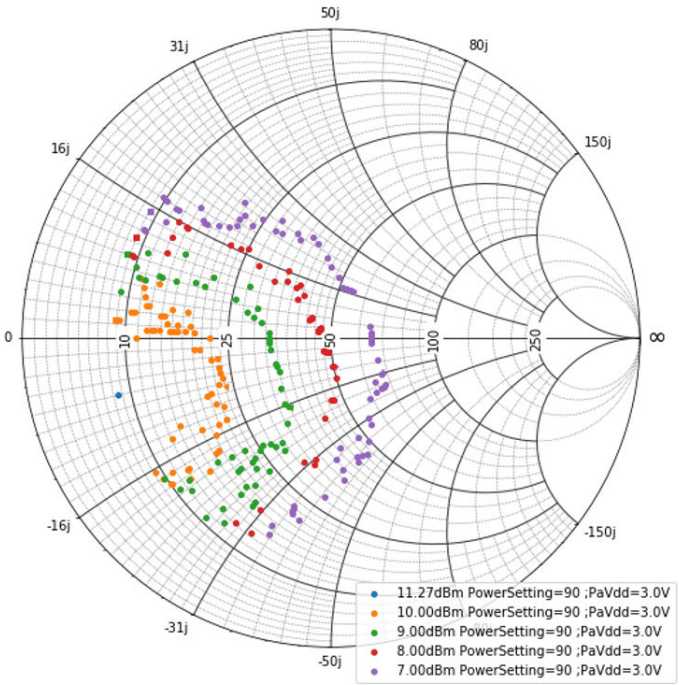

Figure 6.2. Load-pull curves for the 10 dBm PA

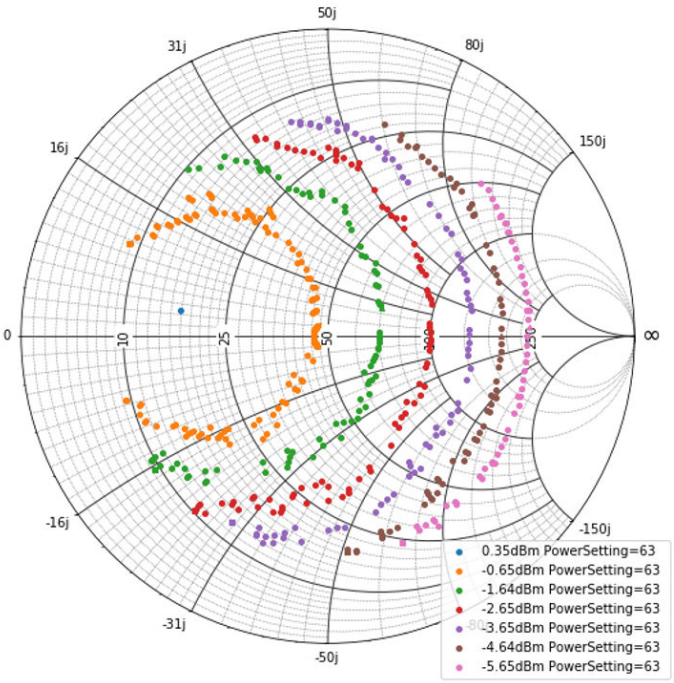

Figure 6.3. Load-pull curves for the 0 dBm PA

7. Revision History

Revision 1.3

September 2023

- Added content for EFR32xG24 WLCSP package.
- Corrected EFR32xG27 optimal load impedance information.
- Added measurement results for EFR32xG27 WLCSP package.

Revision 1.2

August 2023

- Added content for EFR32xG28 devices.

Revision 1.1

July 2023

- Updated EFR32xG21 to include revision EFR32xG21-C.

Revision 1.0

June 2023

- Added content for EFR32xG27 part number designation.

Revision 0.9

April 2022

- Various updates.

Revision 0.8

March 2022

- Added content for EFR32xG24 part

Revision 0.7

August 2021

- Added T-matching network recommendation for EFR32xG22 parts

Revision 0.6

February 2021

- Removed diversity applications language from sections 3.1 EFR32xG21 RF Front-End Overview and 4.1.1 EFR32xG21 Optimum PA Load Impedance.

Revision 0.5

November 2020

- Updated EFR32xG22 generic recommended matching network

Revision 0.4

May 2020

- Added matching recommendation for EFR32xG22 on a 4-layer thin PCB with +8 dBm test data

Revision 0.3

March 2020

- Added content for EFR32xG22 part

Revision 0.2

November 2019

- Highlighting that 0 dBm PA requires to be DC-blocked
- Updating load-pull impedance data and adding load-pull impedance curves for each PA
- Adding discrete 4-element combined 0 / 10 dBm PA match

Revision 0.1

February 2019

Initial release.

Simplicity Studio

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