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AN933.1: EFR32 Series 1 Minimal BOM

The purpose of this application note is to illustrate bill-of-material (BOM)-optimized solutions for sub-GHz and 2.4 GHz applications using the EFR32 Wireless Gecko Portfolio.

Silicon Labs reference radio board designs typically use an extensive number of components for RF and V_{DD} filtering to achieve the best possible RF performance at even the highest output power levels. However, a number of these elements can be eliminated from the design while still maintaining an acceptable RF performance, especially at the lower power levels. This document shows an absolute minimal BOM solution for the EFR32 devices, mainly applicable for Bluetooth Smart applications (i.e. BLE) at the 2.4 GHz frequency band, where the maximum allowed fundamental RF power is generally lower and the design is typically space constrained, such as for wearable applications. Additionally, this application note includes measured and tuning data with several different and simplified VDD filtering approaches at the sub-GHz frequency region. The RF front-end matching principles are described in more detail in the application notes, AN930.1: EFR32 Series 1 2.4GHz Matching Guide and AN923: EFR32 sub-GHz Matching Guide. The RF performance also strongly depends on the PCB layout as well as the design of the matching networks. For optimal performance, Silicon Labs also recommends using the PCB layout design hints described in the application note, AN928.1: EFR32 Layout Design Guide.

KEY POINTS

- BOM & PCB space-optimized reference design for sub-GHz and 2.4 GHz applications
- Eliminates a number of components for RF and V_{DD} domains while maintaining acceptable RF performance
- Measurement results for RX sensitivity, TX performance, and harmonics are provided
- Schematic file is provided

1. Design Considerations

This section summarizes the requirements and considerations for the BOM-optimized designs.

- EFR32 internal, dc-dc converter used for supplying the following V_{DD} rails: DVDD and RFVDD.
- The on-chip dc-dc converter needs an external inductor and capacitor for proper operation.
- For low-power applications (< +14 dBm), it is also generally recommended to supply the PA (PAVDD pin) from the on-chip dc-dc converter in order to achieve better current consumption (i.e., better power efficiency) and immunity against the battery voltage level drop and to avoid output power / RF range degradation due to battery aging.
- For higher power applications (≥ +14 dBm) the PAVDD needs to be connected to the main VDD (e.g., battery).
- For situations where the PA is supplied from the on-chip dc-dc converter, filtering is required on the PAVDD line in order to avoid RF performance degradation (e.g., receiver sensitivity hit). A series ferrite or inductor on the PAVDD line is recommended, especially for the 2.4 GHz applications. Furthermore, stronger harmonic filtering is also required in the RF front-end path.
- For BLE 2.4 GHz applications, EFR32 requires a 32 kHz external crystal to meet the BT Sleep Clock accuracy specification of 500 ppm. Load capacitors are not needed (see section 4. Crystal Requirements for the XTAL requirements). This XTAL can be eliminated from the BOM if this accuracy is not required (e.g. non-BT applications). The 32 kHz crystal can also be eliminated if very low-power sleep mode operation is not required, which will enable the EFR32 to run the high-frequency crystal oscillator to provide the required accuracy.
- The high frequency XTAL is required for operation of RF and MCU parts of the EFR32. Load capacitors are not needed. See section 4. Crystal Requirements. for the XTAL requirements.
- For low-power (≤ +10 dBm) 2.4 GHz applications, the RF front-end matching consists of a series inductor and a parallel capacitor that matches the PA and filters the harmonics. For higher power (> +10 dBm) 2.4 GHz applications, Silicon Labs recommends using the 4-element L-C ladder structure for matching and filtering in the RF-FE path.
- The sub-GHz matching circuit contains discrete capacitors, inductors, and an external balun.
- The following power supply restrictions need to be followed on the EFR32 devices:
  - VREGVDD must be the highest voltage in the system for EFR32.
  - VREGVDD = AVDD
  - DVDD ≤ AVDD
  - IOVDD ≤ AVDD
  - RFVDD ≤ AVDD
  - PAVDD ≤ AVDD
  - DVDD > DECOUPLE

2. Recommended BOM-optimized 2.4 GHz Solution

The recommended RF schematic for minimal BOM option for 2.4 GHz low power (≤ +10 dBm) designs using EFR32 wireless MCUs is shown in the figure below:

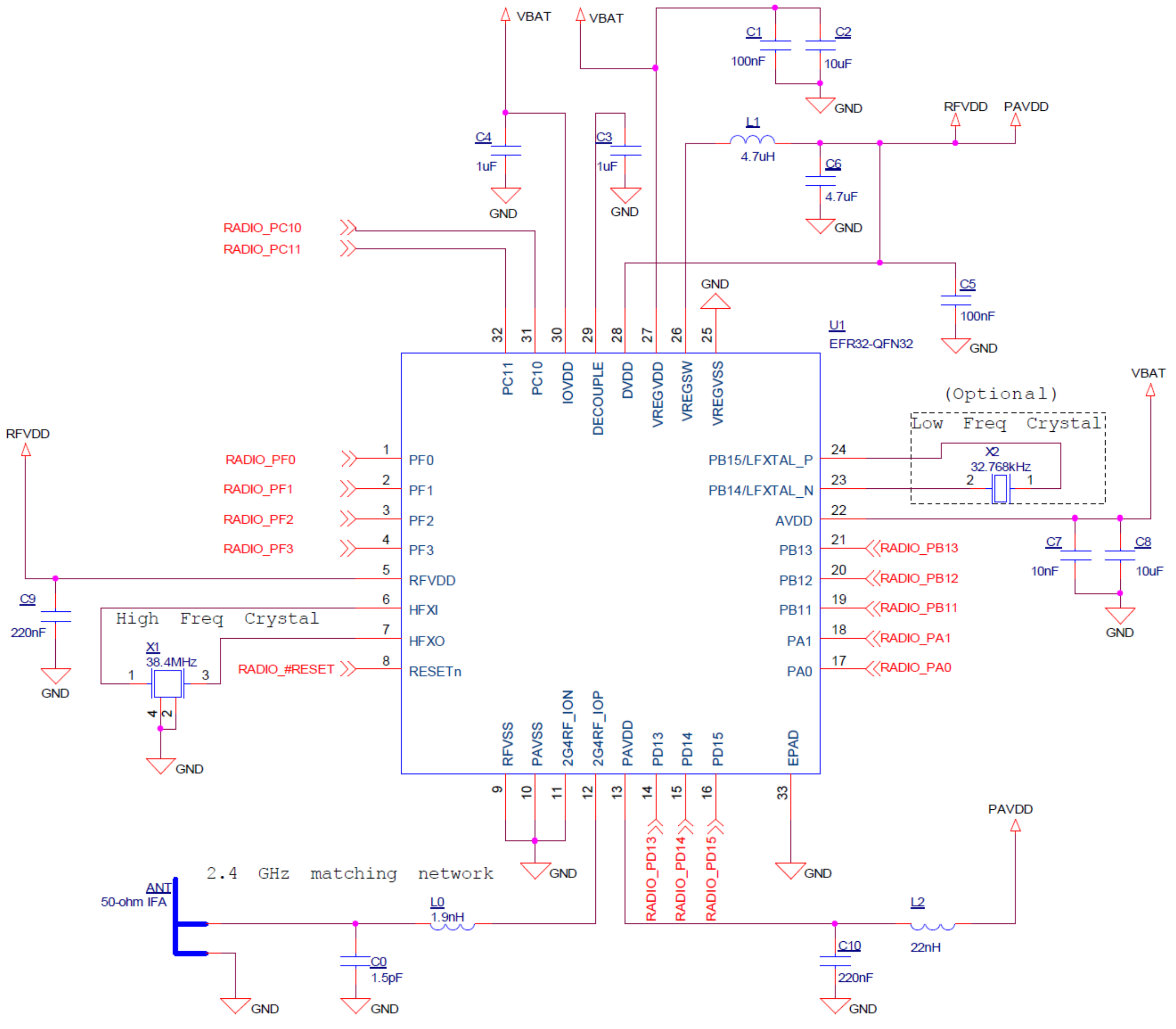


Figure 2.1. Minimal BOM 2.4 GHz Schematic for EFR32

C6 was 1.0 µF in previous revisions of this application note. Although 1.0 µF can still be used, 4.7 µF is now recommended for new designs due to its improved performance under dynamic load conditions and during mode changes. Silicon Labs EFR32xG1 reference radio boards use 1 µF and therefore EFR32xG1 software defaults to using 1 µF (use of emuDcdcLnCompCtrl_1u0F rather than emuDcdcLnCompCtrl_4u7F). Use of 4.7 µF on EFR32xG1 requires changes to this Low Noise Mode Compensator Control emuDcdcLnCompCtrl. See *AN0948: EFM32 and EFR32 Series 1 Power Configurations and DC-DC* sections 4.1 and 6.1 for more details. ERF32xG12 and later reference radio boards use 4.7 µF and EFR32xG12 and later software defaults to 4.7 µF.

Note: Many applications do not require the use of an external LFXO 32.768 kHz (X2 above). See 4. Crystal Requirements for additional details.

2.1 Measured Performance Data

The measurements were done on Silicon Labs' reference radio board: PCB4100A RevB00 based on the RF schematic shown in Figure 2.1 Minimal BOM 2.4 GHz Schematic for EFR32 on page 3.

Table 2.1. RX Sensitivity

PAVDD filtering				RFVDD filtering			Ferrite on AVDD	Input Power [dBm]	PER [%]
Series Ferrite/ Inductor	Parallel Capacitors			Series Ferrite/ Inductor	Parallel Capacitors				
600R ferrite	—	220 nF	—	600R ferrite	10 pF	100 pF	Yes	–98.1	1.08
600R ferrite	—	220 nF	—	600R ferrite	—	220 nF	Yes	–98.1	1.17
600R ferrite	—	220 nF	—	—	—	220 nF	Yes	–98.1	1.03
600R ferrite	—	220 nF	—	—	10 pF	220 nF	Yes	–98.1	1.38
—	—	220 nF	—	—	—	220 nF	Yes	–93.1	1.42
—	10 pF	220 nF	—	—	—	220 nF	Yes	–93.9	1.51
—	10 pF	220 nF	2.2 µF	—	—	220 nF	Yes	–94.8	1.52
—	10 pF	—	—	—	—	220 nF	Yes	–94.6	1.36
600R ferrite	10 pF	—	—	—	—	220 nF	No	–98.2	1.19
600R ferrite	10 pF	—	—	—	—	220 nF	No	–98.4	1.05
22 nH inductor	10 pF	—	—	—	—	220 nF	No	–98.4	1.16
22 nH inductor	10 pF	2.2 µF	—	—	—	220 nF	No	–98.4	1.03
22 nH inductor*	—	220 nF	—	—	—	220 nF	No	–98.4	1.13
—	—	220 nF	—	—	—	220 nF	No	–94.8	1.22

Note: PAVDD is connected to the on-chip dc-dc converter. Better sensitivity results cannot be achieved by placing filtering capacitors at the RF frequencies (i.e. values in the pF range) close to the dc-dc output (VREGSW) pin in parallel with the C6 capacitor. The sensitivity was checked with standard ZigBee packets and the numbers are mainly given for comparison purposes between the different VDD filtering cases. If there is no series filtering on the PAVDD line, 3-4 dB sensitivity degradation can be observed. The best performer of the minimal BOM options is noted with an asterisk "*".

Table 2.2. TX Power and Harmonics

PAVDD filtering			RFVDD filtering			Number of Matching Components	Fund. [dBm]	2nd harm. [dBm]	3rd harm. [dBm]
Series Ferrite/ Inductor	Parallel Capacitors		Series Ferrite/ Inductor	Parallel Capacitors					
600R ferrite	10 pF	220 nF	600R ferrite	10 pF	220 nF	2	10.05	–39.4	–59.3
600R ferrite	10 pF	220 nF	—	—	220 nF	2	10.08	–39.5	–60.3
600R ferrite	—	220 nF	—	—	220 nF	2	10.11	–39.2	–59.8
22 nH inductor	—	220 nF	—	—	220 nF	2	10.12	–39.1	–60
22 nH inductor	—	220 nF	—	—	220 nF	0	10.27	–39.3	–34.2
22 nH inductor	—	220 nF	—	—	220 nF	4	10.53	–59.2	–67
22 nH inductor	—	220 nF	—	—	220 nF	2	0.71	–55.1	–67
22 nH inductor	—	220 nF	—	—	220 nF	0	0.15	–42.4	–49.8

Note: Same TX performance with extra ferrite on the AVDD line. PA power parameters have been set for the different output power levels for the different match cases. The numbers are mainly given for comparison purposes between the different VDD filtering cases. The table above demonstrates that the harmonic levels are not sensitive for filtering the different VDD rails, but mainly depend on the RF-FE matching.

2.2 Additional Concerns

This section lists some additional concerns regarding the RF performance versus different BOM options, and provides some further suggestions on the space constraint layout designs.

- The series inductor or ferrite on the PAVDD line is required to filter the noises generated by the on-chip dc-dc converter. It can be eliminated if the dc-dc converter is not used for supplying the PAVDD.
- The investigation of RF performance (mostly power efficiency and harmonics suppression) versus BOM options for the RF matching network is discussed in more detail in the application note, AN930.1: EFR32 Series 1 2.4GHz Matching Guide.
- If the on-chip dc-dc converter is not used, the following components can be eliminated from the schematic shown in Figure 2.1 Minimal BOM 2.4 GHz Schematic for EFR32 on page 3 L2, L1, and C6.
- If the series inductor or ferrite is deleted from the BOM, but the PA is still supplied from the on-chip dc-dc converter, a 3-4 dB sensitivity degradation can be expected.
- The DVDD can be directly connected to the dc-dc output after the series inductor on the VREGSW pin. There is no need for extra filtering with series ferrite or inductor, but a parallel 100 nF capacitor is suggested on the DVDD pin.
- Ensuring 1-1 additional 10 pF capacitors on both RFVDD and PAVDD lines (in parallel with C9 and C10 in Figure 2.1 Minimal BOM 2.4 GHz Schematic for EFR32 on page 3) will enable better filtering effects at the RF frequencies, if the BOM and space is not so limited.
- The RF front-end matching requires a series inductor with a parallel capacitor. For higher than +10 dBm power output, the 4-element matching network needs to be used to have enough margin at the harmonics. The RF front-end matching principles are described in more detail in application note, AN930.1: EFR32 Series 1 2.4GHz Matching Guide. Generally, stronger filtering is required when the PAVDD is supplied from the on-chip dc-dc converter.
- Even in space-constrained designs, it is strongly recommended to place the L1 and C6 components (at the on-chip dc-dc converter output) as close to the EFR32 wireless MCU's VREGSW pin as possible. Also, the L1 dc-dc inductor should be placed far away from any noise-sensitive circuitry (e.g. radio antenna).
- The high frequency crystal also needs to be placed close to the EFR32 wireless MCU. The XTAL does not require external load capacitors. See section 4. Crystal Requirements. for the XTAL requirements.

3. Recommended BOM-optimized sub-GHz Solution

This section summarizes the measured performance data in the sub-GHz freqeuncy region with several different and simplified VDD rail filtering approaches. The measurements were done on Silicon Labs' reference radio boards: PCB4150B, PCB4152A, and PCB4150A.

3.1 RX Sensitivity

Table 3.1. High-Band; PCB4150B RevC00; PAVDD Connected to DC-DC

PAVDD Filtering				RFVDD Filtering			Ferrite on AVDD	Input Power [dBm]	PER [%]
Series Ferrite/ Inductor	Parallel Capacitors			Series Ferrite/ Inductor	Parallel Capacitors				
—	—	—	56 pF	600R	100 pF	10 pF	Yes	-103	1.0
—	—	—	56 pF	600R	100 pF	10 pF	No	-103	1.0
—	—	—	56 pF	—	100 pF	10 pF	No	-103.5	1.0
—	—	—	56 pF	—	—	220 nF	No	-103	1.0
600R	—	—	56 pF	—	—	220 nF	No	-103	1.0
—	—	—	220 nF	—	—	220 nF	No	-103	1.0

Note: Reference RX sensitivity number: -103.5 dBm at PER = 1% when the PAVDD is connected to VMCU. The sensitivity was checked with O-QPSK DSSS 1:8, 100 kbps DR and 200 kHz deviation at 902 MHz. The numbers are mainly given for comparison purposes between the different VDD filtering cases.

Table 3.2. Low-Band; PCB4152A RevB00; PAVDD Connected to DC-DC

PAVDD Filtering				RFVDD Filtering			Ferrite on AVDD	Input Power [dBm]	PER [%]
Series Ferrite/ Inductor	Parallel Capacitors			Series Ferrite/ Inductor	Parallel Capacitors				
470 nH	—	—	270 pF	600R	100 pF	10 pF	Yes	-106	1.0
470 nH	—	—	270 pF	600R	100 pF	10 pF	No	-106	1.0
470 nH	—	—	270 pF	—	100 pF	10 pF	No	-106	1.0
470 nH	—	—	270 pF	—	—	220 nF	No	-106	1.0

Note: Reference RX sensitivity number: -106 dBm at PER = 1% when the PAVDD is connected to VMCU. The sensitivity was checked with FSK, 62.5 kbps DR and 40 kHz deviation at 431 MHz. The low frequency band designs need to use series choke inductors on the PAVDD rail, because of the external balun topology and the need of PA biasing. The numbers are mainly given for comparison purposes between the different VDD filtering cases.

The tables above show that the receiver sensitivity does not change over the different and simplified VDD rail filtering cases, even if the PA is supplied from the on-chip dc-dc converter. These tests are performed in a conducted way. In order to avoid radiated senstivity degradation, the dc-dc inductor should be placed far away from any noise-sensitive circuitry, such as a radio antenna.

3.2 TX Power and Harmonics

Table 3.3. High-band; PCB4150A RevC00; PAVDD connected to DC-DC

PAVDD filtering			RFVDD filtering			Ferrite on AVDD	Fund. [dBm]	2nd harm. [dBm]	3rd harm. [dBm
Series Ferrite/ Inductor	Parallel Capacitors		Series Ferrite/ Inductor	Parallel Capacitors					
—	—	56 pF	600R	100 pF	10 pF	Yes	14.1	-40.2	-48
600R	—	56 pF	120 nH	220 nF	56 pF	No	13.9	-38.9	-48
—	—	56 pF	600R	220 nF	56 pF	No	14	-39.2	-48
—	—	56 pF	—	220 nF	56 pF	No	14	-38.3	-48
—	—	56 pF	—	—	220 nF	No	14	-38	-48
—	—	56 pF	120 nH	—	56 pF	No	13.9	-39.2	-48
—	—	56 pF	120 nH	—	220 nF	No	14	-40	-48
—	—	56 pF	120 nH	220 nF	56 pF	No	14	-40.1	-48

Note: The fundamental RF frequency was 868 MHz. The numbers are mainly given for comparison purposes between the different VDD filtering cases. As shown in the table above, there is a slight difference on the 2nd harmonic level depending on the strenght of the RFVDD filtering.

Table 3.4. Low-band; PCB4152A RevB00; PAVDD connected to DC-DC

PAVDD filtering			RFVDD filtering			Ferrite on AVDD	Fund. [dBm]	2nd harm. [dBm]	3rd harm. [dBm
Series Ferrite/ Inductor	Parallel Capacitors		Series Ferrite/ Inductor	Parallel Capacitors					
470 nH	—	270 pF	600R	100 pF	10 pF	Yes	12.4	-48	-48
470 nH	—	270 pF	600R	100 pF	10 pF	No	12.4	-48	-48
470 nH	—	270 pF	—	100 pF	10 pF	No	12.4	-48	-48
470 nH	—	270 pF	—	—	220 nF	No	12.4	-48	-48

Note: The fundamental RF frequency was 434 MHz. The numbers are mainly given for comparison purposes between the different VDD filtering cases. As shown in the table above, the harmonic levels are not sensitive for the different and simplified VDD rail filtering cases.

3.3 DC-DC Converter's Switching Frequency Spur

In some cases, the switching frequency (~7 MHz) of the internal dc-dc converter can be modulated onto the RF and can appear in the TX spectrum. To achieve the best possible suppression on these spurs, Silicon Labs recommends to use series ferrite on the PAVDD line.

4. Crystal Requirements

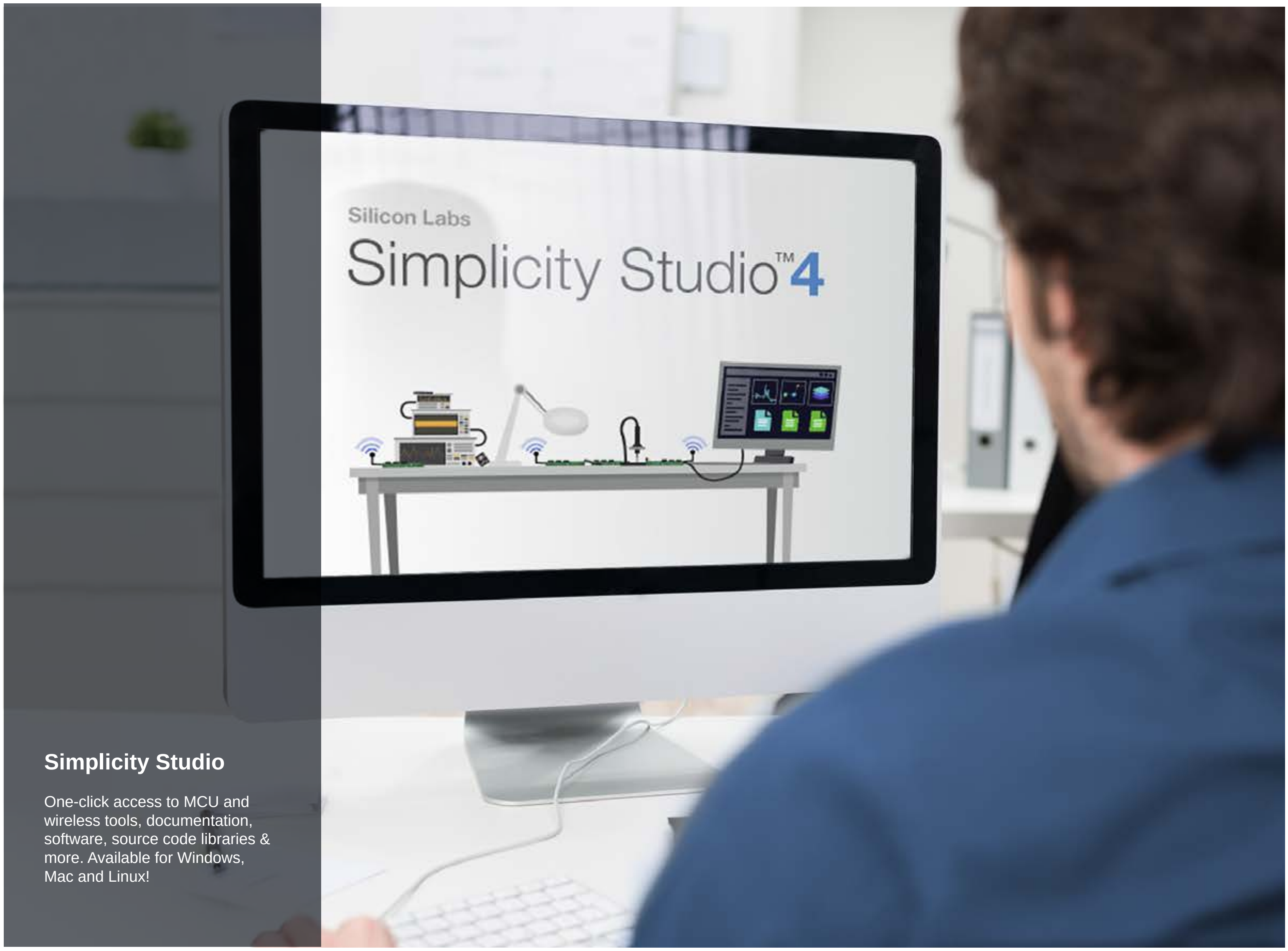
Table 4.1. Crystal Requirements

XTAL type	Crystal Frequency			ESR	Load Capacitance	
	Min	Typ.	Max	Max	Min	Max
LFXO		32.768 kHz		70 kΩ	6 pF	18 pF
HFXO	38 MHz	38.4 MHz	40 MHz	60 Ω	6 pF	12 pF

Note: Many applications do not require the use of an external LFXO. With the EFR32xG13 and EFR32xG14 there is a PLFRCO (32 kHz with 500 ppm accuracy) which replaces the external LFXO component in many use cases. Many applications do not require precise sleep timing and can operate with the LFRCO (32 kHz) or even the ULFRCO (1 kHz), again eliminating the need for an external LFXO.

5. Recommendations for the DC-DC Converter’s External Inductor

- Silicon Labs’ general recommendation on the external inductor (see L1 in 2. Recommended BOM-optimized 2.4 GHz Solution) for the internal dc-dc converter is to use the LQH3NPN4R7MM0L from Murata which has very good performance, is cheap, rugged, and magnetically shielded, but a bit large (3x3 mm).
- For more space-constrained designs, Silicon Labs recommends the NRS2012T4R7MGJ from Taiyo Yuden, which is physically smaller (2x2 mm).
- Some additional candidates: MBKK1608T4R7M, CBMF1608T4R7M.



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