AN933.2: EFR32 Series 2 Minimal BOM

The purpose of this application note is to illustrate bill-of-material (BOM) and cost-optimized solutions for 2.4 GHz applications using the EFR32xG21, EFR32xG22, EFR32xG24, and EFR32xG27/29 Wireless Gecko SoCs.

Silicon Labs reference radio board designs typically use an extensive number of components and multiple layers for RF and VDD filtering to achieve the best possible RF performance at even the highest output power levels. So, the number of PCB layers can be decreased and many of these elements can be eliminated from the design while still maintaining an acceptable RF performance, especially at the lower power levels. This document shows an absolute cost-optimized solution for the EFR32 Series 2 devices targeting high-volume and cost-sensitive applications, mainly applicable for Bluetooth Smart (i.e., BLE) and Zigbee applications at the 2.4 GHz frequency band, where the maximum allowed fundamental RF power is generally lower and the design is typically space-constrained, such as for wearable applications. This application note includes measured data with several different and simplified VDD filtering approaches at the 2.4 GHz frequency region. The RF front-end matching principles are described in more detail in the application note, AN930.2: EFR32 Series 2 2.4GHz Matching Guide. The RF performance also strongly depends on the PCB layout as well as the design of the matching networks. For optimal performance, Silicon Labs also recommends using the PCB layout design guidelines described in the application note, AN928.2: EFR32 Series 2 Layout Design Guide.

KEY POINTS

- BOM, cost, and PCB space-optimized reference design for 2.4 GHz applications
- Eliminates a number of components for RF and V_{DD} domains while maintaining acceptable RF performance
- Measurement results for RX sensitivity, TX performance, and harmonics are provided

1. Device Compatibility

This application note applies to the following EFR32 Series 2 devices:

- EFR32MG21
- EFR32BG22
- EFR32FG22
- EFR32MG22
- EFR32BG24
- EFR32MG24
- EFR32BG27
- EFR32MG27
- EFR32BG29
- EFR32MG29

2. Outline

The following table summarizes the available minimal BOM solutions for EFR32 Series 2 devices.

Table 2.1. Minimal BOM Designs

Part(s)	BOM Reduction*	Max Power	Power Amplifier used	PAVDD Voltage
xG21	7 pcs.	0 dBm	0 dBm PA	3.0 V
	11 pcs.	6 dBm	10 dBm PA	3.0 V
xG22	6 pcs.	6 dBm	0 & 8 dBm PA	1.8 V
xG24	14 pcs.	8 dBm	0 & 10 dBm PA	3.0 V
xG27/29 (QFN)	13 pcs.	8 dBm	0 & 8 dBm PA	1.8 V
xG27/29 (WLCSP)	13 pcs.	4 dBm	0 & 4 dBm PA	1.8 V
*Number of eliminated components compared to the full BOM solution.				

Note: All these designs are only guidelines to show how to reduce the BOM for EFR32 ICs. Main RF parameters were tested on a limited number of devices; full validation and characterization on these minimal BOM solutions were not performed.

3. Minimal BOM Design for EFR32xG21

Silicon Labs developed multiple design options for lowering the manufacturing cost of devices containing the EFRxG21 ICs.

3.1 Design Considerations

This section summarizes the requirements and considerations for the BOM-optimized designs for EFR32xG21 devices.

- For BLE 2.4 GHz applications, EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. EFR32xG21 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements so an external low frequency crystal can be eliminated unless the application requires a higher clock accuracy. See the EFR32MG21 data sheet for reference if LFXO needs to be used in the design.
- The high frequency XTAL is required for operation of EFR32 RF and MCU parts. Load capacitors are not needed. See the EFR32MG21 data sheet for reference.
- The original design contains various supply filtering capacitors to optimize RF performance, but most of these can be eliminated at 0 dBm and 6 dBm TX power and only cause minor degradation in sensitivity and harmonic performance.
- The 0 dBm setup needs a harmonic suppressing capacitor at the RF2G4_IO1 pin.
- An advantage of the 0 dBm setup is lower power consumption by ~ 6mA. See the EFR32MG21 data sheet for reference.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply pin.

3.2 Recommended BOM-optimized 2.4 GHz Solutions

This device does not have a dc-dc converter, so there is a lot less noise on the supply lines compared to designs with one. However, the original radio board contains various supply filtering parts to provide optimal performance at higher power levels. At lower TX powers, like 0 and 6 dBm, most of these can be removed without significantly degrading performance.

The changes made and the measurements are summarized in the following tables and schematic figures.

For the 0 dBm version, all the measurements were taken on the BRD4179B Radio Board (with EFP chip bypassed).

For the 6 dBm version, all the measurements were taken on the BRD4181B Radio Board.

Every part used is 0201 size (deviating from this size will require additional tuning).

Fewer supply filtering components can compromise the receiver's sensitivity, so Table 3.1 Minimal BOM Sensitivity on page 4 shows this value for the BOM-optimized solutions.

Table 3.1. Minimal BOM Sensitivity

Version	Filtering	Sensitivity @2440 MHz (dBm)	
		BLE 1 Mbps, 37 byte payload	802.15.4 Zigbee
6 dBm	Default[1]	-97.4	-104.8
	Min. BOM	-97.5	-104.9
0 dBm	Default[2]	-97.1	-104.2
	Min. BOM	-97.1	-104.3

Note:
1. BRD4181B Radio Board
2. BRD4179B Radio Board (EFP bypassed)

If the default matching is used, fewer filtering components on the RF supply pins can also compromise TX harmonic performance, so Table 3.2 6 dBm Minimum BOM Radiated Harmonics on page 5 and Table 3.3 0 dBm Minimum BOM Radiated Harmonics on page 6 shows radiated TX performance for 6 dBm and 0 dBm Minimal BOM designs.

Table 3.2. 6 dBm Minimum BOM Radiated Harmonics

Frequency (2402 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
		Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Fund	8.9	N/A	8.9	21.1	30
2nd	-47.2	-3.3	-50.5	9.2	-41.2
3rd	-37.8	-5.2	-43.0	13.0	-30.0
4th	-56.2	-6.7	-62.9	32.9	-30.0
5th	-46.1	-6.7	-52.8	11.5	-41.2

Frequency (2440 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
		Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Fund	9.4	N/A	9.4	20.6	30
2nd	-50.0	-3.3	-53.3	12.1	-41.2
3rd	-39.4	-5.2	-44.6	3.4	-41.2
4th	-56.7	-6.7	-63.4	33.4	-30
5th	-49.7	-6.7	-56.4	15.2	-41.2

Frequency (2480 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
		Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Fund	9.6	N/A	9.6	20.4	30
2nd	-51.0	-3.3	-54.3	13.0	-41.2
3rd	-42.8	-5.2	-48.0	6.8	-41.2
4th	-56.6	-6.7	-63.3	33.3	-30.0
5th	-51.8	-6.7	-58.5	17.2	-41.2

Table 3.3. 0 dBm Minimum BOM Radiated Harmonics

Frequency (2402 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
		Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Fund	1.4	N/A	1.4	28.6	30
2nd	-43.7	-3.3	-47.0	5.7	-41.2
3rd	-53.1	-5.2	-58.3	28.3	-30.0
4th	-53.5	-6.7	-60.2	30.2	-30.0
5th	-54.3	-6.7	-61.0	19.7	-41.2

Frequency (2440 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
		Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Fund	1.9	N/A	1.9	28.1	30
2nd	-46.8	-3.3	-50.1	8.9	-41.2
3rd	-53.9	-5.2	-59.1	17.9	-41.2
4th	-54.6	-6.7	-61.3	31.3	-30
5th	-54.3	-6.7	-61.0	19.8	-41.2

Frequency (2480 MHz)	Measured Unmodulated EIRP (dBm)	Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	Limit in EIRP (dBm)
Fund	2.4	N/A	2.4	27.6	30
2nd	-51.0	-3.3	-54.3	13.0	-41.2
3rd	-55.7	-5.2	-60.9	19.6	-41.2
4th	-53.1	-6.7	-59.8	29.8	-30.0
5th	-53.4	-6.7	-60.1	18.8	-41.2

Both configurations above can be valid, and pass FCC/ETSI regulatory margins.

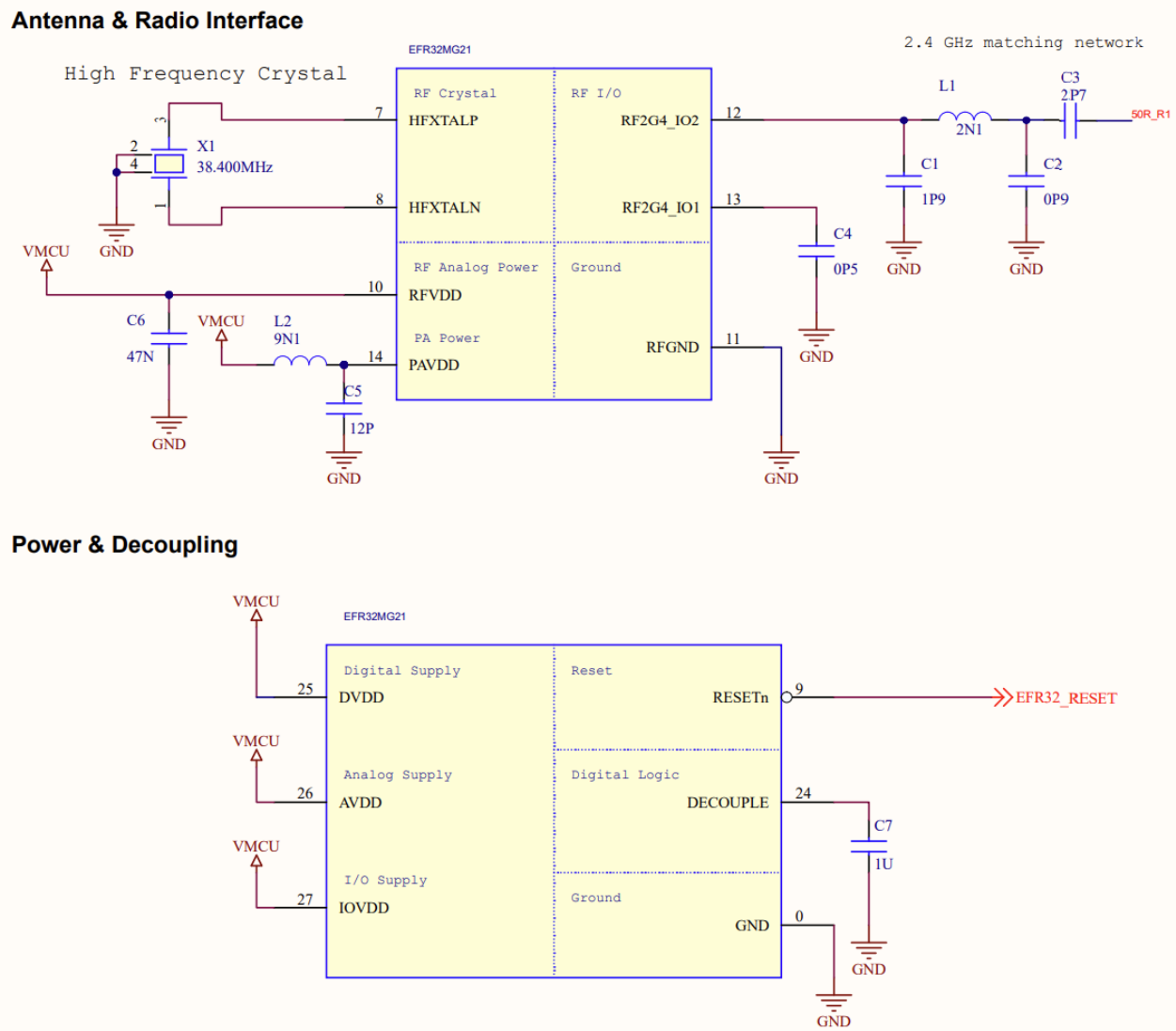


Figure 3.1. Recommended 0 dBm Minimal BOM Schematic for EFR32xG21

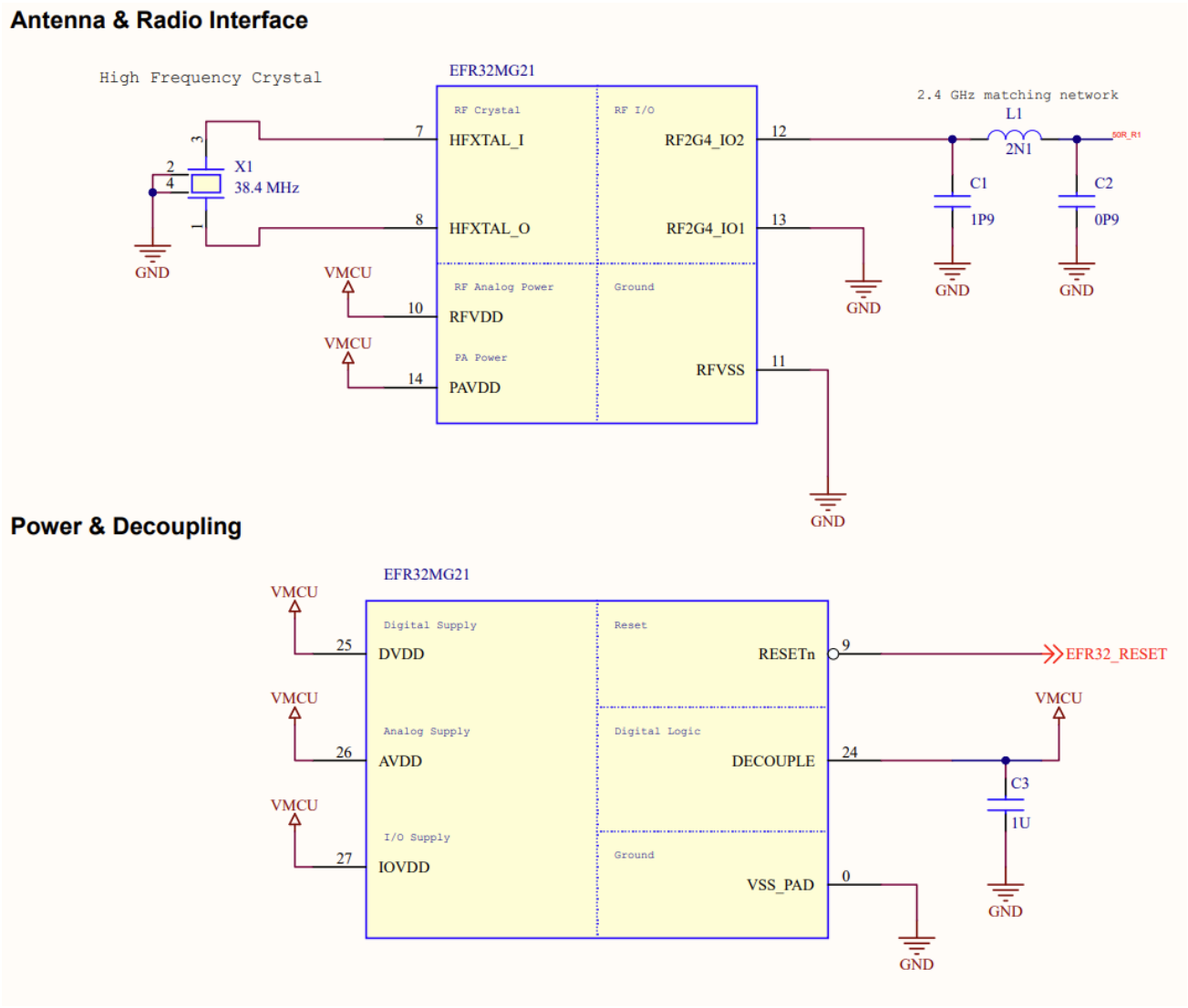


Figure 3.2. Recommended 6 dBm Minimal BOM schematic for EFR32xG21

3.3 Layout Concerns

The results were all measured on a 4-layer board, so the RF matching network component values may not be the same for a 2-Layer board depending on the layout approach used on the RF path. Refer to the application note, AN930.2: EFR32 Series 2 2.4 GHz Matching Guide, for details on the recommended component values depending on the layout approach.

4. Minimal BOM Design for EFR32xG22

Silicon Labs developed a 2-layer design and reduced the official radio board's BOM for lowering the manufacturing cost of devices containing the EFRxG22 ICs.

4.1 Design Considerations

This section summarizes the requirements and considerations for the BOM-optimized designs for EFR32xG22 devices.

- For minimizing costs at the manufacturing level for EFR32xG22 devices, Silicon Labs designed a 2-layer reference design board for customers to use as reference during their design phase. So, as a low-cost solution, the minimal BOM solution presented in this application note is also applicable to the 2-layer EFR32xG22 reference design. For the schematic, layout, BOM and other design files of the low cost reference design, see the design package.
- EFR32 internal dc-dc converter is used for supplying the following VDD rails: DVDD, PAVDD, and RFVDD.
- The on-chip dc-dc converter needs an external inductor and capacitor for proper operation. The inductor used in the 2-layer reference design is CIG10W2R2MNC from Samsung, which is inexpensive and small, but can only be used for low load current. See section 4.4 Recommendations for the DC-DC Converter's External Inductor for other inductor options.
- For EFR32xG22, it is recommended to supply PAVDD, RFVDD, and DVDD from the on-chip dc-dc converter to achieve better current consumption (i.e., better power efficiency) and immunity against the battery voltage level drop and to avoid output power or RF range degradation due to battery aging.
- For BLE 2.4 GHz applications, EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. EFR32xG22 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements so an external low frequency crystal can be eliminated unless the application requires a higher clock accuracy. See section 4.3 Crystal Requirements if LFXO needs to be used in the design.
- The high frequency XTAL is required for operation of RF and MCU parts of the EFR32. Load capacitors are not needed. See section 4.3 Crystal Requirements for the XTAL requirements.
- The RF front-end matching consists of a dc blocking capacitor and a 3-element, C-L-C Pi-network or a L-C-L T-network based on the generic layout concept (detailed in the application note, "AN930.2: EFR32 Series 2 2.4 GHz Matching Guide") to filter the harmonics.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply pin

4.2 Recommended BOM-optimized 2.4 GHz Solutions

The recommended schematics for minimal BOM option for designs using EFR32xG22 wireless MCUs with reduced power supply filtering are shown in the figures below. Note that only the RF matching network is different between both schematics. C5 (120 pF) on PAVDD can be removed in either solution for designs using only the 0 dBm PA.

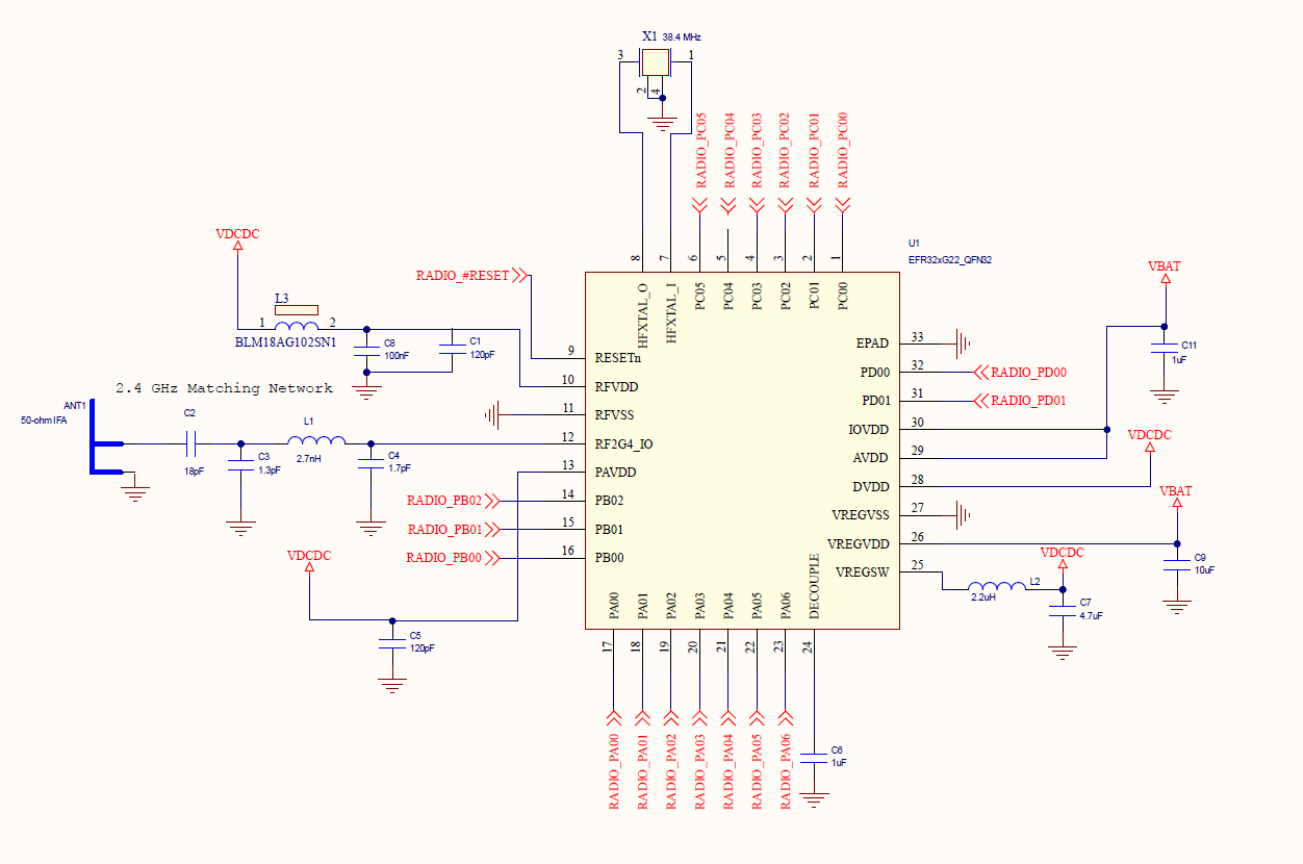


Figure 4.1. Minimal BOM 2.4 GHz Schematic for EFR32xG22 using a 3-element Pi Network

Note: The RF matching network component values may not be the same for a 4-Layer board depending on the layout approach used on the RF path. Refer to application notes, AN930.2 and AN928.2 for details on the recommended component values depending on the layout approach.

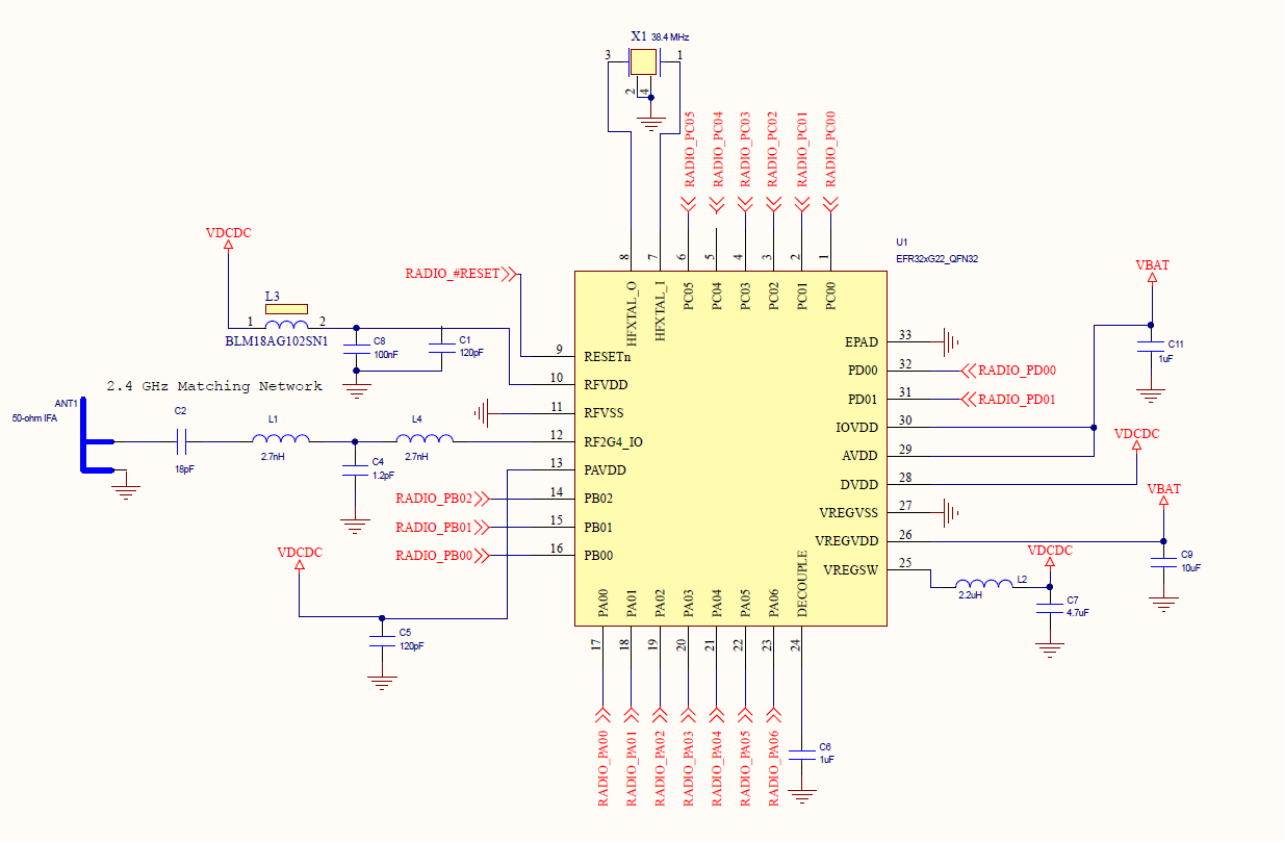


Figure 4.2. Minimal BOM 2.4 GHz Schematic for EFR32xG22 using a 3-element T Network

4.2.1 Measured Performance Data

4.2.1.1 4-Layer EFR32xG22 Reference Design

A full characterization was performed on Silicon Labs' reference radio board BRD4182A Rev. B05 to determine the minimal BOM solution without a significant compromise on the RF performance. For demonstration purposes and summarizing the test results, only a subset of the measurements were chosen to share in this application note. The following measurements performed on BRD4182A are based on the power supply filtering shown in Figure 4.1 on page 10 and Figure 4.2 on page 11.

Table 4.1. Conducted RX Sensitivity

BLE PHY	RFVDD Filtering			RX Sensitivity (dBm)
	Series Ferrite	Parallel Capacitors		
2 Mbps, 37 byte payload[1]	—	120 pF	—	-95.3
	—	120 pF	100 nF	-95.5
	600R ferrite*	120 pF	100 nF	-95.7
1 Mbps, 37 byte payload[1]	600R ferrite*	120 pF	100 nF	-98.5
	—	120 pF	—	-98.7
	—	120 pF	100 nF	-98.7
125 kbps, 255 byte payload[2]	600R ferrite*	120 pF	100 nF	-105.8
	—	120 pF	—	-103.3
	—	120 pF	100 nF	-103.6

Note:
1. 0.1 % Bit Error Rate
2. 0.017% Bit Error Rate

PAVDD, RFVDD, and DVDD are connected to the on-chip dc-dc converter. AVDD, DVDD, IOVDD, and VREGVDD follow the filtering configuration provided in the minimal BOM schematic in Figure 4.1 on page 10 and Figure 4.2 on page 11. There is no filtering on PAVDD.

The conducted RX sensitivity was checked with BLE packets at various data rates (2 Mbps, 1 Mbps, and 125 kbps) and the values are provided here mainly for comparison purposes between the different RFVDD filtering cases. The table above demonstrates that the lack of filtering on RFVDD can cause up to 2 dB of degradation in sensitivity. The best performer of these minimal BOM configurations is marked with an asterisk "*".

Table 4.2. Radiated TX Power and Harmonics

Matching Configuration	PA	BOM Configuration [1]	Capacitor on PAVDD	TX power @ 2440 MHz (dBm)	H2 max (dBm)	H3 max (dBm)	H4 max (dBm)	H5 max (dBm)
Pi Network	6 dBm	Default	N/A	8.7	-55.7	-38.4	< -52.3[2]	-37
	0 dBm	Optimized	No	2.4	-54.3	-49.4	< -51.6[2]	< -48.7[2]
	6 dBm		No	8.2	-55.4	-36.8	< -51.9[2]	-33.3
	6 dBm*		Yes	8.8	-56.1	-37.6	< -51.9[2]	-36.1
T Network	6 dBm			8.6	-52.6	-41.7	-55.3	-40.6

Note:

1. The default BOM configuration refers to the full BOM on the reference design. The optimized BOM refers to the minimal BOM solution from the schematic shown in Figures 3.1 and 3.2, except for PAVDD where the TX measurements are taken with and without a 120 pF capacitor.
2. Under SA noise floor.

Although no filtering is required on PAVDD for acceptable RX sensitivity as shown in Table 4.1 Conducted RX Sensitivity on page 12, it was determined during the measurements with a Pi network that a 120 pF on PAVDD is needed for the radiated TX harmonic levels to achieve similar performance as the default BOM configuration with ~1dB difference. So, this configuration is the best minimal BOM configuration as marked by the asterisk "*".

The harmonic values are the measured maximums of the radiated power in EIRP (dBm) taken in an unmodulated carrier transmission mode so depending on the modulation scheme, the actual radiated power with modulated transmission will be lower. The calculated modulated EIRP of the Pi match and T match using the minimal BOM configuration is provided in the table below, which shows that the critical 3rd and 5th harmonics of the Pi match are indeed compliant with FCC/ETSI limits. The modulation scheme with the lowest correction factor was chosen for the calculations to show the worst case margins. See the BRD4182A reference manual for more details on the measured relaxation factors of the supported modulation schemes to calculate the modulated EIRP from the measured unmodulated EIRP.

Table 4.3. Calculated Modulated EIRP

Matching Configuration	Frequency (2440 MHz)	Measured Unmodulated EIRP (dBm)	BLE 125 Kb/s Coded Modulation			Limit in EIRP (dBm)
			Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Pi Network	Fund	8.8	N/A	8.8	21.2	30
	2nd	-56.1	-2.7	-58.8	17.6	-41.2
	3rd	-37.6	-4.8	-42.4	1.2	-41.2
	4th	< -51.9	-5.5	<-57.4	27.4	-30
	5th	-36.1	-6.3	-42.4	1.2	-41.2
T Network	Fund	8.6	N/A	8.6	21.4	30
	2nd	-52.6	-2.7	-55.3	14.1	-41.2
	3rd	-41.7	-4.8	-46.5	5.3	-41.2
	4th	-55.3	-5.5	-60.8	30.8	-30
	5th	-40.6	-6.3	-46.9	5.7	-41.2

4.2.1.2 2-Layer EFR32xG22 Reference Design

The following conducted and radiated measurements show that the minimal BOM solution determined for BRD4182A is applicable to the low-cost, 2-layer EFR32xG22 reference design as well due to the similar performance with default vs. optimized BOM.

Table 4.4. Conducted TX Power, Harmonics, and RX Sensitivity

Matching Configuration	BOM Configuration	Frequency (MHz)	Power Level (raw)	RX Sensitivity (dBm)	TX Power (dBm)	H2 max (dBm)	H3 max (dBm)	H4 max (dBm)	H5 max (dBm)
Pi Network	Default	2450	52	-97.9	6.2	-68	-35	-56	-42
	Optimized	2450	52	-97.8	6	-65	-36	-56	-43
		2405	114	-97.4	8.2	-57	-32	-54	-37
		2450	114	-97.8	8.1	-60	-33	-53	-35
		2478	114	-96.8	8.05	-61	-33	-53	-35
T network		2450	50	-98	6	-44	-59	-67	-56
		2450	127	-98	8.3	-49.1	-45	-73	-53.6

Note:

1. The BOM-optimized solution provided in Figures 3.1 and 3.2 was used for the measurements.
2. RX Sensitivity test condition: BLE PHY 1 Mbps 2GFSK, 0.1 % BER.
3. The conducted harmonic levels were measured using an unmodulated carrier tone.

As shown in the table above, the 2-layer board with minimal BOM configuration using a T match can transmit up to 8 dBm with acceptable conducted harmonic performance. However, the radiated 3rd and 5th harmonic performance in this configuration has not been verified, so the recommended minimal BOM solutions can only be applied to power levels up to 6 dBm.

Table 4.5. 2-layer Radiated TX Power and Harmonics

Matching Configuration	BOM Configuration	Frequency (MHz)	TX Power @ 2440 MHz (dBm)	H2 max (dBm)	H3 max (dBm)	H4 max (dBm)	H5 max (dBm)
Pi Network	Default	2449	5.38	-48.44	-37.91	-50.93	-43.92
	Optimized	2449	5.8	-50.18	-37.45	-50.9	-42.31
T Network		2450	7.1	-46.1	-43.6	-62.7	-38.1

The data shows that the radiated performance is within ~1 dB difference between the optimized and the default BOM, so the optimized BOM solution provided in Figure 4.1 Minimal BOM 2.4 GHz Schematic for EFR32xG22 using a 3-element Pi Network on page 10 can be used on 2-layer EFR32xG22 designs.

The harmonic values are the measured maximums of the radiated power in EIRP (dBm) taken in an unmodulated carrier transmission mode, so the true evaluation of the radiated harmonics compliance and its margins with ETSI/FCC limits is done in Table 4.6 Calculated Modulated EIRP on page 15, which shows that the critical 3rd harmonic using a Pi network and 5th harmonic using T network actually pass the regulatory limits with 1.05 dB and 3.2 dB margins respectively.

Table 4.6. Calculated Modulated EIRP

Matching Configuration	Frequency (2440 MHz)	Measured Unmodulated EIRP (dBm)	BLE 125 Kb/s Coded Modulation			Limit in EIRP (dBm)
			Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
Pi Network	Fund	5.8	N/A	5.8	24.2	30
	2nd	-50.18	-2.7	-52.88	11.68	-41.2
	3rd	-37.45	-4.8	-42.25	1.05	-41.2
	4th	-50.9	-5.5	-56.4	26.4	-30
	5th	-42.31	-6.3	-48.61	7.41	-41.2
T Network	Fund	7.1	N/A	7.1	22.9	30
	2nd	-46.1	-2.7	-48.8	7.6	-41.2
	3rd	-43.6	-4.8	-48.4	7.2	-41.2
	4th	-62.7	-5.5	-68.2	38.2	-30
	5th	-38.1	-6.3	-44.4	3.2	-41.2

4.2.2 Additional Concerns

This section lists some additional concerns regarding the RF performance versus different BOM options, and provides some further suggestions on the space constraint layout designs.

- If the on-chip dc-dc converter is not used, the following components can be eliminated from the schematics shown in Figures 3.1 and 3.2: L2 and C7. However, the trade-off would be an increase in current consumption. Refer to Section 4.6 of EFR32xG22's data sheet for more details on the current consumption values in different EM modes.
- Because the AVDD and IOVDD pads are beside each other, a single 1 uF capacitor can be used for both VDD supplies; however, they must be tied together.
- Even in space-constrained designs, it is strongly recommended to place the L2 and C7 components (at the on-chip dc-dc converter output) as close to the EFR32xG22 wireless MCU's VREGSW pin as possible. Also, the L2 dc-dc inductor should be placed far away from any noise-sensitive circuitry (ex: radio antenna).
- The high frequency crystal also needs to be placed close to the EFR32xG22 wireless MCU.
- A 100 nF capacitor on the RESET line is needed to filter noise if the trace is long and routed to a push button on a different board. Otherwise, it can be eliminated.
- The critical harmonics, such as the 3rd and 5th harmonic, are sensitive to the routing of the RF path from the chip to the antenna, so it is strongly recommended to follow the layout approach provided in AN928.2: EFR32 Series 2 Layout Design Guide for achieving optimal RF performance.

4.3 Crystal Requirements

Table 4.7. Crystal Requirements

XTAL Type	Crystal Frequency	Gain	ESR		Load Capacitance		
			Typ	Max	Min	Typ	Max
LFXO	32.768 kHz	0	—	80 kΩ[1]	4	—	6
		1	—	100 kΩ	6	—	10
		2	—		10	—	12.5
		3	—		12.5	—	18
HFXO	38.4 MHz	—	40 Ω	—	—	10 pF	—

Note:

1. Many applications do not require the use of an external LFXO. With the EFR32xG22, there is a LFRCO with precision mode (32 kHz with 500 ppm accuracy), which can replace the external LFXO component in many use cases. Many applications do not require precise sleep timing and can operate with the LFRCO (32 kHz) or even the ULFRCO (1 kHz), again eliminating the need for an external LFXO.

4.4 Recommendations for the DC-DC Converter's External Inductor

- Silicon Labs' general recommendation on the external inductor for the internal dc-dc converter is to use the CIG22H2R2MNE from Samsung which has very good performance and is inexpensive, but a bit large (2.5 x 2 mm) compared to CIG10W2R2MNC (1.6 x 0.8 mm).
- Some additional candidates: LQM2HPN2R2MG0L, CIG22L2R2MNE

5. Minimal BOM Design for EFR32xG24

Silicon Labs has developed multiple design options for lowering the manufacturing cost of devices containing the EFRxG24 ICs.

5.1 QFN40 and QFN48 Package

5.1.1 Design Considerations

This section summarizes the requirements and considerations for BOM-optimized designs using EFR32xG24 devices with QFN40 and QFN48 package.

- EFR32 internal dc-dc converter is used for supplying the following VDD rails: DVDD, PAVDD, and RFVDD in filtering option 2, 3, and 4. In option 1, no such converter is used, thus it has a higher current consumption, in both RX and TX mode, by approximately 3 mA (MCU in sleep mode).
- The on-chip dc-dc converter needs an external inductor and capacitor for proper operation. The inductor used is the same as in the BRD4186C Reference Design.
- For BLE 2.4 GHz applications, EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. EFR32xG24 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements so an external low frequency crystal can be eliminated unless the application requires a higher clock accuracy. See the EFR32MG24 Data Sheet for reference if LFXO needs to be used in the design.
- The high frequency XTAL is required for operation of RF and MCU parts of the EFR32. Load capacitors are not needed. See the EFR32MG24 Data Sheet for reference.
- The original design contains various supply filtering capacitors to optimize RF performance, but most of these can be eliminated at 0 dBm TX power, and only cause minor degradation in sensitivity and harmonic performance.
- The 4-element Pi-match can be reduced to only one element at 0 dBm power without breaking the FCC regulatory margins.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply pin

5.1.2 Recommended BOM-Optimized 2.4 GHz Solutions

The original radio board contains various supply filtering parts and a 4-element Pi-matching network. Both of these can be reduced to lower manufacturing costs.

The changes made and the measurements are summarized in the following tables and schematic figures.

Every measurement was taken on the BRD4186C Radio Board (with indicated minor modifications if it was necessary), and **every part used is 0201 size** (deviating from this size will require additional tuning).C_AVDD (1 uF), C_DEC (1 uF) and CC1 (18 pF) capacitors are necessary and present in ALL options.

Fewer supply filtering components can mainly compromise the receiver's sensitivity. Table 5.1 on page 18 below shows this value for every reduction option.

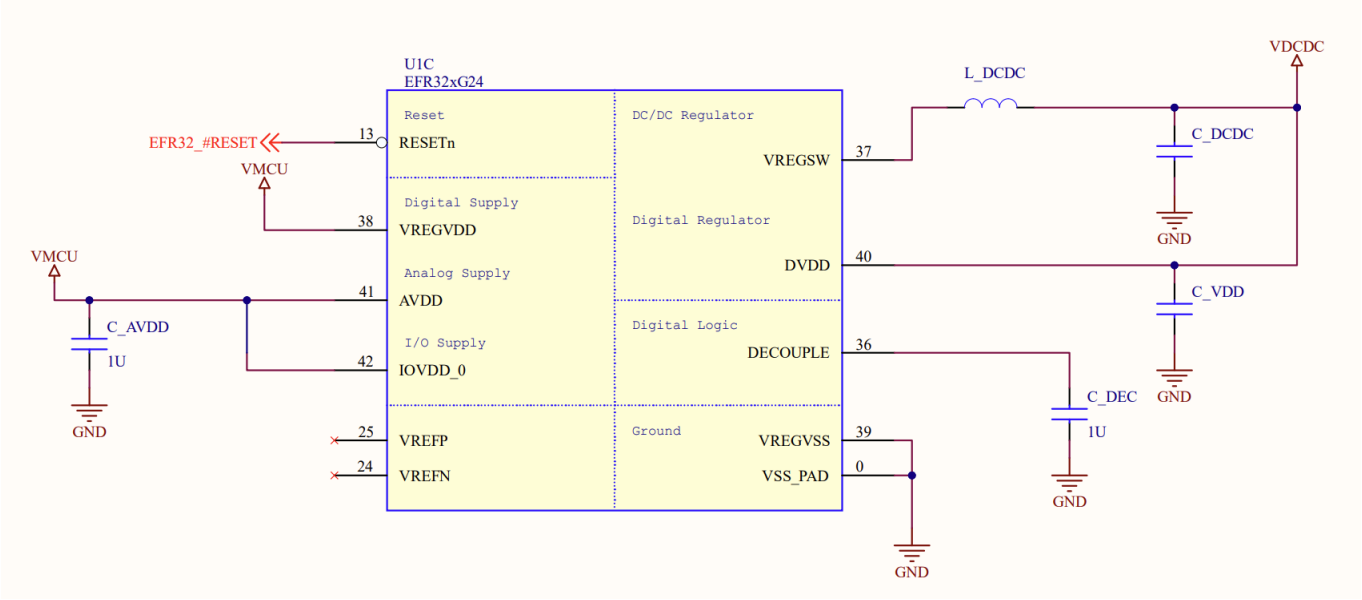


Figure 5.1. Power Supply Filtering Schematic

Table 5.1. Power Supply Filtering Reduction Options

Filtering options	Sensitivity @2440 MHz [dBm] [1]		Filtering Parts					
	BLE 1 Mbps, 37 byte payload	802.15.4 Zigbee	DCDC			RFVDD		PAVDD
			C_VDD	L_DCDC	C_DCDC	C_RFVDD	L_RFVDD[2]	C_PAVDD
Option 1[3]	-97.7	-105.5	—	—	—	—	v	—
Option 2	-97.1	-105	—	2.2 µH	4.7 µF	—	Ferrite	—
Option 3	-97.1	-105.1	10 µF	2.2 µH	4.7 µF	—	Ferrite	—
Option 4	-97.7	-105.7	10 µF	2.2 µH	4.7 µF	2.2 µF	Ferrite	120 pF
Default	-97.7	-105.6	Original BRD4186C values					

Note:

1. Default matching used.
2. Ferrite bead (BLM03AG700SN1)
3. DCDC converter not used, V_DCDC and VMCU shorted, this results in ~3 mA extra consumption in both RX and TX (0 dBm).

Fewer matching components can compromise mostly the transmitter's performance and also RX sensitivity, so Table 5.4 on page 20 and Table 5.5 on page 20 show TX power and harmonic performance and Table 5.3 on page 20 contains sensitivity values. These were all measured using the **Option 2** filtering configuration, which is the recommended one, because of its minimal compromise in RX and TX performance.

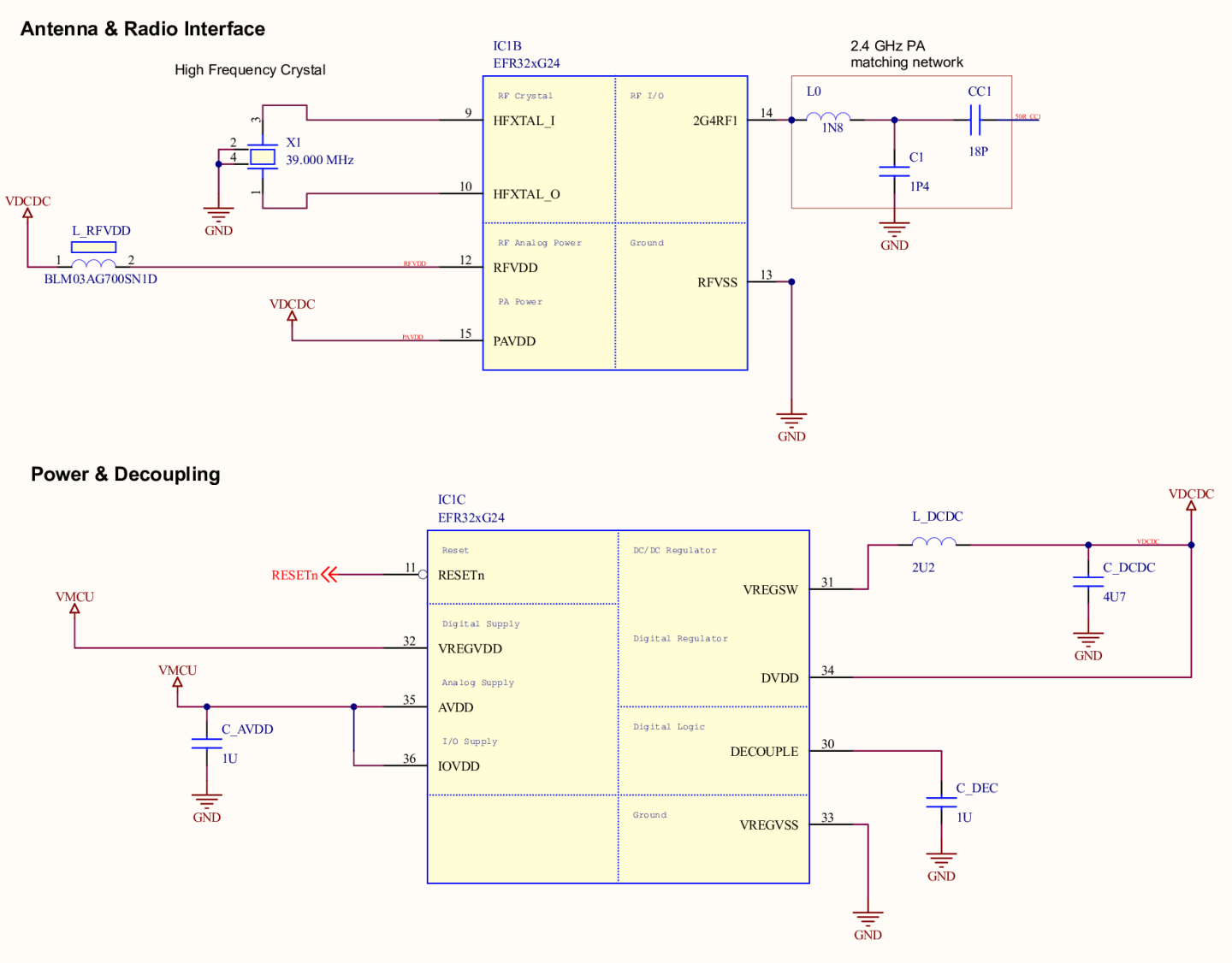


Figure 5.2. RF Components Schematic

Table 5.2. Matching Reduction Options

Matching	Values				
	Capacitors		Inductors		
	C1	C2	L0	L1	L2
Default	2.3 pF	1.6 pF	—	2.5 nH	1.7 nH
2-element	1.6 pF	—	1.3 nH	—	—
1-element	1.5 pF	—	—	—	—
Note: If a part is not used, the footprint should be removed/shorted.					

Table 5.3. Matching Options RX Sensitivity

Matching	Sensitivity @2440 MHz (dBm)	
	BLE 1 Mbps, 37 byte payload	802.15.4 Zigbee
Default	-97.1	-105
2-element	-97.7	-105.6
1-element	-97.9	-105.6

Note: Measured with Option 2 filtering.

Table 5.4. Conducted 0 dBm TX Performance

Matching[1]	Max. TX Output Power (0 dBm PA) (dBm)	Conducted TX Harmonics @f0=2450 MHz, max power (dBm)				I_TX[2] (mA)
		2nd	3rd	4th	5th	
Default	-1.0	-64.7	-82.3	-96.1	-98.0	4.7
2-element	-0.5	-45.4	-76.2	-83.8	-92.1	4.7
1-element	-0.4	-43.8	-65.4	-82.4	-94.7	4.6

Note:

1. Paired with Option 2 filtering.
2. @ VDD = 3.0 V, f = 2.45 GHz, CW, 0 dBm PA, max power, MCU in sleep mode.

Table 5.5. Radiated Performance at 3 Power Levels

Configuration	Frequency (2450 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
			Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
2- element Network, 0 dBm TX power[1]	Fund	2.9	N/A	2.9	27.1	30
	2nd	-55.3	-3.3	-58.6	17.4	-41.2
	3rd	-56.1	-5.2	-61.3	20.1	-41.2
	4th	-58.2	-6.7	-64.9	34.9	-30
	5th	-54.7	-6.7	-61.4	20.2	-41.2
1- element Network, 0 dBm TX power[1]	Fund	1.8	N/A	1.8	28.2	30
	2nd	-52.5	-3.3	-55.8	14.6	-41.2
	3rd	-55.8	-5.2	-61.0	19.8	-41.2
	4th	-58.1	-6.7	-64.8	34.8	-30
	5th	-55.5	-6.7	-62.2	21.0	-41.2

Configuration	Frequency (2450 MHz)	Measured Unmodulated EIRP (dBm)	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
			Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
2- element Network, 4 dBm TX power[2]	Fund	7.6	N/A	7.6	22.4	30
	2nd	-47.9	-3.3	-51.2	10.0	-41.2
	3rd	-54.3	-5.2	-59.5	18.3	-41.2
	4th	-57.7	-6.7	-64.4	34.4	-30
	5th	-54.9	-6.7	-61.6	20.4	-41.2
2- element Network, 8 dBm TX power[3]	Fund	12.7	N/A	12.7	17.3	30
	2nd	-43.6	-3.3	-46.9	5.7	-41.2
	3rd	-40.0	-5.2	-45.2	4.0	-41.2
	4th	-54.6	-6.7	-61.3	31.3	-30
	5th	-48.8	-6.7	-55.5	14.3	-41.2

Note:

1. 0 dBm PA max power.
2. 10 dBm PA, Raw power setting: 16.
3. 10 dBm PA, Raw power setting: 46.

All the configurations above can be valid, and pass FCC regulatory margins. Although, all the power supply filtering and matching variations are capable solutions, the recommended one is **Option 2 with the 2-element matching network** (Figure 5.3 on page 22), because it provides the smallest compromise between RF performance and cost. Also, it does not require additional tuning like its 1-element counterpart.

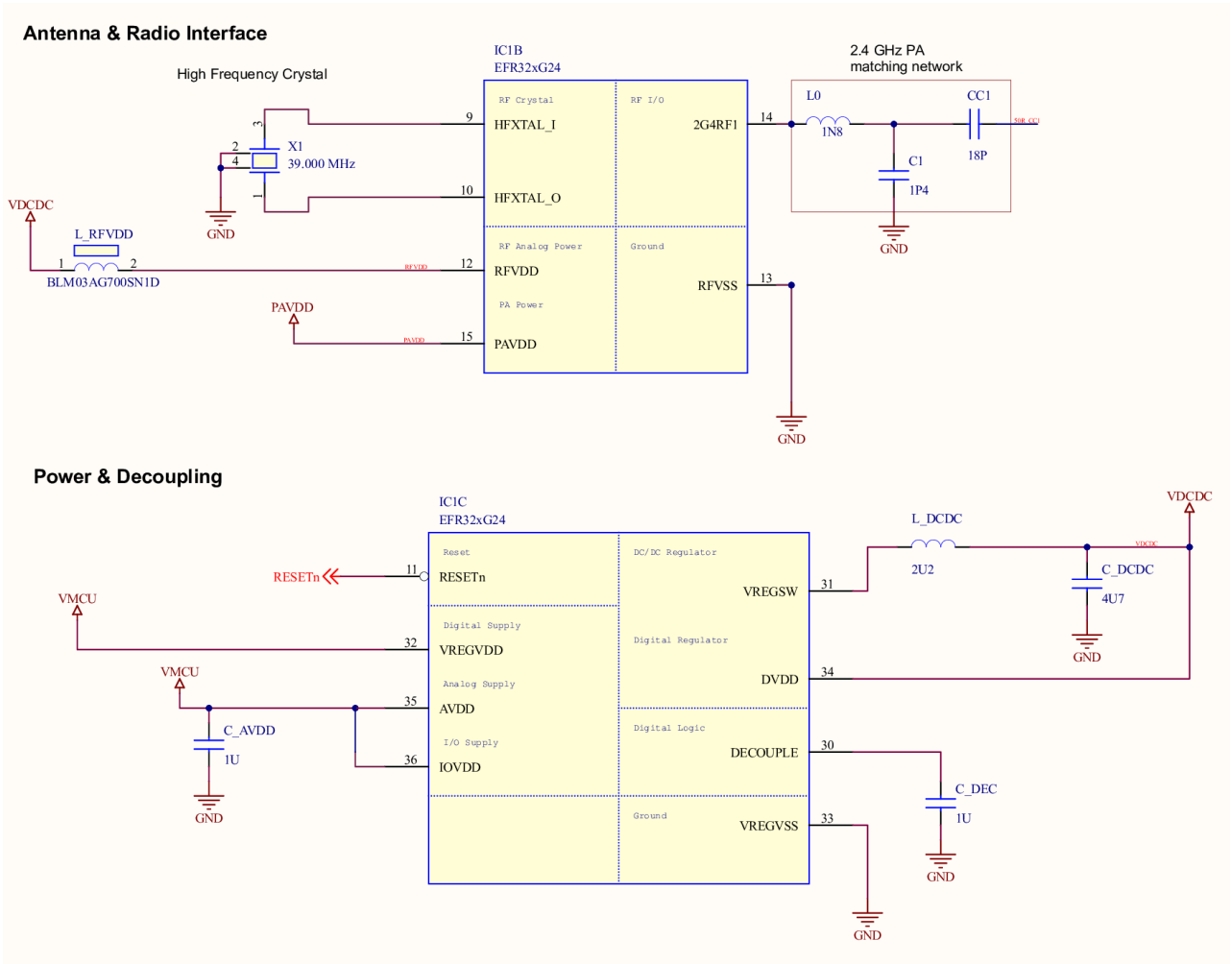


Figure 5.3. Recommended Minimal BOM Schematic for EFR32xG24

5.1.3 Layout Concerns

All the layouts mentioned were using the guidelines laid in application note, AN928.2: EFR32 Series 2 Layout Design Guide.

The 1-element and 2-element matching options require some minor modifications in the matching layout.

In the default reference design there is no footprint for L0, so a modified layout for the 2-element matching can be seen in the figure below.

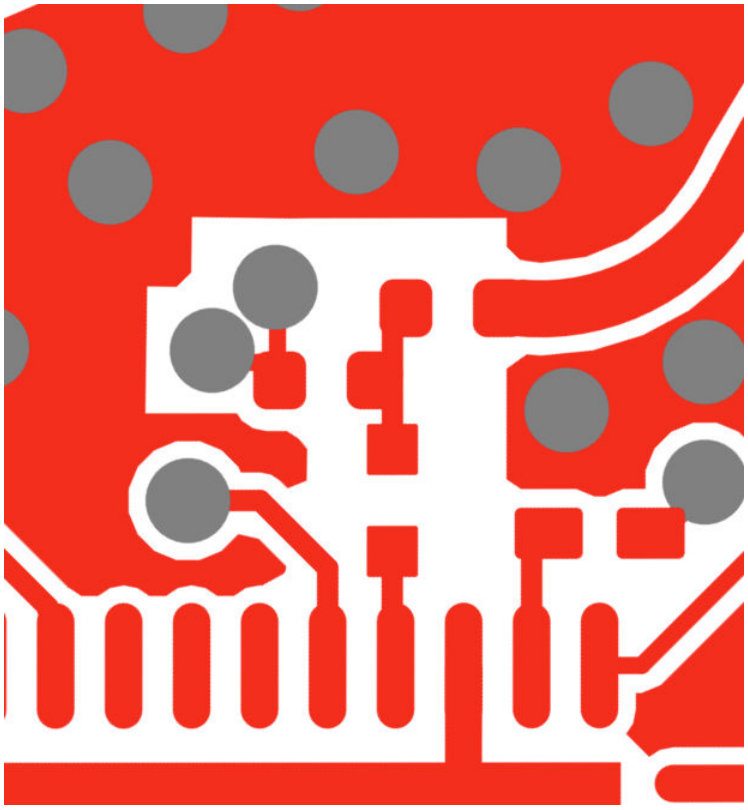


Figure 5.4. Layout for the 2-Element Matching

For the 1-element matching a distributed element is used. This element's impedance is sensitive to all the PCB parameters (dielectric constant, stackup etc.), trace width, clearance and length, so additional tuning may be required.

This can be done most conveniently by changing the distance between the RF2G4_IO pin and C1. The distance on the reference layout, used in the measurements above, is 3 mm, so it is recommended as a starting value. Trace clearance and width, as well as PCB stackup, should be the same as the BRD4186C Reference Design, to minimize the need for tuning.

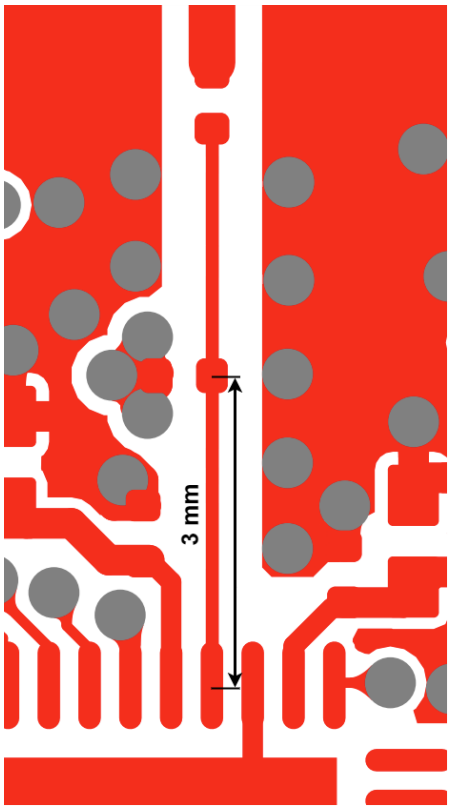


Figure 5.5. Layout for the 1-Element Matching

For detailed instructions on layout design guidelines, refer to application note, AN928.2: EFR32 Series 2 Layout Design Guide.

Note: The results were all measured on a 4-layer board, so the RF matching network component values may not be the same for a 2-Layer board depending on the layout approach used on the RF path. Refer to application note, AN930.2: EFR32 Series 2 2.4 GHz Matching Guide for details on the recommended component values depending on the layout approach.

5.2 WLCSP42 Package

5.2.1 Design Considerations

This section summarizes the requirements and considerations for BOM-optimized designs based on EFR32xG24 devices with WLCSP42 package.

- For optimum power efficiency, the internal dc-dc converter is used for supplying the following VDD rails: DVDD, PAVDD, and RFVDD
- The on-chip dc-dc converter needs an external inductor and capacitor for proper operation. The inductor used is DFE2HCAH2R2MJ0L from Murata, which is the same as in the BRD4115B radio board reference design. See AN0948.2: EFM32 and EFR32 Series 2 DC-to-DC Converter for additional details as well as guidelines on selecting alternative components.
- For BLE 2.4 GHz applications, the EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. The EFR32xG24 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements, so an external, low-frequency crystal can be eliminated unless the application requires a higher clock accuracy and/or lower sleep current. See the EFR32BG24 Data Sheet for reference if LFXO needs to be used in the design.
- The high frequency XTAL is required for operation of RF and MCU parts of the EFR32. Load capacitors are not needed. See the EFR32BG24 Data Sheet for reference.
- The original design contains various supply filtering capacitors to optimize RF performance, however, most of these can be eliminated while causing only minor degradation in sensitivity and harmonic performance.
- The RF matching and filtering network used is the reference matching that is also used in the BRD4115B Reference Design. It consists of a 3-element L-C-L T-network and a dc-blocking capacitor. The same matching network can be used for the low-power (0 dBm) and the high-power (+4 dBm) PA.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply

5.2.2 Recommended BOM-optimized 2.4 GHz Solution

The schematics for the recommended EFR32xG24 WLCSP minimum BOM solution are shown in the figures below. Note that only the power supply filtering and decoupling networks were reduced compared to the default reference design. The 3-element RF matching network (consisting of L1, C2, and L2) is identical to the default matching. The series dc blocking capacitor (CC1) is required when the 0 dBm PA is utilized. A 3-element pi-network placeholder (consisting of C4, L3, and C5) is included for antenna impedance tuning purposes. If the antenna impedance is guaranteed to be 50 Ω or its impedance can be tuned by other means, then the antenna tuning placeholder can be omitted.

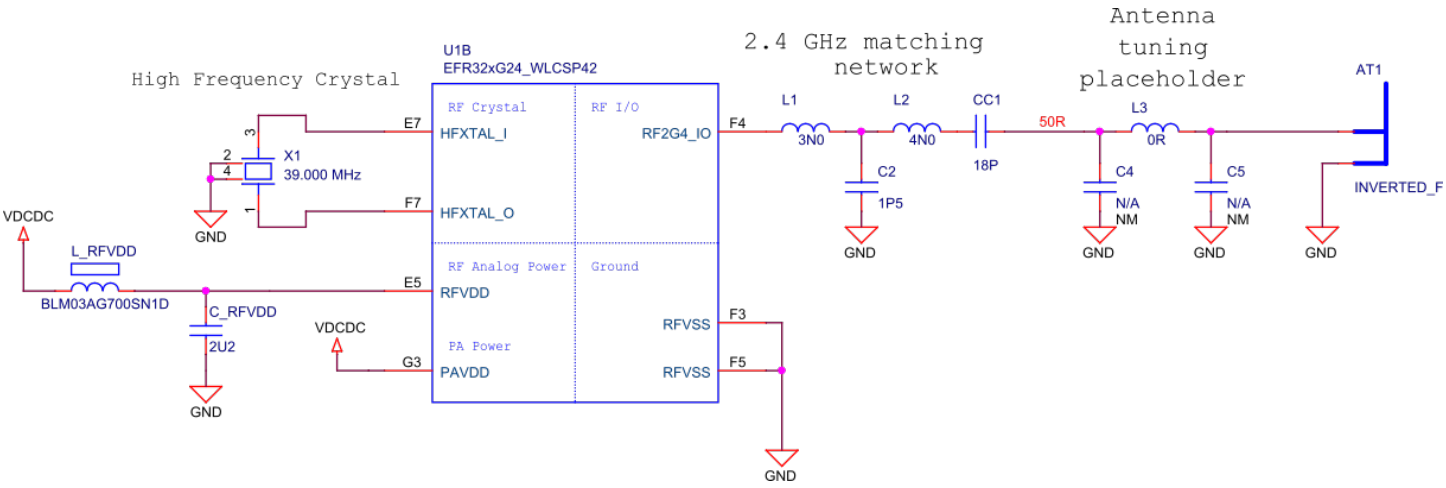
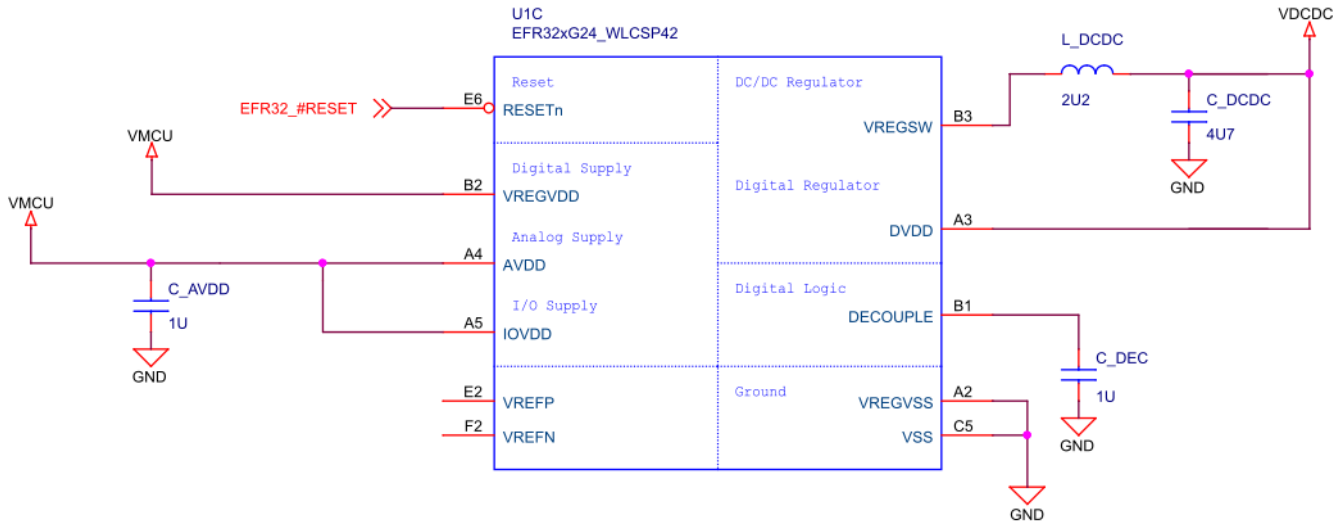


Figure 5.6. Recommended Minimum BOM for EFR32xG24 WLCSP (Radio)

Note: The design uses SMD 0201 components. Without additional tuning, the usage of different size components (especially in the RF matching network) may result in degraded RF performance and/or elevated harmonic emissions. For additional guidelines on the matching network, refer to AN930.2: EFR32 Series 2 2.4 GHz Matching Guide.

Figure 5.7. Recommended Minimum BOM for EFR32xG24 WLCSP (Power & Decoupling)



The requirements and design guidelines on the layout are documented in AN928.2: EFR32 Series 2 Layout Design Guide.

Characterization was performed on a BRD4115B radio board. The RF performance was tested with both the Default “Full” BOM and the Minimum BOM.

As per the test results, compared to the Default “Full” BOM:

- The RX sensitivity is degraded by ~0.3 dB
- The TX power is ~0.2 dB higher when the LP (0 dBm) PA is used while ~0.3 dB lower when the HP (+4 dBm) PA is used.

The measured radiated harmonic levels indicate >10 dB margin to the applicable FCC and ETSI limits.

The test conditions and the detailed results are summarized in the tables below:

Table 5.6. EFR32xG24 WLCSP TX Performance

PA	Power Setting (raw)	BOM Configuration	TX Power [dBm]	TX Current[1] [mA]	Conducted TX Harmonics[2] [dBm]			
					2nd	3rd	4th	5th
0 dBm	15	Default	0.5	4.8	-52.1	-78.6	-92.9	-95.0
		Minimum BOM	0.7	4.9	-52.5	-75.3	-93.9	-96.9
+4 dBm	17	Default	4.4	11	-47.0	-76.5	-90.6	-81.5
		Minimum BOM	4.1	10.8	-47.7	-80.0	-89.3	-82.9

Notes:
1. Total system current consumption measured at VMCU = 3.0 V, MCU in EM1, VSCALE1, f = 2450 MHz, CW signal.
2. Max. across band. Signal is unmodulated carrier (CW).

Table 5.7. EFR32xG24 WLCSP RX Sensitivity

Config	Sensitivity [dBm]							
	BLE 1 Mbps[1]		BLE 125 Kbps[1]		BLE 2 Mbps[1]		802.15.4[2]	
	Avg.[2]	Max.[2]	Avg.[2]	Max.[2]	Avg.[2]	Max.[2]	Avg.[23]	Max.[2]
Default	-98.0	-97.8	-106.1	-106.0	-95.3	-95.2	-105.9	-105.7
Minimum BOM	-97.7	-97.5	-105.8	-105.7	-95.0	-94.7	-105.7	-105.6

Notes:
1. BER≤0.1%, Signal is reference signal, 37 byte payload.
2. PER≤1%, Signal is reference signal, packet length is 20 octets.
3. Across all channels.

Table 5.8. EFR32xG24 WLCSP Radiated Harmonics[1]

PA	Power Setting (raw)	Harmonic No.	Measured Un-modulated EIRP [dBm]	BLE 125 Kb/s Coded Modulation			Limit in EIRP [dBm]
				Correction Factor [dB][2]	Calculated Modulated EIRP [dBm]	Modulated Margin [dB]	
LP (0 dBm)	15	Fund.	2.5	N/A (0 is used)	2.5	27.5	30
		2nd	-55.8	-2.7	-58.5	17.3	-41.2
		3rd	-46.9	-4.8	-51.7	10.5	-41.2
		5th	-53.5	-6.3	-59.8	18.6	-41.2
HP (+4 dBm)	17	Fund.	6.2	N/A (0 is used)	6.2	23.8	30
		2nd	-56.4	-2.7	-59.1	17.9	-41.2
		3rd	-56.1	-4.8	-60.9	19.7	-41.2
		4th	-58.1	-5.5	-63.6	33.6	-30
		5th	-54.5	-6.3	-60.8	19.6	-41.2

Notes:

1. Using the on-board printed Inverter-F (IFA) antenna.
2. Fundamental powers are the average of the tested frequencies (2402 MHz, 2450 MHz, 2480 MHz) powers while harmonic powers are worst case across test planes and frequencies (2402 MHz, 2450 MHz, 2480 MHz).

Note: All the listed tests were performed with a 4-layer board. The optimum RF matching network components and/or the RF performance may not be the same with 2-layer boards.

6. Minimal BOM Design for EFR32xG27/29

Silicon Labs has reduced the official radio board's BOM to lower the manufacturing cost of devices containing the EFR32xG27/29 ICs.

6.1 QFN40 Package with Internal Buck-Converter

6.1.1 Design Considerations

This section summarizes the requirements and considerations for the BOM-optimized designs for EFR32xG27/29 QFN devices with an internal buck dc-dc converter.

- The on-chip dc-dc converter needs an external inductor and capacitor for proper operation. The inductor used is the same as in the BRD4194A Reference Design.
- For EFR32xG27/29, it is recommended to supply PAVDD, RFVDD, and DVDD from the on-chip dc-dc converter to achieve better current consumption (i.e., better power efficiency) and immunity against the battery voltage level drop and to avoid output power or RF range degradation due to battery aging.
- For BLE 2.4 GHz applications, EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. EFR32xG27/29 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements, so an external low frequency crystal can be eliminated unless the application requires a higher clock accuracy. See section 4.3 Crystal Requirements if LFXO needs to be used in the design.
- The high frequency XTAL is required for operation of RF and MCU parts of the EFR32. Load capacitors are not needed. See section 4.3 Crystal Requirements for the XTAL requirements.
- The RF front-end matching consists of a dc blocking capacitor and a 2-element LC matching network to filter the harmonics. The same matching network can be used for the 0 dBm and the 8 dBm PA.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply pin

6.1.2 Recommended BOM-Optimized 2.4 GHz Solution

The original radio board contains various supply filtering parts and a 3-element T-matching network. Both of these can be reduced to lower manufacturing costs.

The changes made and the measurements are summarized in the following tables and schematic figures.

Every measurement was taken on the BRD4194 Radio Board (with indicated minor modifications if it was necessary), and every part used is 0201 size (deviating from this size will require additional tuning).

A single minimum BOM design is proposed that can be used with both the 0 dBm and the 8 dBm PA with acceptable margins on the FCC radiated harmonic limits. TX power and harmonics and RX sensitivity did not degrade by the VDD filtering BOM reduction. Performance degradation was only attributed to the matching network BOM reduction.

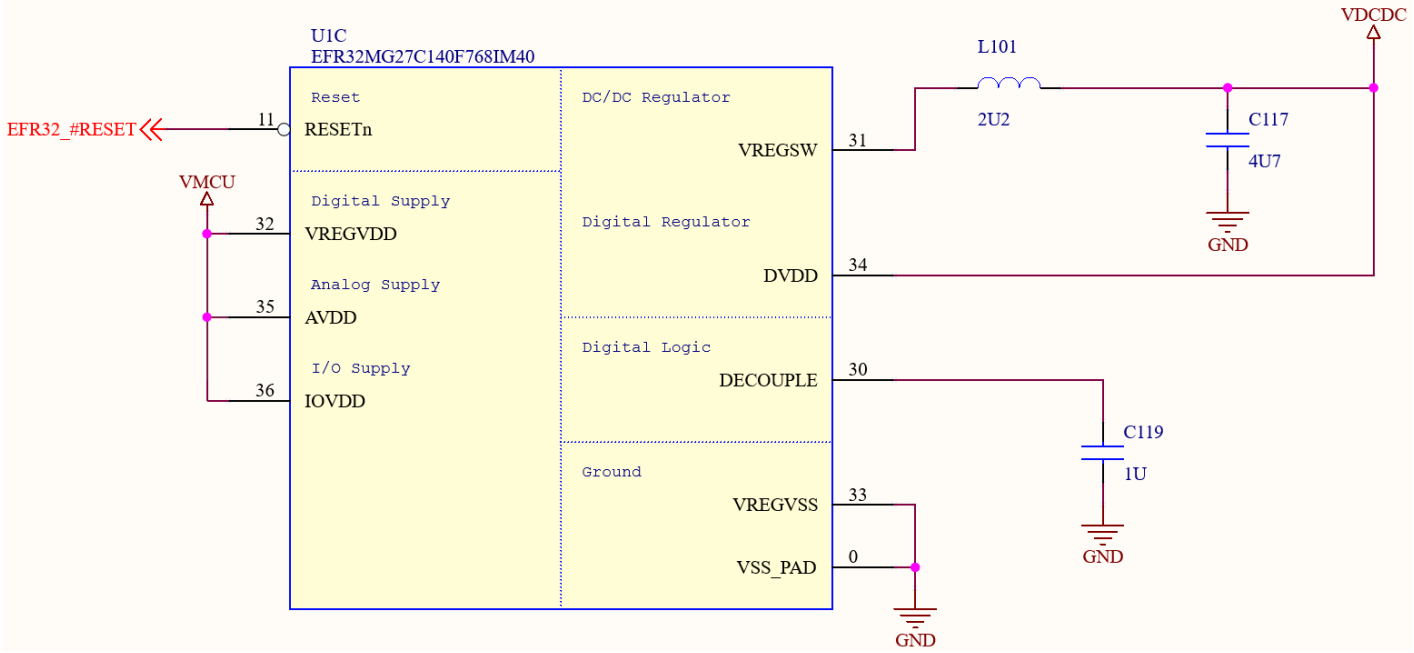


Figure 6.1. Power Supply Filtering Schematic

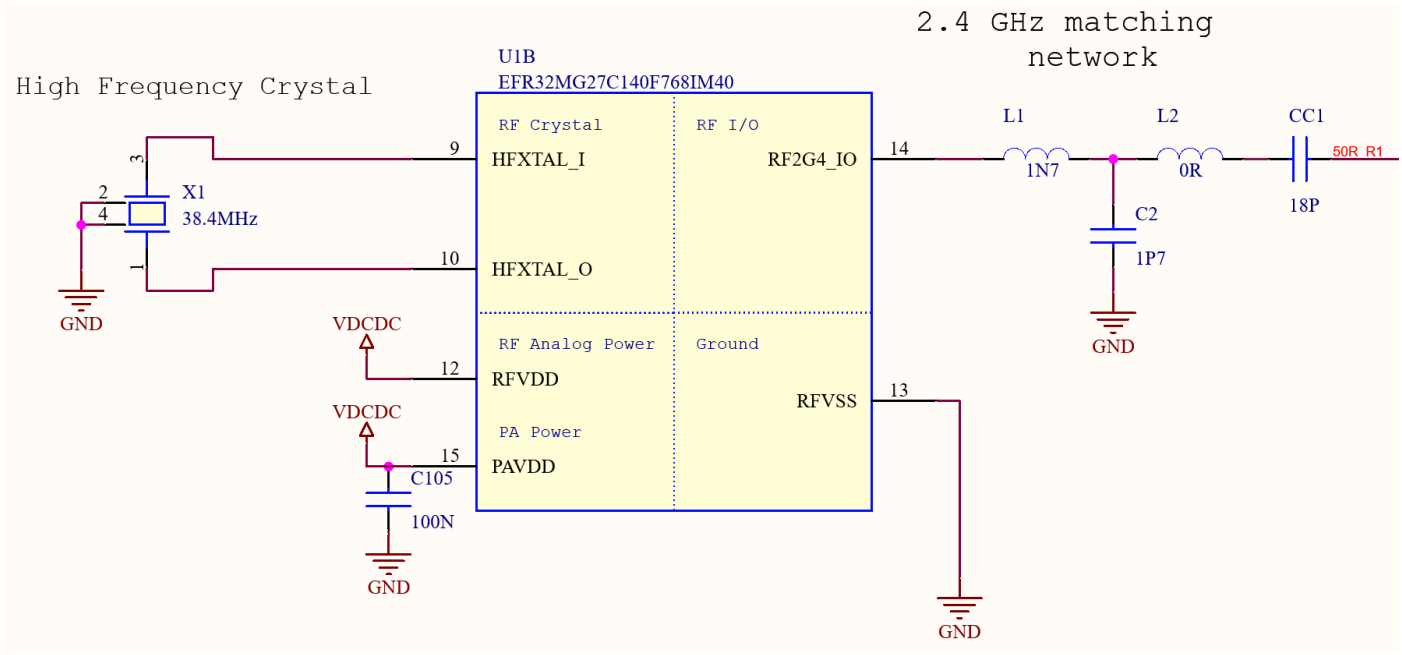


Figure 6.2. RF Components Schematic

The tables below show the results of the RF measurements.

Table 6.1. Conducted RX Performance

BOM	Sensitivity (dBm)[3]		Values					
			Matching Network			VDD Filtering Network		
	BLE1 Mbps, 37 byte payload	802.15.4 Zigbee	L1	C2	L2	L_DCDC	C_DCDC	C_PAVDD
Minimum	-98.4	-101.4	1.7 nH	1.7 pF	0 Ω[1]	2.2 uH	4.7 uF	100 nF[2]
Default	-99.2	-102.2	2 nH	1.6 pF	3.2 nH	Original BRD4194A BOM (16 components in total)		

Note:

1. L2 was shorted with a 0 Ω resistor. The footprint can be removed from the design.
2. C_PAVDD = 100 nF is responsible for filtering the HFXO spurs around the carrier.
3. The frequency for this table was selected in the 2.4 GHz band where the sensitivity degradation was the largest (0.8 dB). The degradation was seen at the 2430-2450 MHz channels, while on the rest of the channels it was close to the data sheet value.
4. CC1 = 18 pF is a dc-blocking capacitor that is necessary when using the 0 dBm PA.

Table 6.2. Conducted TX Performance

Matching	Power Setting (raw)[1]	Max. TX Output Power (dBm)	ConductedTX Harmonics @2450 MHz (dBm)				I_TX[2]
			2nd	3rd	4th	5th	
Option 1	15	-0.8	-55.3	-58.8	-76.3	-62.1	4.2
Default	15	-1.0	-52.2	-65.0	-72.3	-63.0	4.1
Option 1	127	7.2	-48.0	-43.1	-59.7	-44.7	11.2
Default	127	7.5	-45.2	-56.3	-69.2	-54.2	11.8

Note:

1. The raw power settings 15 and 127 correspond to the maximum output power of the 0 dBm and 8 dBm PAs.
2. The current consumption was measured in EM1 sleep mode.

Table 6.3. Radiated TX Performance[1]

Matching	Power Setting (raw)	Frequency (2450 MHz)	Measured Un-modulated EIRP (dBm)[3]	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
				Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated-Margin (dB)	
Option 1	15	Fund	-0.1[2]	N/A	-0.1	30.1	30
		2nd	-57.1	-3.3	-60.4	19.2	-41.2
		3rd	-52.2	-5.2	-57.4	16.2	-41.2
		4th	-57.0	-6.7	-63.7	33.7	-30
		5th	-55.3	-6.7	-62.0	20.8	-41.2
	127	Fund	8.1[2]	N/A	8.1	21.9	30
		2nd	-54.1	-3.3	-57.4	16.2	-41.2
		3rd	-40.2	-5.2	-45.4	4.2	-41.2
		4th	-49.1	-6.7	-55.8	25.8	-30
		5th	-41.73	-6.7	-48.43	7.23	-41.2

Notes:

1. The on-board printed Inverter-F (IFA) antenna was used for the radiated measurements.
2. Average of the center and edge channel fundamental powers across all symmetry planes.
3. Worst case harmonics across all symmetry planes.

The radiated TX results show that the critical 3rd harmonic passes the FCC limit of -41.2 dBm with 4.2 dB modulated margin with BLE 1 Mb/s modulation, and therefore proves to be a good compromise between BOM cost and overall RF performance.

Notes:

- Replacing L1 = 1.7 nH to 1.6 nH improves RX sensitivity (on the worst-case frequency) by +0.3 dB. The downside of this change is that the modulated margin on the 5th harmonic decreases to around 1-2 dB, which is close to the limit. Therefore, the recommended matching network should have L1 = 1.7 nH despite the RX sensitivity degradation.
- Using the VDD BOM reduction but keeping the radio board 3-element T-match shows no notable degradation in RF performance.

6.2 WLCSP39 Package with Internal Buck and Boost Converters

6.2.1 Design Considerations

This section summarizes the requirements and considerations for the BOM-optimized designs for EFR32xG27/29 WLCSP devices with buck and boost converters.

- The on-chip dc-dc converters need an external inductor and capacitor for proper operation. The inductor used is the same as in the BRD4110B and 4111B reference designs. Refer to these schematics and the data sheet of the device for the buck and boost mode hardware configurations.
- For EFR32xG27/29, it is recommended to supply PAVDD, RFVDD, and DVDD from the on-chip dc-dc converter to achieve better current consumption (i.e., better power efficiency) and immunity against the battery voltage level drop and to avoid output power or RF range degradation due to battery aging.
- For BLE 2.4 GHz applications, EFR32 needs to meet the BT Sleep Clock accuracy specification of ±500 ppm. EFR32xG27/29 has an internal RC oscillator 32 kHz (LFRCO) with precision mode that meets the BLE requirements, so an external low frequency crystal can be eliminated unless the application requires a higher clock accuracy. See section 4.3 Crystal Requirements if LFXO needs to be used in the design.
- The high frequency XTAL is required for operating the RF and MCU parts of the EFR32. Load capacitors are not needed. See section 4.3 Crystal Requirements for the XTAL requirements.
- The RF front-end matching consists of a dc-blocking capacitor and a 2-element LC matching network to filter the harmonics. Two different matching networks are recommended for the 0 and the 4 dBm PA.
- The following power supply restrictions need to be followed on the EFR32 Series 2 devices:
  - VREGVDD ≥ DVDD
  - DVDD ≥ DECOUPLE
  - PAVDD ≥ RFVDD
  - AVDD and IOVDD: No dependency with each other or any other supply pin

Note: The high power PA is capable of providing 8 dBm output power in both buck and boost dc-dc modes, but it is recommended to set the power to maximum 4 dBm for optimal performance and FCC compliance.

6.2.2 Recommended BOM-Optimized 2.4 GHz Solutions

The original radio boards contain various supply filtering parts and a 3-element T-matching network. Both of these can be reduced to lower manufacturing costs.

The changes made and the measurements are summarized in the following tables and schematic figures.

Every measurement was taken on the BRD4110B (buck) and BRD4111B (boost) Radio Boards (with indicated minor modifications if it was necessary), and every part used is 0201 size (deviating from this size will require additional tuning).

Different minimum BOM designs (matching network) are proposed for the 0 and the 4 dBm PA with acceptable margins on the FCC radiated harmonic limits. The designs can be used for both buck and boost dc-dc modes. TX power and harmonics and RX sensitivity did not degrade by the VDD filtering BOM reduction. Performance degradation was only attributed to the matching network BOM reduction.

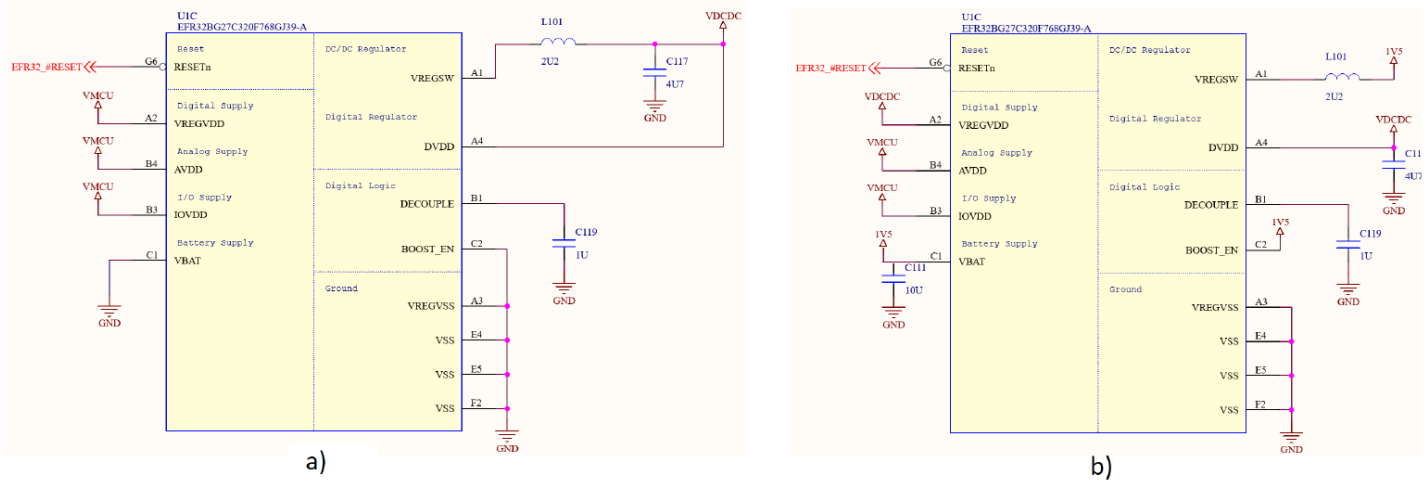


Figure 6.3. Power Supply Filtering Schematic for a) Buck b) Boost DC-DC Mode

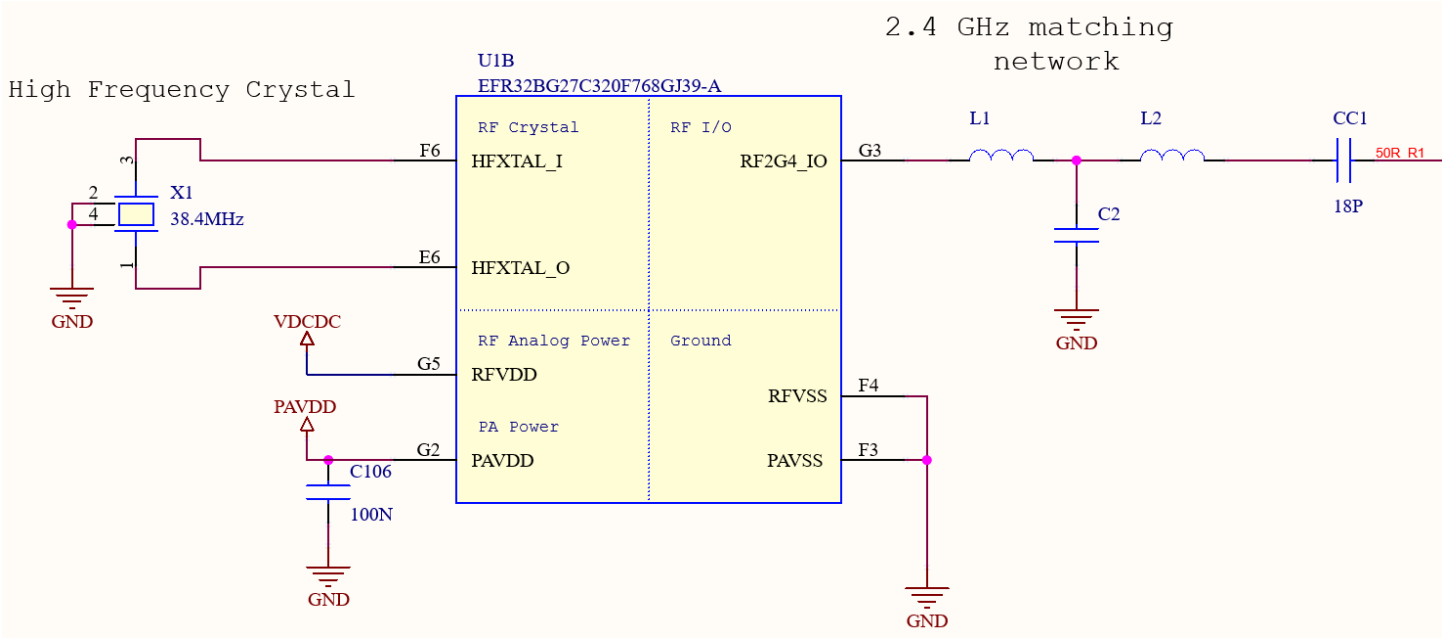


Figure 6.4. RF Components Schematic

The tables below show the results of the RF measurements.

Table 6.4. Conducted RX Performance

BOM	Sensitivity (dBm)[1]		Values						
			Matching Network			VDD Filtering Network			
	BLE 1 Mbps, 37 byte pay-load	802.15.4 Zigbee	L1	C2	L2	L_DCDC	C_DCDC	C_VBAT	C_PAVDD
Minimum 0 dBm	-99.1	-102.1	2.9 nH	0.7 pF	0 Ω[2]	2.2 µH	4.7 µF	10 µF[3]	100 nF[4]
Minimum 4 dBm	-98.6	-101.6	3.4 nH	0.8 pF	0 Ω[2]				
Default	-99.2	-102.2	3.5 nH	1.3 pF	3.8 nH	Original BRD4110B and BRD4111B BOM (18 components in total)			

Notes:

1. The frequency for this table was selected in the 2.4 GHz band where the sensitivity degradation was the largest (0.6 dB). The degradation was seen at the 2450-2470 MHz channels, while on the rest of the channels it was closer to the data sheet value.
2. L2 was shorted with a 0 Ω resistor. The footprint can be removed from the design.
3. C_VBAT = 10 µF is necessary only for the boost dc-dc mode. For buck mode, VBAT should be directly grounded.
4. C_PAVDD = 100 nF is responsible for filtering the HFXO spurs around the carrier.

Table 6.5. Conducted TX Performance

Matching	Power Setting (raw)[1]	Max. TX Output Power (dBm)	Conducted TX Harmonics @2450 MHz (dBm)				I_TX[2, 3]
			2nd	3rd	4th	5th	
Minimum BOM 0 dBm	15	0.5	-53.6	-44.1	-101	-95	11
Default 0 dBm	15	0.2	-50.9	-56.6	-90	-73.5	11.1
Minimum BOM 4 dBm	43	4.0	-42.5	-44.7	-98	-62	17.7
Default 4 dBm	40	4.0	-50.4	-56.6	-90.6	-73.5	18

Notes:

1. The raw power settings 15 and 40/43 correspond to the maximum output power of the 0 dBm, and the 4 dBm output power of the 8 dBm PA.
2. The current consumption was measured for all VDD pins (total current).
3. The current consumption is shown for the boost dc-dc mode application. In buck mode, overall better current consumption is expected. The slight performance improvement from default to the minimum BOM is similar in buck mode.

Table 6.6. Radiated TX Performance[1]

Matching	Power Setting (raw)	Frequency (2450 MHz)	Measured Un-modulated EIRP (dBm)[2]	BLE 1 Mb/s Coded Modulation			Limit in EIRP (dBm)
				Correction Factor (dB)	Calculated Modulated EIRP (dBm)	Modulated Margin (dB)	
0 dBm	15	Fund	2.3[3]	N/A	2.3	27.7	30
		2nd	-46.0	-3.3	-49.3	-8.1	-41.2
		3rd	-40.9	-5.2	-46.1	-4.9	-41.2
		4th	-57.1	-6.7	-63.8	-33.8	-30
		5th	-55.4	-6.7	-62.1	-20.9	-41.2
4 dBm	43	Fund	7.5[3]	N/A	7.5	22.5	30
		2nd	-45.4	-3.3	-48.7	-7.5	-41.2
		3rd	-39.6	-5.2	-44.8	-3.6	-41.2
		4th	-57	-6.7	-63.7	-33.7	-30
		5th	-52	-6.7	-58.7	-17.5	-41.2

Notes:

1. The on-board printed Inverter-F (IFA) antenna was used for the radiated measurements.
2. Worst case harmonics across all symmetry planes.
3. Average of the center and edge channel fundamental powers across all symmetry planes.

The radiated TX results show that the critical 3rd harmonic passes the FCC limit of -41.2 dBm with BLE 1 Mb/s modulation with:

- 3.6 dB modulated margin at 4 dBm output power
- 4.9 dB modulated margin at 0 dBm output power

Therefore, the design proves to be a good compromise between BOM cost and overall RF performance.

Notes:

- Decreasing the values of the 4 dBm matching network improves RX sensitivity by +0.3 dB. The downside of these changes is that the modulated margin on the 3rd harmonic decreases to around 1-2 dB, which is close to the limit. Therefore, the recommended matching network should be as introduced above despite the RX sensitivity degradation.
- Using the VDD BOM reduction but keeping the radio board 3-element T-match shows no notable degradation in RF performance.

7. Revision History

Revision 0.9

July 2025
- Added EFR32xG29 QFN40 and WLCSP45 package information.

Revision 0.8

September 2023
- Added EFR32xG24 WLCSP42 package information.

Revision 0.7

August 2023
- Added EFR32xG27 WLCSP39 package with internal buck and boost converters.

Revision 0.6

August 2023
- Added EFR32xG21.

Revision 0.5

July 2023
- Added EFR32xG27 QFN40 package with internal buck-converter.

Revision 0.4

February 2023
- Added EFR32xG24.

Revision 0.3

August 2021
- Added schematic and RF test results using T match.

Revision 0.2

November 2020
- Updated minimal BOM recommendation to be applicable to the 6 dBm PA.
- Added test results of minimal BOM testing on radio board BRD4182A.
- Updated test results of EFR32xG22 2-layer reference design.

Revision 0.1

March 2020
- Initial release.

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