# AN976: CP2101/2/3/4/9 to CP2102N Porting Guide

The CP2102N USB-to-UART bridge device has been designed to be a replacement and upgrade for existing single-interface CP210x USB-to-UART devices.

For some devices, such as the CP2102 and CP2104, the CP2102N is virtually a drop-in replacement. Apart from the addition of two resistors, no other hardware or software changes are required to use the CP2102N in existing designs. For other devices, slight package or feature differences may require minor changes to hardware or host software.

This application note describes in detail the steps required to integrate a CP2102N device into a design in place of a previous CP210x device. Devices covered by this application note are: CP2101, CP2102/9, CP2103, and CP2104. Multiple-interface devices, such as the CP2105 and CP2108, are not discussed.

KEY POINTS

- The CP2102N maintains a high degree of pin and feature compatibility with most existing CP210x devices.
- Designs will require minimal hardware or software changes when migrating to the CP2102N.
- The CP2102N provides a migration path for:
  - CP2101
  - CP2102/9
  - CP2103
  - CP2104

Existing Design

USB to UART Bridge Device
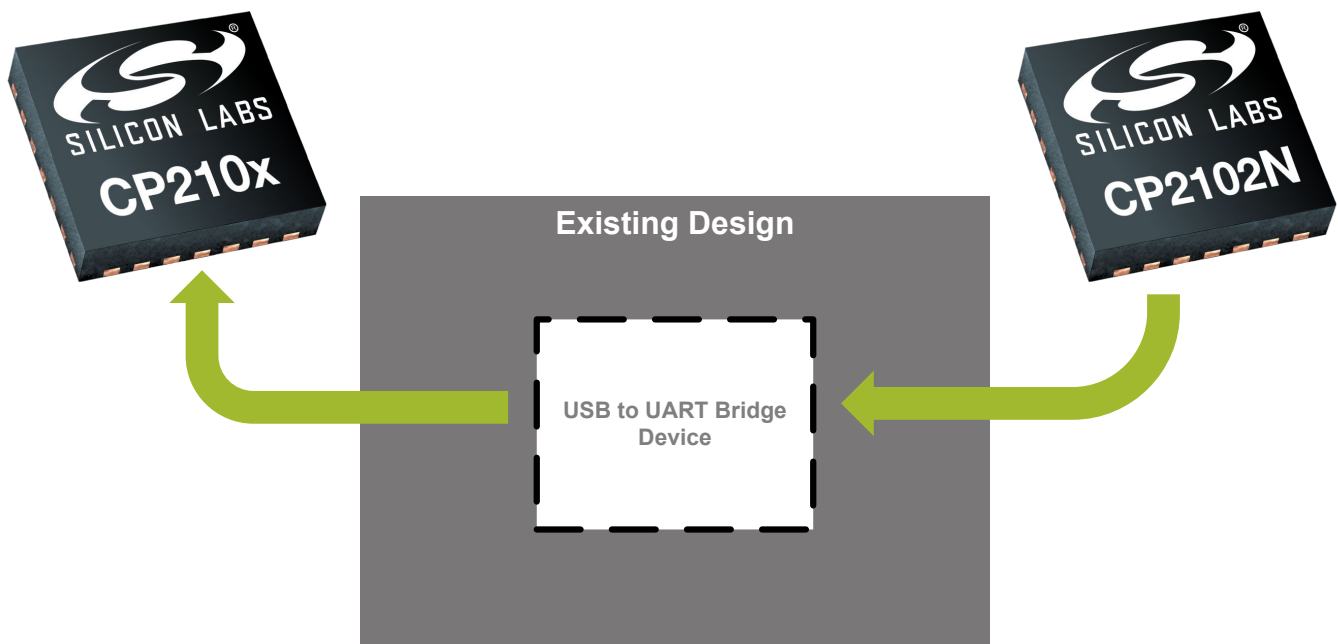
1. Device Comparison

1.1 Feature Compatibility

A full feature comparison table for all CP210x devices, including the CP2102N, is given below. In general, the CP2102N meets or exceeds the feature set of all previous CP210x devices.

Table 1.1. CP210x Family Features

Feature	CP2101	CP2102	CP2109	CP2103	CP2104	CP2102N
Re-programmable	X	X		X		X
One-time-programmable			X		X	
UART Features						
Max Baud Rate	921.6kbps	921.6kbps	921.6kbps	921.6kbps	921.6kbps	3Mbps
Data Bits: 8	X	X	X	X	X	X
Data Bits: 5, 6, 7		X	X	X	X	X
Stop Bits: 1	X	X	X	X	X	X
Stop Bits: 1.5, 2		X	X	X	X	X
Parity Bit: Odd, Even, None	X	X	X	X	X	X
Parity Bit: Mark, Space		X	X	X	X	X
Hardware handshake	X	X	X	X	X	X
X-ON/X-OFF handshake	X	X	X	X	X	X
Event Character Support	X	X	X			X
Line Break Transmission		X	X		X	X* (see note)
Baud Rate Aliasing		X	X	X		
Driver Support						
Virtual COM Port Driver	X	X	X	X	X	X
USBXpress Driver	X	X	X	X	X	X
Other Features						
RS-232 support	X	X	X	X	X	X
RS-485 support				X	X	X
GPIOs	None	None	None	4	4	4-7
Battery Charger Detect						X
Remote Wake-up						X
Clock Output						X

Note: The CP2102N cannot directly generate Line Break Conditions. The use of this feature is generally considered uncommon, although it was previously supported on CP2102/9 devices. A Line Break Condition occurs when the receiver input is held to logic low (i.e. zero) for some period of time, generally for more than one character time. This condition is seen by the receiver as a character with all zero bits with a framing error. A user can potentially emulate this on a CP2102N, however, by changing the baud rate to be slower than expected, then transmitting a null character. The CP2102N does have the capability to receive Line Breaks.

1.2 Pin Compatibility

With the exception of its VBUS pin, which must be connected to a voltage divider for proper operation, the CP2102N is largely pin-compatible with most CP210x devices. Below is a table of variants of the CP2102N that can be used to replace previous CP210x devices.

Table 1.2. CP2102N Replacements for CP210x Devices

CP210x Device	Pin-Compatible Replacement
CP2101	CP2102N-A02-GQFN28
CP2102/9	CP2102N-A02-GQFN28
CP2103	None (refer to 2.3 CP2103 to CP2102N for migration considerations)
CP2104	CP2102N-A02-GQFN24

As the CP2102N datasheet notes, there are two relevant restrictions on the VBUS pin voltage in self-powered and bus-powered configurations. The first is the absolute maximum voltage allowed on the VBUS pin, which is defined as VIO + 2.5 V in Absolute Maximum Ratings table. The second is the input high voltage (VIH) that is applied to VBUS when the device is connected to a bus, which is defined as VIO – 0.6 V in the table of GPIO specifications.

A resistor divider (or functionally-equivalent circuit) on VBUS, as shown in Figure 1.1 Bus-Powered Connection Diagram for USB Pins on page 3 and Figure 1.2 Self-Powered Connection Diagram for USB Pins on page 4 for bus- and self-powered operation, respectively, is required to meet these specifications and ensure reliable device operation. In this case, the current limitation of the resistor divider prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while the device is not powered.

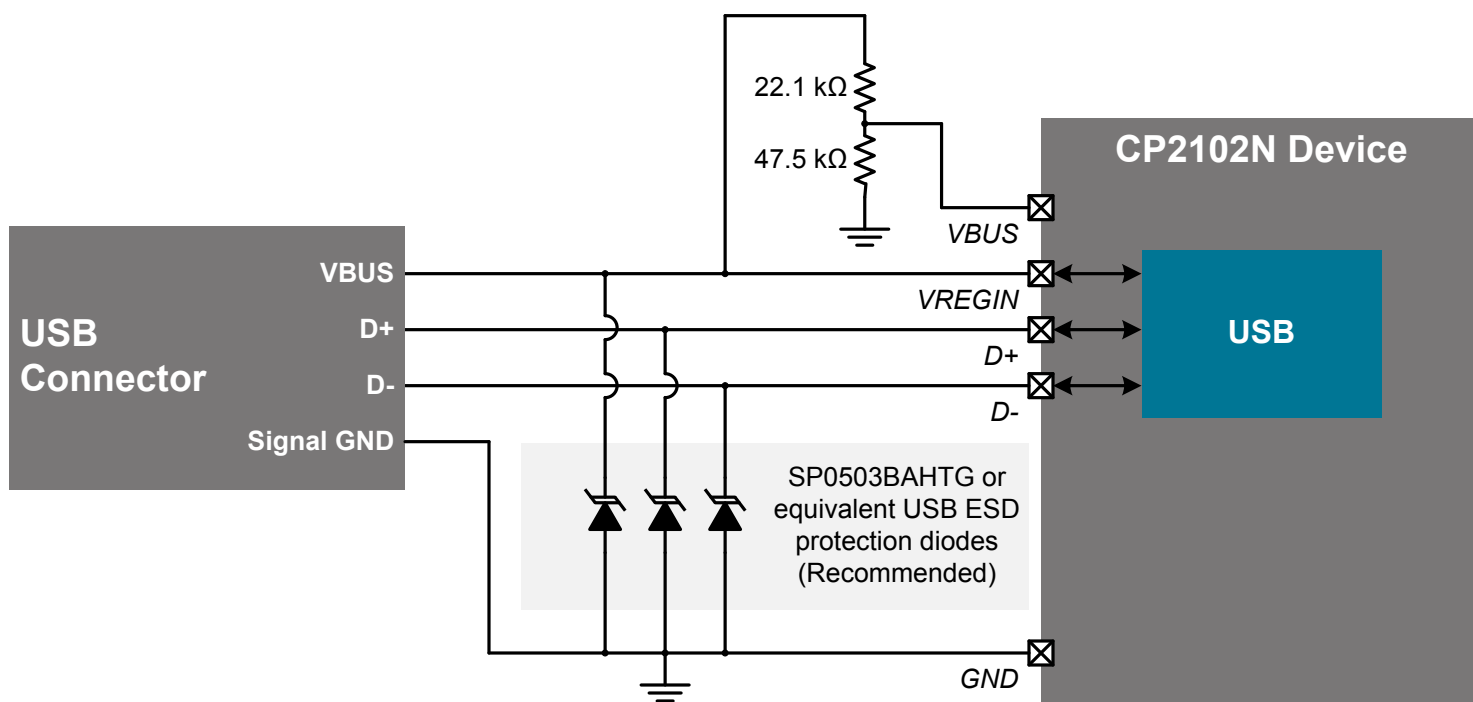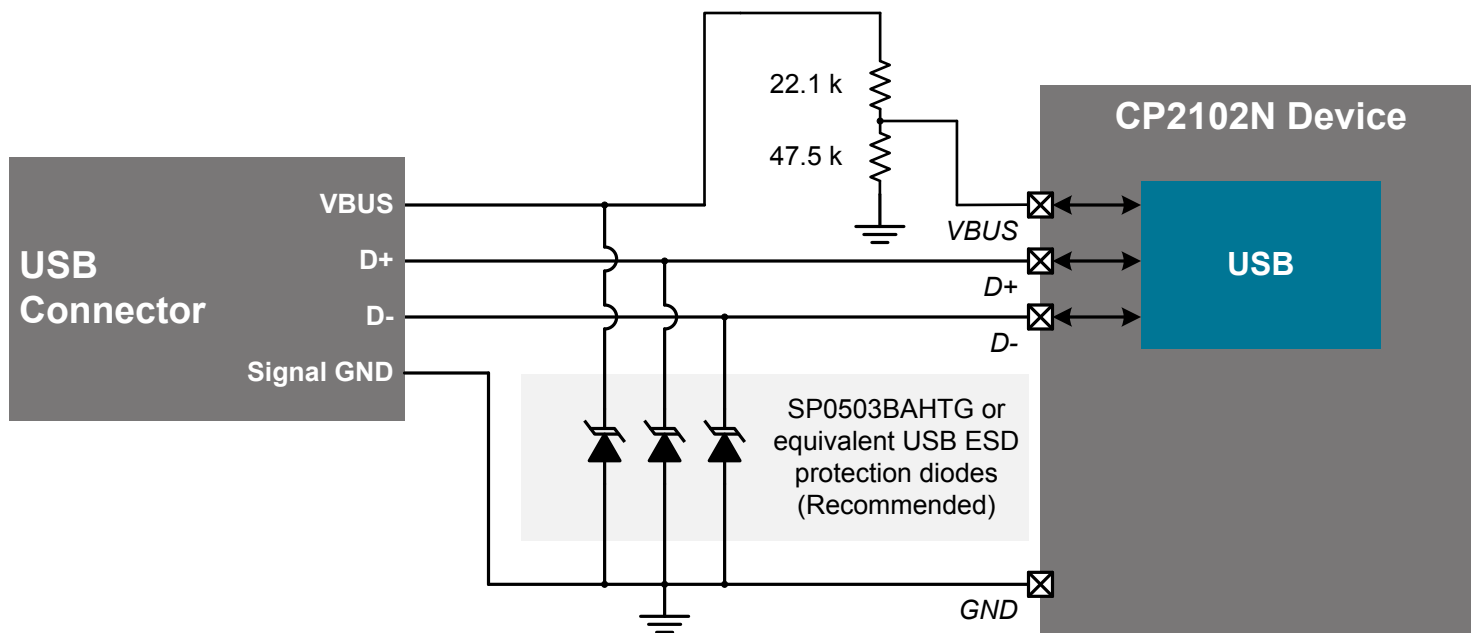**Figure 1.1. Bus-Powered Connection Diagram for USB Pins**

Figure 1.2. Self-Powered Connection Diagram for USB Pins

1.3 Configuration Compatibility

While the CP2102N supports the same configuration parameters as the CP210x, the means of programming these into the device are different. Of particular note is the fact that the configuration data structure for the CP2102N has an entirely different format than that used for the CP210x. In short, it is not possible to write the configuration data for a legacy CP210x device to the CP2102N and vice versa.

Furthermore, if the CP210x manufacturing DLL is incorporated into custom software as part of a production or test flow, the API calls used to read and write the individual parameters on a CP210x device **cannot** be used with the CP2102N. Thus, calls to any of the functions listed in Table 1.3 CP210x Configuration APIs on page 5 and documented in *AN721: USBXpress™ Device Configuration and Programming Guide* must be replaced wholesale with calls to the new `CP210x_GetConfig` and `CP210x_SetConfig` functions that are specific to the CP2102N.

Table 1.3. CP210x Configuration APIs

Read Call	Write Call
CP210x_GetDeviceVid	CP210x_SetVid
CP210x_GetDevicePid	CP210x_SetPid
CP210x_GetDeviceManufacturerString	CP210x_SetManufacturerString
CP210x_GetDeviceProductString	CP210x_SetProductString
CP210x_GetDeviceSerialNumber	CP210x_SetSerialNumber
CP210x_GetSelfPower	CP210x_SetSelfPower
CP210x_GetMaxPower	CP210x_SetMaxPower
CP210x_GetDeviceVersion	CP210x_SetDeviceVersion
CP210x_GetBaudRateConfig	CP210x_SetBaudRateConfig
CP210x_GetLockValue	CP210x_SetLockValue
CP210x_GetPortConfig	CP210x_SetPortConfig

2. Device Migration

The following sections describe the migration considerations when transitioning from an existing CP210x device to a CP2102N device.

2.1 CP2101 to CP2102N

Hardware Compatibility

The CP2102N-A02-GQFN28 is pin compatible with the CP2101 with the addition of the voltage divider circuit shown in Figure 1.1 Bus-Powered Connection Diagram for USB Pins on page 3 and Figure 1.2 Self-Powered Connection Diagram for USB Pins on page 4.

The CP2102N does, however, have extra functionality on pins 13 through 22. A new design may want to take advantage of these extra pins, but they can be safely left unconnected.

Software Compatibility

The CP2102N is fully feature compatible with the CP2101. No software changes will be required when transitioning a CP2101 design to the CP2012N.

The CP2102N does have several common features that the CP2101 lacks. For example, the CP2101 only allows for 8 data bits per frame, where the CP2102N has the ability for 5, 6, 7, or 8 data bits. If desired, the CP2102N can be customized to disable these additional features.

2.2 CP2102/9 to CP2102N

Hardware Compatibility

The CP2102N-A02-GQFN28 is pin compatible with the CP2102/9 with the addition of the voltage divider circuit shown in Figure 1.1 Bus-Powered Connection Diagram for USB Pins on page 3 and Figure 1.2 Self-Powered Connection Diagram for USB Pins on page 4.

The CP2102N does, however, have extra functionality on pins 13 through 22. A new design may want to take advantage of these extra pins, but they can be safely left unconnected.

The CP2109 has an additional hardware requirement that the VPP pin (pin 18) should be connected to a capacitor to ground for in-system programming. This capacitor is not required on the CP2102N and can be safely omitted.

Software Compatibility

The CP2102N is feature compatible with the CP2102/9, with two exceptions:
*   Baud Rate Aliasing
*   Line Breaks / Break Conditions

Baud Rate Aliasing is a feature that allows a device to use a pre-defined baud rate in place of a baud rate that is requested by the user. For example, a device using Baud Rate Aliasing can be programmed to use a baud rate of 45 bps whenever 300 bps is requested. Baud Rate Aliasing is not supported on the CP2102N.

If Baud Rate Aliasing is used in a CP2102/9 design, the CP2102N is incompatible as a replacement.

Line Breaks (also called a Break Condition) occur when the transmission line to logic low for more than one character time. The CP2102/9 devices have the ability to transmit a Line Break or Break Condition by directly setting the device's break state property. This forces the transmission line to logic low until the break state property is cleared. This feature is not directly supported on the CP2102N. However, a break condition can be emulated by temporarily lowering the baud rate, then transmitting a null character. The duration of this emulated break condition can be controlled by adjusting the baud rate, but it cannot exceed 27ms (8 bits at the lowest available baud rate, 300bps).

If Break Conditions are used in a CP2102/9 design, care must be taken to assure that the CP2102N can emulate these conditions correctly.

2.3 CP2103 to CP2102N

Hardware Compatibility

The CP2102N does not have a pin-compatible variant that can replace the CP2103. The CP2103 QFN28 package has an additional VIO pin at pin 5 which shifts the function of previous pins on the package clock-wise around the package by one pin compared to the CP2102N QFN28 package. This affects pins 1-4 and 22-28. All other pins remain in the same configuration.

If a separate VIO rail is required for a design, the smaller CP2102N QFN24 variant can be used. This variant has an identical functionality set as the CP2103, but in the smaller QFN24 package.

Beside this difference in pin-outs, no other hardware changes are required to migrate from the CP2103 to the CP2102N.

Software Compatibility

The CP2102N is fully feature compatible with the CP2103 with one exception: Baud Rate Aliasing.

Baud Rate Aliasing is a feature that allows a device to use a pre-defined baud rate in place of a baud rate that is requested by the user. For example, a device using Baud Rate Aliasing can be programmed to use a baud rate of 45 bps whenever 300 bps is requested. Baud Rate Aliasing is not supported on the CP2102N.

If Baud Rate Aliasing is used in a CP2103 design, the CP2102N is incompatible as a replacement.

2.4 CP2104 to CP2102N

Hardware Compatibility

The CP2102N-A02-GQFN24 is pin compatible with the CP2104 with the addition of the voltage divider circuit shown in Figure 1.1 Bus-Powered Connection Diagram for USB Pins on page 3 and Figure 1.2 Self-Powered Connection Diagram for USB Pins on page 4. No other hardware changes are required when transitioning a CP2104 design to the CP2102N. The CP2104 does require a capacitor between VPP (pin 16) and ground for in-system programming, but this pin is not connected on the CP2102N. Whether or not this capacitor is attached to this pin will have no effect on the CP2102N.

Software Compatibility

The CP2102N is fully feature compatible with the CP2104. No software changes will be required when transitioning a CP2104 design to the CP2012N.

3. Revision History

Revision 1.3

Mar, 2022

- Added X to CP2104 Line Break Transmission in Table 1.1 CP210x Family Features on page 2.
- Updated CP2102-A01-GQFN28 with CP2102-A02-GQFN28 in Table 1.2 CP2102N Replacements for CP210x Device on page 3 and Chapter 2. Device Migration.
- Updated Figure 1.1 Bus-Powered Connection Diagram for USB Pin on page 3 and Figure 1.2 Self-Powered Connection Diagram for USB Pin on page 4 to reflect new SP0503BAHTG protection device RoHS-compliant part number.
- Corrected typo in Configuration Compatibility section names.

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