Timing Solutions

PRODUCT SELECTOR GUIDE

Timing

The industry’s broadest portfolio of oscillators, clock buffers, clock generators, PCI Express (PCIe) clocks, jitter attenuators and SyncE/IEEE 1588 clocks.

Timing Solutions

Silicon Labs offers a broad portfolio of timing products that enable hardware designers to simplify clock generation, clock distribution, jitter attenuation and network synchronization. These products combine best-in-class jitter performance and frequency flexibility, enabling customers to easily architect optimized clock tree solutions. Custom samples are available in 1-2 weeks, easing design and reducing time-to-market.

Products

**Oscillators**
- Any frequency up to 3.0 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

**Clock Generators**
- Any-frequency, any-output
- Ultra-low jitter: 70 fs RMS
- Clock tree on a chip replaces clocks and XOs

**Clock Buffers**
- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

**Jitter Attenuating Clocks/Network Synchronizers**
- Any frequency, any output
- Ultra-low jitter: 70 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Applications

- Enterprise routers
- Cable/DSL
- PON
- Base stations
- Small cells/DAS
- Backhaul/Fronthaul
- Broadcast video
- Industrial
- Medical imaging
- Test and measurement
- Emulation & prototyping
- Aerospace and defense

- Switches/servers
- Storage/security
- Search acceleration
- Machine learning

- Data center interconnect
- 100G/400G Optical Transport (OTN)
- WDM
- Carrier Ethernet
- Enterprise routers
- Cable/DSL
- PON
Silicon Labs offers the industry’s broadest portfolio of high performance, low jitter XOs and VCXOs. Silicon Labs’ new Si54x and Si56x Ultra Series™ family of high performance XOs delivers best-in-class jitter performance and frequency flexibility. All devices are highly customizable, with samples of any XO available with 1-2 week lead times.

## Portfolio Key Features
- Industry’s lowest jitter any frequency XOs
- Jitter as low as 80 fs RMS typ
- Any frequency up to 3.0 GHz
- Single, dual and I2C prog. options
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Superior stability vs. SAW oscillators
- Best-in-class power supply noise rejection
- Single device supports 1.8 – 3.3 V operation
- -40° to +85° C operation
- 5x7 mm, 3.2x5mm, 2.5x3.2mm
- Samples in 1-2 weeks

## Featured Products

### Ultra Low Jitter
- **Si545**: Single
  - Frequency Range: 200 kHz to 1.5 GHz
  - Typical Jitter (fs RMS): 80
  - Total Stability (±PPM): 25, 50
  - Available Voltage: 1.8 - 3.3
  - Package Size: 5 x 7

- **Si546**: Dual
  - Frequency Range: 200 kHz to 1.5 GHz
  - Typical Jitter (fs RMS): 125
  - Total Stability (±PPM): 25, 50
  - Available Voltage: 1.8 - 3.3
  - Package Size: 5 x 7

- **Si547**: Quad
  - Frequency Range: 200 kHz to 1.5 GHz
  - Typical Jitter (fs RMS): 90
  - Total Stability (±PPM): 50
  - Available Voltage: 1.8 - 3.3
  - Package Size: 5 x 7

### Low Jitter
- **Si530/1**: Single
  - Frequency Range: 10 MHz to 1.4 GHz
  - Typical Jitter (fs RMS): 300
  - Total Stability (±PPM): 31.5, 61.5
  - Available Voltage: 1.8, 2.5, 3.3
  - Package Size: 5 x 7

- **Si532/3**: Dual
  - Frequency Range: 10 MHz to 1.4 GHz
  - Typical Jitter (fs RMS): 500
  - Total Stability (±PPM): 30, 50, 100
  - Available Voltage: 1.8, 2.5, 3.3
  - Package Size: 5 x 7

### General Purpose
- **Si590/1**: Single
  - Frequency Range: 10 MHz to 810 MHz
  - Typical Jitter (fs RMS): 500
  - Total Stability (±PPM): 30, 50, 100
  - Available Voltage: 1.8, 2.5, 3.3
  - Package Size: 5 x 7

- **Si598**: Any
  - Frequency Range: 10 MHz to 810 MHz
  - Typical Jitter (fs RMS): 800
  - Total Stability (±PPM): 30, 50, 100
  - Available Voltage: 1.8, 2.5, 3.3
  - Package Size: 5 x 7

### Example Application: 100G/200G Optical Module

- **XO**: 10G/40G/60G/100G/200G Transceiver
- **Driver**: Laser
- **Laser**: TX
- **RX**: Gearbox or Retimer
- **TIA**: PD
- **Driver**: TX

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Voltage-Controlled Crystal Oscillators (VCXO)

Silicon Labs offers the industry’s broadest portfolio of high performance, low jitter XOs and VCXOs. Silicon Labs’ new Si56x Ultra Series™ family of high performance VCXOs deliver exceptional jitter performance and best-in-class control voltage linearity and power supply noise rejection. All devices are highly customizable, with samples of any VCXO available with 1-2 week lead times.

Portfolio Key Features

- Jitter: 100 fs RMS typ (12 kHz – 20 MHz)
- Any frequency up to 3.0 GHz
- Single, dual, quad and I2C prog. options
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Superior linearity vs. traditional VCSO/VCXOs
- Best-in-class power supply noise rejection
- 1.8, 2.5 or 3.3 V
- 5x7 mm, 3.2x5 mm, 2.5x3.2 mm
- -40° to +85° C operation
- Samples in 1-2 weeks

Example Application: Video Format Converter

Master Sync Generator

Video Processing SDI SerDes

Sync Separator

Portfolio 

Featured Voltage-Controlled Crystal Oscillators (VCXO)

<table>
<thead>
<tr>
<th>PERFORMANCE OPTION</th>
<th>PART NUMBER</th>
<th>PART NUMBER</th>
<th>NUMBER OF FREQUENCIES</th>
<th>FREQUENCY RANGE</th>
<th>MIN APR (±PPM)</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
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<td>1.8, 2.5, 3.3</td>
<td>3.2 x 5</td>
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</tbody>
</table>

VCXO | VCXO Software Tools | VCXO Development Tools | Reference Designs
Clock Generators

Silicon Labs offers the industry’s lowest jitter, most frequency flexible, most highly integrated clock generators. Leveraging Silicon Labs’ proven MultiSynth technology, a single clock generator can replace an entire clock tree of multiple oscillators, buffers, clock generators, and muxes, simplifying design and accelerating time to market. Silicon Labs’ comprehensive clock generator portfolio offers optimized solutions for communications, data center, industrial and consumer applications.

Portfolio Key Features
- Ultra-low jitter as low as 69 fs RMS
- Generate any combination of frequencies
- Lowest jitter fractional clock synthesis
- Programmable format per output
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Programmable VDDO per output
- Best-in-class power supply noise rejection
- PCIe Gen 1/2/3/4/5 compliant
- Custom samples in 2 weeks
- ClockBuilder Pro support

Application Example: Data Center Ethernet Switch

CPU Board

Ethernet Switch (MAC/PHY)

Sil332 Clock

Sil391 Clock

Optical Modules

Featured Clock Generators

<table>
<thead>
<tr>
<th>PERFORMANCE OPTION</th>
<th>PART NUMBER</th>
<th>CLOCK INPUTS</th>
<th>CLOCK OUTPUTS</th>
<th>MAX OUTPUT FREQUENCY</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE (MM)</th>
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<td>1.8, 3.3</td>
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Clock Buffers

Silicon Labs offers a comprehensive portfolio of clock buffers. In addition to universal buffers that support any in/out signal format translation, we offer a wide range of differential and single-ended buffers that provide ultra-low additive jitter and low skew clock distribution. Silicon Labs also offers a broad range of low-power PCIe buffers that integrate all termination components while providing compliance with PCIe Gen 1/2/3/4 standards.

Portfolio Key Features
- Ultra-low additive jitter as low as 50 fs RMS
- Clock distribution up to 1.25 GHz
- LVPECL, LVDS, HCSL, CML, LVCMOS
- Pin-selectable signal format
- Individual clock output OE control
- Synchronous, glitchless OE control
- Best-in-class power supply noise rejection
- PCIe: push-pull HCSL drivers
- PCIe: integrated termination resistors
- PCIe: Gen 1/2/3/4/5 compliant
- PCIe: Intel-qualified solutions

Application Example: Switch/Router

![Clock Buffer Diagram]

Featured Clock Buffers

<table>
<thead>
<tr>
<th>PRODUCT FAMILY</th>
<th>PART NUMBER</th>
<th>CLOCK INPUTS</th>
<th>CLOCK OUTPUTS</th>
<th>MAX OUTPUT FREQUENCY</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
<th>VOLTAGE (V)</th>
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<td>6, 8, 12, 15, 19</td>
<td>133 MHz</td>
<td>80</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>3.3</td>
<td>40QFN</td>
</tr>
<tr>
<td>TCXO BUFFERS</td>
<td>SL10060/1</td>
<td>1</td>
<td>3</td>
<td>52 MHz</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8</td>
<td>TDFN10</td>
</tr>
</tbody>
</table>

Buffers  PCIe Clock Jitter Tool  Buffer Development Tools  Reference Designs
Jitter Attenuating Clocks

Silicon Labs offers the industry’s lowest jitter, most frequency flexible, most highly integrated jitter attenuating clock generators. Leveraging Silicon Labs’ proven DSPLL and MultiSynth technology, a single jitter attenuating clock can synchronize to a wide range of different clocks, filter jitter, and provide any combination of output frequencies. Silicon Labs offers an extensive range of jitter attenuating clocks to solve the most complex timing challenges in 100G+ packet optical transport and Ethernet designs.

### Portfolio Key Features
- Generate any combination of output frequencies
- Ultra-low jitter as low as 69 fs RMS
- Enhanced hitless switching
- Programmable loop bandwidth down to 0.1 Hz
- Programmable format per output (LVPECL, LVDS, HCSL, CML, LVCMOS)
- Programmable VDDO per output
- Best-in-class power supply noise rejection
- Custom samples in 2 weeks
- ClockBuilder Pro support

### Application Example:

![Diagram showing clock generation and application examples](image)

### Featured Jitter Attenuating Clocks

<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>PART NUMBER</th>
<th># DSPLL</th>
<th># MULTISYNTH</th>
<th>CLOCK INPUTS</th>
<th>CLOCK OUTPUTS</th>
<th>MAX OUTPUT FREQUENCY</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OPTICAL NETWORKING &amp; BROADBAND</strong></td>
<td>Si5395/4/2</td>
<td>1</td>
<td>5/4/2</td>
<td>4</td>
<td>12/4/2</td>
<td>1028 MHz</td>
<td>69</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN64/QFN44</td>
</tr>
<tr>
<td></td>
<td>Si5345/4/2</td>
<td>1</td>
<td>5/4/2</td>
<td>4</td>
<td>10/4/2</td>
<td>1028 MHz</td>
<td>90</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN44/QFN44</td>
</tr>
<tr>
<td></td>
<td>Si5347</td>
<td>4</td>
<td>4</td>
<td>8/4</td>
<td>720 MHz</td>
<td>90</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN64</td>
</tr>
<tr>
<td></td>
<td>Si5346</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>720 MHz</td>
<td>90</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN44</td>
</tr>
<tr>
<td><strong>COHERENT OPTICS</strong></td>
<td>Si5344H/42H</td>
<td>1</td>
<td>21</td>
<td>2</td>
<td>4/2</td>
<td>2.75 GHz</td>
<td>50</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 2.5, 3.3</td>
<td>QFN44</td>
</tr>
</tbody>
</table>

### Categories
- Jitter Attenuators
- JA Software Tools
- JA Development Tools
- Reference Designs
Wireless Clocks

Silicon Labs offers the industry’s most highly integrated clocking solutions for radio access networks. Leveraging Silicon Labs’ proven DSPLL and MultiSynth technology, a single jitter attenuating clock can synchronize to a wide range of different clocks, filter jitter, and generate LTE, Ethernet and general-purpose clocks from a single device. All PLL components are integrated on-chip, eliminating the need for discrete VCXOs, XOs and loop filters in the design.

**Portfolio Key Features**
- Ultra-low phase noise
- Replaces multiple clock IC’s and VCXO’s
- Generates LTE & Ethernet clocks from single IC
- No external loop filter
- Integrated crystal option
- Noise floor: -165 dBC/Hz
- Best-in-class power supply noise rejection
- Custom samples in 2 weeks
- ClockBuilder Pro support

**Application Example: Small Cell / DAS**

**Featured Wireless Clock**

<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>PART NUMBER</th>
<th># DSPLL</th>
<th># MULTISYNTH</th>
<th>CLOCK INPUTS</th>
<th>CLOCK OUTPUTS</th>
<th>MAX OUTPUT FREQUENCY</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-RAN SMALL CELLS DAS</td>
<td>Si5386</td>
<td>1</td>
<td>5</td>
<td>4</td>
<td>12</td>
<td>2.94912 GHz</td>
<td>80</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>LGA64 QFN64</td>
</tr>
<tr>
<td>MACRO RRU</td>
<td>Si5380</td>
<td>1</td>
<td>0</td>
<td>4</td>
<td>12</td>
<td>1.475 GHz</td>
<td>65</td>
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<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN64</td>
</tr>
<tr>
<td>BACKHAUL FRONTHAUL BBU</td>
<td>Si5381</td>
<td>4</td>
<td>0</td>
<td>4</td>
<td>12</td>
<td>2.94912 GHz</td>
<td>80</td>
<td>✓</td>
<td>✓</td>
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<td>✓</td>
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<td>1.8, 3.3</td>
<td>LGA64 QFN64</td>
</tr>
<tr>
<td>Si5382</td>
<td>4</td>
<td>0</td>
<td>4</td>
<td>12</td>
<td>2.94912 GHz</td>
<td>80</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>LGA64 QFN64</td>
<td></td>
</tr>
</tbody>
</table>

Wireless Clks  Wireless Clk Software Tools  Wireless Clk Dev Tools  Ref Designs
Network Synchronizers (Synchronous Ethernet / IEEE 1588)

Silicon Labs offers standards-compliant synchronization clocks that lead the industry in terms of jitter performance and power consumption. These products combine network synchronization and jitter attenuation functions in a single device, enabling single-IC designs for pizza box Carrier Ethernet switches/routers and BBU control card applications.

Portfolio Key Features
- Ultra-low jitter as low as 100 fs RMS
- Programmable loop bandwidth down to 1mHz
- Each DSPLL generates any output frequency
- Support for 1PPS/1Hz input and output
- Synchronous, free-run, holdover modes
- Automatic/manual hitless switching
- Pin or SW-controlled 1588 DCO (1 ppt/step)
- Meets G.8262 (SyncE), G.812, G.813
- Suitable for ITU-T G.8273.1 T-GM, G.8273.2
- T-BC, T-TSC
- ClockBuilder Pro support

Application Example: Telecom Boundary Clock

Featured Network Synchronizers

<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>PART NUMBER</th>
<th># DSPLL</th>
<th>GPS SYNC (1 PPS INPUT)</th>
<th>MIN LOOP BANDWIDTH</th>
<th>CLOCK INPUTS</th>
<th>CLOCK OUTPUTS</th>
<th>MAX OUTPUT FREQUENCY</th>
<th>TYP JITTER (fs RMS)</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HCSL</th>
<th>CML</th>
<th>LVCMOS</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPTICAL NETWORKING</td>
<td>Si5383</td>
<td>3</td>
<td>✓</td>
<td>1 mHz</td>
<td>5</td>
<td>7</td>
<td>718.5 MHz</td>
<td>150</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>LGA56</td>
</tr>
<tr>
<td></td>
<td>Si5384</td>
<td>1</td>
<td>✓</td>
<td>1 mHz</td>
<td>5</td>
<td>7</td>
<td>718.5 MHz</td>
<td>150</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>LGA56</td>
</tr>
<tr>
<td>WIRELESS</td>
<td>Si5348</td>
<td>3</td>
<td>✓</td>
<td>1 mHz</td>
<td>5</td>
<td>7</td>
<td>150 MHz</td>
<td>150</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>1.8, 3.3</td>
<td>QFN64</td>
</tr>
</tbody>
</table>