EFM32TG Errata

This document contains information on the EFM32TG errata. The latest available revision of this device is revision D.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March 2021.

1. Errata Summary

The table below lists all known errata for the EFM32TG and all unresolved errata in revision D of the EFM32TG.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround	Exists on Revision:			
		Exists	A	B	C	D
ADC_E118	Requirements for ADC_CLK > 7 MHz	Yes	X	X	X	X
AES_E101	BYTEORDER Does Not Work in Combination with DATASTART/XORSTART	Yes	X	X	X	X
AES_E102	AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set	Yes	X	X	X	X
BOOT_E101	Bootloader Pin Location	No	X	X	—	—
CMU_E108	LFxCLKEN Write	Yes	X	X	—	—
CMU_E109	LFXO Configuration Incorrect	Yes	X	X	—	—
CMU_E115	HFRCO 1 MHz Band Switching	Yes	X	X	X	X
DAC_E109	DAC Output Drift Over Lifetime	Yes	X	X	X	X
DMA_E101	EM2 with WFE and DMA	Yes	X	X	X	X
DMA_E102	2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel	Yes	X	X	X	X
EMU_E105	Debug Unavailable During DMA Processing from EM2	Yes	X	X	—	—
EMU_E107	Interrupts During EM2 Entry	Yes	X	X	X	X
GPIO_E101	GPIO Wakeup from EM4	Yes	X	X	—	—
LCD_E103	Indeterminate Animation Engine Start-Up	Yes	X	X	X	X
LCD_E104	Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO	Yes	X	X	X	X
LES_E101	LESENSE and Schmitt Trigger	Yes	X	X	—	—
LES_E102	LESENSE and DAC CH1 Configuration	Yes	X	X	—	—
LES_E103	AUXHFRCO and LESENSE	Yes	X	X	—	—
LES_E104	LFPRESC Can Extend Channel Start-Up Delay	Yes	X	X	X	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	X	X	X	X
PRS_E101	Edge Detect on GPIO/ACMP	No	X	X	X	X
RMU_E102	Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers	Yes	X	X	X	—
RMU_E103	Reset May Fail to Trigger During Supply Voltage Brownouts	Yes	X	X	X	—
TIMER_E102	Timer Capture and Debugger	Yes	X	X	X	X
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	No	X	X	X	X
USART_E112	USART AUTOTX Continues to Transmit Even With Full RX Buffer	No	X	X	X	X
USART_E113	IrDA Modulation and Transmission of PRS Input Data	Yes	X	X	X	X

Designator	Title/Problem	Workaround Exists	Exists on Revision:			
			A	B	C	D
WDOG_E103	WDOG EM2 Detection with LFXO Digital/Sine Input	Yes	X	X	X	X

2. Current Errata Descriptions

2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

Description of Errata
If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification.
Affected Conditions / Impacts
Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits.
Workaround
For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements.
Resolution
There is currently no resolution for this issue.

2.2 AES_E101 — BYTEORDER Does Not Work in Combination with DATASTART/XORSTART

Description of Errata
When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART.
Affected Conditions / Impacts
If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.
Workaround
Do not use BYTEORDER in combination with DATASTART or XORSTART.
Resolution
There is currently no resolution for this issue.

2.3 AES_E102 — AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set

Description of Errata
When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.
Affected Conditions / Impacts
If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.
Workaround
If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
Resolution
There is currently no resolution for this issue.

2.4 CMU_E115 — HFRCO 1 MHz Band Switching

Description of Errata
Switching to or from the 1 MHz band of the HFRCO or AUXHFRCO may cause a hard fault even at the maximum supported number of wait states.
Affected Conditions / Impacts
When the HFRCO or AUXHFRCO is selected as a clock source (e.g., the HFRCO has been selected as the HFCLK source) and the device is running with the maximum supported number of wait states, switching to or from the 1 MHz band can possibly cause a clock glitch that results in unexpected behavior or a hard fault.
Workaround
Before switching to or from the 1 MHz band when the HFRCO or AUXHFRCO is selected as the clock source, first switch to another stable clock source (such as the LFRCO). For example, when switching from the 21 MHz band to the 1 MHz band, the following procedure needs to be followed: 1. Select another stable clock source by writing to the HFCLKSEL field of the CMU_CMD register. 2. Wait until the clock source shows that it has been selected in the CMU_STATUS register, (e.g., CMU_STATUS_LFRCOSEL = 1). 3. Program the CMU_HFRCOCTRL register to select the 1 MHz band and tuning value. 4. Wait until the HFRCO has stabilized at the new frequency by waiting for the HFRCORDY bit in the CMU_STATUS register to change for 0 to 1. 5. Select the HFRCO as the clock source by writing to the HFCLKSEL field of the CMU_CMD register.
Resolution
There is currently no resolution for this issue.

2.5 DAC_E109 — DAC Output Drift Over Lifetime

Description of Errata
The voltage output of the DAC might drift over time.
Affected Conditions / Impacts
When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.
Workaround
Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
Resolution
There is currently no resolution for this issue.

2.6 DMA_E101 — EM2 with WFE and DMA

Description of Errata
WFE does not work for the DMA in EM2.
Affected Conditions / Impacts
In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.
Workaround
Use WFI (Wait for Interrupt) or EM1 instead.
Resolution
There is currently no resolution for this issue.

2.7 DMA_E102 — 2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel

Description of Errata
When performing a 2D copy (rectangular copy) on one DMA channel, more data than is specified is occasionally transferred from the source buffer if another channel is being used in ping-pong or scatter-gather mode.
Affected Conditions / Impacts
The incorrect number of bytes is transferred during the 2D copy when there is corruption caused by concurrent ping-pong or scatter-gather operation. This would be most noticeable when 2D copy is used for moving a graphic image to a display but could cause problems in other use cases.
Workaround
Do not allow ping-pong or scatter-gather mode DMA transfers to occur concurrently with a 2D copy. If both types operations are required, interleave them such that the 2D copy is complete before enabling a channel in ping-pong or scatter-gather mode or vice versa.
Resolution
There is currently no resolution for this issue.

2.8 EMU_E107 — Interrupts During EM2 Entry

Description of Errata
An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag.
Affected Conditions / Impacts
During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0.
Workaround
Before entering EM2, disable all high frequency peripheral interrupts in the core.
Resolution
There is currently no resolution for this issue.

2.9 LCD_E103 — Indeterminate Animation Engine Start-Up

Description of Errata
The LCD controller animation engine starts counting based on when the writes to LCD_AREGA and LCD_AREGB occur in relation to the clock for the animation frame counter. Because the animation engine cannot know when the writes occur, it is not possible to know whether the A or B register will shift first, which can result in one of the registers shifting twice before the other shifts once.
Affected Conditions / Impacts
Animations that require specific sequencing may not start in the correct state such that frames are not displayed in the correct order.
Workaround
If animation sequences must be seen in a specific order, consider handling this in software instead of using the animation engine. If the purpose of the animation is to denote ongoing activity, use segments that can be cycled in a generic fashion such that the output achieves the desired effect without depending on a specific frame order.
Resolution
There is currently no resolution for this issue.

2.10 LCD_E104 — Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO

Description of Errata
A leakage path to IOVDD exists when the LCD controller is configured to use the internally boosted or external power supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is due to PMOS transistors in the LCD pin logic having their source/bulk terminals connected to the highest VDD (thus the LCD power supply when external/boost mode is used) while their gates are connected to IOVDD.
Affected Conditions / Impacts
Use of LCD pins for GPIO results in increased current draw when the LCD controller is configured to use the internally boosted or external supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is particularly noticeable when the device is operating in EM2 as the LCD to IOVDD supply leakage can amount to tens of microamps. While the GPIO functionality of the LCD pins is not impaired, for certain applications, the increased current draw can be undesirable.
Workaround
Do not use LCD pins for GPIO functionality if the LCD controller is configured to use an external power supply or boost mode, and the resulting VLCD can be greater than the IOVDD supply.
Resolution
There is currently no resolution for this issue.

2.11 LES_E104 — LFPRESC Can Extend Channel Start-Up Delay

Description of Errata
Setting LESENSE_TIMCTRL_LFPRESC to a value other than DIV1 may delay channel start-up longer than the number of $LFACLK_{LESENSE}$ clock cycles specified by LESENSE_TIMCTRL_STARTDLY.
Affected Conditions / Impacts
Delaying channel start-up delays the subsequent excitation and measurement phases and may have an impact on the data returned by the LESENSE.
Workaround
If a channel start-up delay is used (LESENSE_TIMCTRL_STARTDLY > 0), LESENSE_TIMCTRL_LFPRESC must be set to DIV1.
Resolution
There is currently no resolution for this issue.

2.12 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.13 PRS_E101 — Edge Detect on GPIO/ACMP

Description of Errata
Edge detect on peripherals with asynchronous edges might be missed.
Affected Conditions / Impacts
When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC, edges can be missed.
Workaround
Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC.
Resolution
There is currently no resolution for this issue.

2.14 TIMER_E102 — Timer Capture and Debugger

Description of Errata
Timer capture triggered when timer is halted by debugger.
Affected Conditions / Impacts
When DEBUGRUN is disabled and the capture input is HIGH, it is possible to wrongly trigger a capture event by halting the MCU and starting it again (for instance by setting a breakpoint).
Workaround
Enable DEBUGRUN when using a debugger.
Resolution
There is currently no resolution for this issue.

2.15 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e., ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

2.16 USART_E112 — USART AUTOTX Continues to Transmit Even With Full RX Buffer

Description of Errata
USART AUTOTX continues to transmit even with full RX buffer.
Affected Conditions / Impacts
When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.17 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

Description of Errata
If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled.
Affected Conditions / Impacts
It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0.
Workaround
Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data. If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART.
Resolution
There is currently no resolution for this issue.

2.18 WDOG_E103 — WDOG EM2 Detection with LFXO Digital/Sine Input

Description of Errata
The WDOG will mistake EM2 for EM3 if using LFXO with digital or sine input.
Affected Conditions / Impacts
When the WDOG is using LFXO with digital or sine input as a clock source, it will mistake EM2 for EM3. The EM2RUN and EM3RUN bits of WDOG_CTRL will behave accordingly.
Workaround
When using LFXO with digital/sine input, EM3RUN must be set to keep the WDOG running in EM2.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EFM32TG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 BOOT_E101 — Bootloader Pin Location

Description of Errata
A set of early EFM32TG108Fxx and EFM32TG110Fxx parts have wrong bootloader pin locations.
Affected Conditions / Impacts
On EFM32TG108Fxx parts with datecodes 1117 and 1120, and EFM32TG110Fxx parts with datecodes 1117 and 1120, the bootloader communication pins are located at pins D6 and D7. On newer EFM32TG108Fxx and EFM32TG110Fxx parts, these are located on pins F0 and F1 along with debug functionality.
Workaround
Do not use the D6 and D7 bootloader pins when designing for EFM32TG108Fxx and EFM32TG110Fxx.
Resolution
This issue is resolved in revision C devices.

3.2 CMU_E108 — LFxCLKEN Write

Description of Errata
First write to LFxCLKEN can be missed.
Affected Conditions / Impacts
For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN may cause the write to miss its effect.
Workaround
For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
Resolution
This issue is resolved in revision C devices.

3.3 CMU_E109 — LFXO Configuration Incorrect

Description of Errata
LFXO configuration incorrect.
Affected Conditions / Impacts
For devices with PROD_REV < 15, the default value for LFXOBOOST in CMU_CTRL is wrong.
Workaround
On devices with PROD_REV < 15, change LFXOBOOST to 0.
Resolution
This issue is resolved in revision C devices.

3.4 EMU_E105 — Debug Unavailable During DMA Processing from EM2

Description of Errata
The debugger cannot access the system processing DMA request from EM2.
Affected Conditions / Impacts
DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.
Workaround
Make sure DMA requests triggered from EM2 are handled.
Resolution
This issue is resolved in revision C devices.

3.5 GPIO_E101 — GPIO Wakeup from EM4

Description of Errata
On GPIO wakeup from EM4, all cause bits for high-polarity wakeup pins are set.
Affected Conditions / Impacts
All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup.
Workaround
Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup.
Resolution
This issue is resolved in revision C devices.

3.6 LES_E101 — LESENSE and Schmitt Trigger

Description of Errata
Schmitt trigger cannot be disabled on pins used for sensor excitation
Affected Conditions / Impacts
When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable amount of current.
Workaround
Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor.
Resolution
This issue is resolved in revision C devices.

3.7 LES_E102 — LESENSE and DAC CH1 Configuration

Description of Errata
LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.
Affected Conditions / Impacts
LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.
Workaround
Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1.
Resolution
This issue is resolved in revision C devices.

3.8 LES_E103 — AUXHFRCO and LESENSE

Description of Errata
LESENSE will not work properly at low AUXHFRCO frequencies.
Affected Conditions / Impacts
LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.
Workaround
Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
Resolution
This issue is resolved in revision C devices.

3.9 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

Description of Errata
Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset.
Affected Conditions / Impacts
The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7
Workaround
Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again.
Resolution
This issue is resolved in revision D devices.

3.10 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

Description of Errata
Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range.
Affected Conditions / Impacts
If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD
Workaround
Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again.
Resolution
This issue is resolved in revision D devices.

4. Revision History

Revision 1.50

March, 2021

- Added CMU_E115

Revision 1.40

November, 2019

- Updated to product revision D.
- Removed "Tiny" from front page.
- Added LES_E104.
- Resolved RMU_E102, and RMU_E103.
- Updated ADC_E118.
- Migrated to new errata document format.

Revision 1.30

January, 2019

- Added DMA_E102, LCD_E103, LCD_E104, RMU_E102, RMU_E103, and USART_E113.
- Removed CMU_E101, CMU_E102, EMU_E101, TIMER_E101, and USART_E101 from revision history. These errata have never been present on Tiny Gecko.

Revision 1.20

December, 2016

- Added ADC_E118.
- Updated errata formatting.
- Merged all errata documents for EFM32TG devices into one document.
- Merged errata history and errata into one document.

Revision 1.10

February, 2015

- Added DAC_E109, EMU_E107, PCNT_E102, and TIMER_E103.
- Updated link to errata for older revisions.
- Corrected typos.

Revision 1.00

August 21, 2013

- Added AES_E102.
- Updated disclaimer, trademark and contact information.

Revision 0.90

July, 2013

- Added DMA_E101.
- Updated errata naming convention.

Revision 0.80

November 26, 2012

- Removed errata no longer present on chip revision C — BOOT_E101, GPIO_E101, LES_E101, LES_E102 and LES_E103.
- Added AES_E101.

Revision 0.70

August 22, 2012

- Initial release for EFM32TG225 and EFM32TG825 BGA48 package devices.

April 24, 2012

- Added LES_E103.

Revision 0.60

January 20, 2012

- Added GPIO_E101.

Revision 0.50

January 13, 2012

- No longer applies. See above.

Revision 0.40

January, 2011

- No longer applies. See above.

Revision 0.30

November 11, 2011

- Added PRS_E101.

Revision 0.20

June, 2011

- Added BOOT_E101.

Revision 0.10

July 15, 2011

- Initial preliminary release for EFM32TG842 and EFM32TG232 devices.

May 20, 2011

- Initial preliminary release for EFM32TG108, EFM32TG110, EFM32TG210, EFM32TG222, EFM32TG230, EFM32TG822, and EFM32TG840 devices.

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