Wireless Gecko
EFR32BG27 Errata

This document contains information on the EFR32BG27 errata. The latest available revision of this device is revision B.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from the package marking or electronically.

Errata effective date: August, 2022.

1. Errata Summary

The table below lists all known errata for the EFR32BG27 and all unresolved errata of the EFR32BG27.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			A	B
DCDC_E303	DC-DC gets stuck in Boost Start-up mode after DVDD powered to 1.8V	Yes	X	—
EMU_E306	IOVDD Brown-Out Misdetection During Supply Ramp	Yes	X	X
IADC_E306	Changing Gain During a Scan Sequence Causes an Erroneous IADC Result	Yes	X	X
USART_E304	PRS Transmit Unavailable in Synchronous Secondary Mode	No	X	X

2. Current Errata Descriptions

2.1 EMU_E306 – IOVDD Brown-Out Misdetection During Supply Ramp

Description of Errata
The IOVDD brown-out detector incorrectly reports a valid operating level when the IOVDD supply begins ramping after DVDD has reached the mininum operating level and the device has been released from reset.
Affected Conditions / Impacts
Because the IOVDD supply is fully decoupled from the DVDD supply, it is permissible for the DVDD supply to lead the IOVDD supply and thus allow the CPU to exit reset and begin executing code before IOVDD has reached a suitable minimum operating voltage for external logic. In such a configuration, the IOVDD brown-out detector cannot be immediately relied upon to detect a valid operating level because it will inadvertently show that IOVDD is valid over a nominal range of 0.5 V to 0.7 V. The duration of this misdetection and the specific voltage range over which it occurs vary depending on the ramp rate of IOVDD. Variation is also observed from device to device and over temperature. For slower ramps, the duration is extended and the range adheres more closely to 0.5 V to 0.7 V. For faster ramps, the duration is reduced but the range over which the misdetection occurs can shift to higher voltages. The brown-out detector will settle and report correctly within 1 ms of IOVDD reaching its steady-state level.
Workaround
For a system that might be subject to this condition, select one of the following two workarounds: 1. Use a power supply configuration in which IOVDD is tied to or ramps concurrently with DVDD. 2. Characterize the system's IOVDD ramp time and implement a software delay with some headroom (e.g. via Sleeptimer and with the underlying hardware timer clocked from the LFRCO) that must first elapse to account for the misdetection period and before proceeding with the initialization of GPIO pins. **Note:** The IADC cannot be used to monitor the IOVDD ramp because its supply input multiplexer will not be powered until IOVDD reaches a valid operating level.
Resolution
There is currently no resolution for this issue.

2.2 IADC_E306 – Changing Gain During a Scan Sequence Causes an Erroneous IADC Result

Description of Errata
Differences in the ANALOGGAIN setting within multiple IADC_CFGx groups during a scan sequence introduces a transient condition that may result in an inaccurate IADC conversion.
Affected Conditions / Impacts
The result of the IADC scan measurement may not match the expected result for the voltage present on the pin during the conversion.
Workaround
Both 1 and 2 shown below must be implemented. 1. If there is a difference in the ANALOGGAIN setting between IADC_CFGx groups during a scan sequence, the IADC_SCHEDx clock prescaler must also change to an appropriate setting. This forces a warmup state (5 µs delay) in between ANALOGGAIN changes. Note that the same IADC_SCHEDx clock prescaler value may be an appropriate setting for both ANALOGGAIN settings, but to force the warmup delay, the IADC_SCHEDx must have different values. 2. The first and last entry of a scan group should use IADC_CFG0, which is the default configuration of the IADC at the start and end of a scan conversion sequence. If CONFIG1 is used at the start and end of the scan group, erronous IADC results may occur.
Resolution
There is currently no resolution for this issue.

2.3 USART_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

Description of Errata
When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).
Affected Conditions / Impacts
Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO_USARTn_RXROUTE and GPIO_USARTn_TXROUTE registers are used.
Workaround
There is currently no workaround for this issue.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EFR32BG27 devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 DCDC_E303 – DC-DC gets stuck in Boost Start-up mode after DVDD powered to 1.8V

Description of Errata
The boost DC-DC will get stuck in Boost Start-up mode when the VBAT rail drops below the VBAT POR threshold (approximately 0.6V) after DVDD is powered up to 1.8V.
Affected Conditions / Impacts
When the boost DC-DC gets stuck in Boost Start-up mode, the DVDD supply would be regulated at approximately 2.4V instead of 1.8V, supporting only 3mA load instead of 25mA.
Workaround
When the boost DC-DC is stuck in Boost Start-up mode, perform the steps below to resume normal operation: 1. Shutdown the boost DC-DC by clearing EMU_BOOSTCTRL.BOOSTENCTRL to 0x0 and toggle the BOOST_EN pin from logic '1' to logic '0', this will bring the DC-DC into shutdown boost mode 2. Toggle the BOOST_EN pin from logic '0' to logic '1', this will power back up the DC-DC
Resolution
This issue is resolved on revision B devices.

4. Revision History

Revision 0.2

August, 2022

- Updated for device revision B.
- Added DCDC_E303.

Revision 0.1

May, 2022

- Initial release.

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