

### Analog Peripherals

- **8-Bit ADC**
  - Up to 500 ksp/s
  - Up to 8 external inputs
  - Programmable amplifier gains of 4, 2, 1, & 0.5
  - VREF from external pin or V<sub>DD</sub>
  - Built-in temperature sensor
  - External conversion start input
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (<0.5 μA)

### On-chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

### Supply Voltage 2.7 to 3.6 V

- Typical operating current: 6.6 mA @ 25 MHz;  
14 μA @ 32 kHz
- Typical stop mode current: 0.1 μA
- Temperature range: -40 to +85 °C

### Full Technical Data Sheet

- C8051F300/1/2/3/4/5

### High Speed 8051 μC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

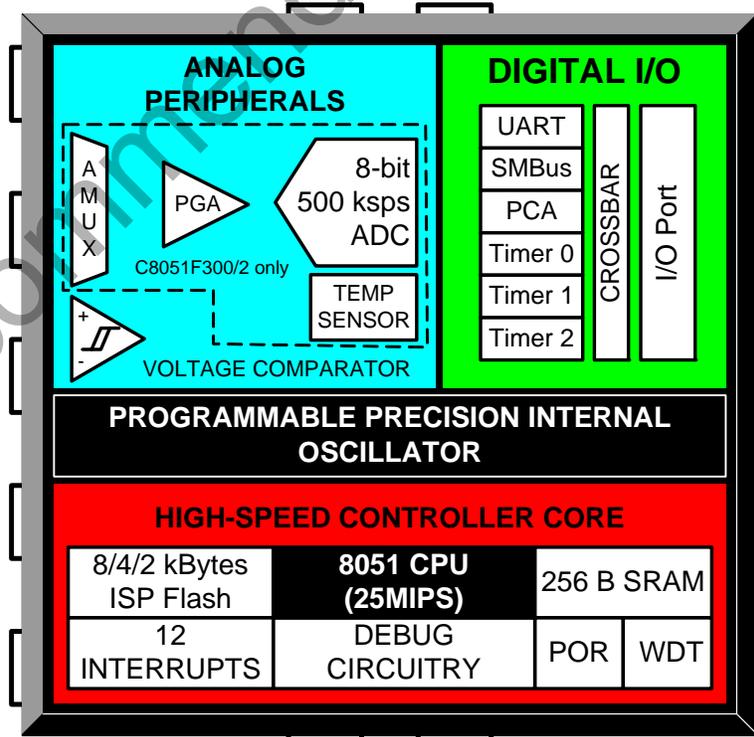
- 256 bytes internal data RAM
- 8 kB Flash; 512 bytes are reserved in the 8 kB devices

### Digital Peripherals

- 8 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general-purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with three capture/compare modules
- Real time clock mode using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz with ±2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; Useful in power saving modes



# C8051F300-GDI

## 1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)*	RAM (Bytes)	SMBus/I <sup>2</sup> C	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	8-bit 500 ksps ADC	Programmable Current Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F300-GDI	25	8	256	1	1	3	✓	8	✓	✓	✓	1	✓	Tested Die in Wafer Form

\*Note: 512 bytes reserved for factory use.

## 2. Pin Definitions

**Table 2.1. Pin Definitions for the C8051F300-GDI**

Name	Physical Pad Number	Type	Description
VREF / P0.0	3	A In D I/O or A In	External Voltage Reference Input. Port 0.0.
P0.1	4	D I/O or A In	Port 0.1.
V <sub>DD</sub>	5		Power Supply Voltage.
XTAL1 / P0.2	6	A In D I/O or A In	Crystal Input. This pin is the external oscillator circuit return for a crystal or ceramic resonator. Port 0.2.
XTAL2 / P0.3	7	A Out D I/O	Crystal Input/Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC network configurations. Port 0.3.
P0.4	13	D I/O or A In	Port 0.4.
P0.5	14	D I/O or A In	Port 0.5.
C2CK /  RST	15	D I/O D I/O	Clock signal for the C2 Development Interface. Device Reset. Open-drain output of internal POR or V <sub>DD</sub> monitor. An external source can initiate a system reset by driving this pin low for at least 10 $\mu$ s.
P0.6 / CNVSTR	16	D I/O or A In D I/O	Port 0.6. ADC External Convert Start Input Strobe.
C2D / P0.7	17	D I/O D I/O or A In	Data signal for the C2 Development Interface. Port 0.7.
GND	18		Ground.

# C8051F300-GDI

## 3. Bonding Instructions

Table 3.1. C8051F300-GDI Pad Connections

Physical Pad Number	Example Package Pin Number (11-QFN)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	Reserved*		-1001.5	-575
2	Reserved*		-926.5	-575
3	1	VREF/P0.0	-795.5	-575
4	2	P0.1	-615.5	-575
5	3	VDD	346.17	-575
6	4	XTAL1/P0.2	615.5	-575
7	5	XTAL2/P0.3	795.5	-575
8	Reserved*		926.5	-575
9	Reserved*		1001.5	-575
10	Reserved*		1000	-429.57
11	Reserved*		1001.5	575
12	Reserved*		926.5	575
13	6	P0.4	790.5	575
14	7	P0.5	620.5	575
15	8	/RST/C2CK	440.5	575
16	9	P0.6/CNVSTR	-523.5	575
17	10	C2D/P0.7	-703.5	575
18	11	GND	-834.5	575
19	Reserved*		-926.5	575
20	Reserved*		-1001.5	575

**\*Note:** Pins marked "Reserved" should not be connected.

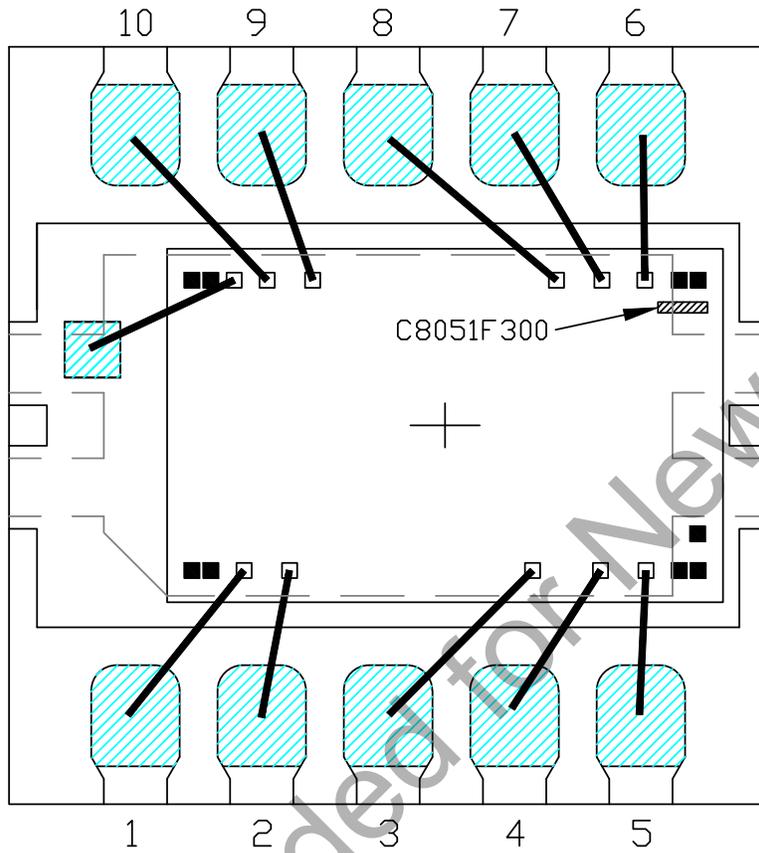


Figure 3.1. Example Die Bonding (QFN-11)

# C8051F300-GDI

Table 3.2. Wafer and Die Information

Wafer ID	C8051F300
Wafer Dimensions	8 in
Die Dimensions	1.40 mm x 2.2 mm
Wafer Thickness	12 mil $\pm$ 1 mil
Wafer Identification	Notch
Scribe Line Width	80 $\mu$ m
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 $\mu$ m x 60 $\mu$ m
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 $\mu$ m
<b>*Note:</b> This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

## 4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

Not Recommended for New Designs

# C8051F300-GDI

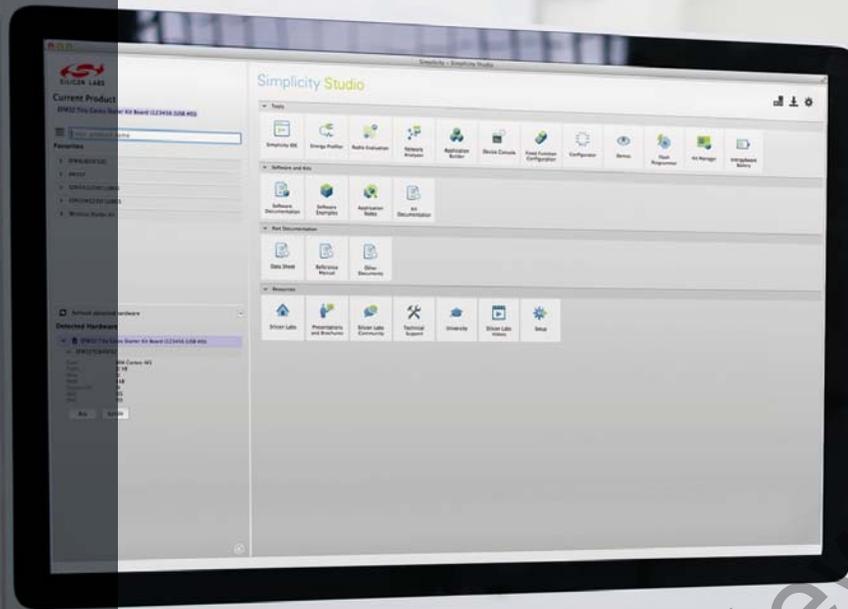
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## DOCUMENT CHANGE LIST

### Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 6.

Not Recommended for New Designs



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