Si4707-B20

WEATHER BAND AND SAME DATA RECEIVER

Features

- Weather band support (162.4–162.55 MHz)
- SAME processor
  - Excellent SAME sensitivity
  - Byte-wise data quality metrics
  - Advanced error correction
- 1050 Hz alert tone detection
- Excellent real-world performance
- Freq synthesizer with integrated VCO
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Adaptive noise suppression
- WB digital tuning
- Low-IF direct conversion with no external ceramic filters
- Programmable reference clock
- Volume control
- Receive signal quality indicators (RSSI and SNR)
- 2-wire and 3-wire control interface
- Integrated LDO regulator
- 2.7 to 5.5 V supply voltage
- Firmware upgradeable
- 3 x 3 x 0.55 mm 20-pin QFN package
  - Pb-free/RoHS compliant

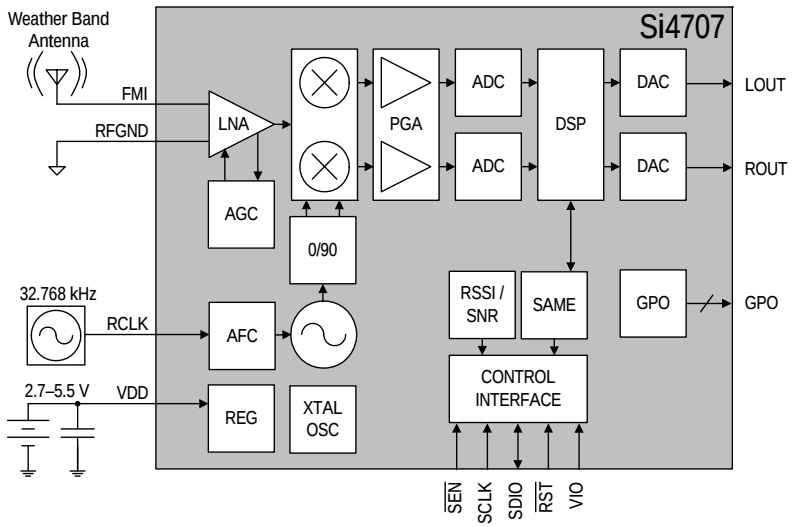
Applications

- Emergency radios
- Table and portable radios
- Stereos
- Mini/micro systems
- Portable media players
- Boom boxes
- Cellular handsets
- Modules
- Clock radios
- Mini HiFi

Description

The Si4707 is the first digital CMOS weather band and SAME decoder receiver IC to integrate the complete tuner and decoder functionality from antenna input to audio and/or data output.

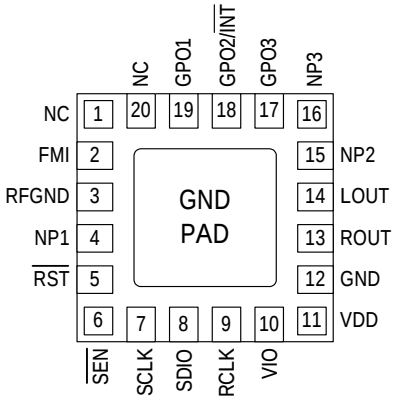
Functional Block Diagram



Ordering Information:
See page 22.

Pin Assignments

Si4707-B20-GM
(Top View)



Patents pending

Notes:

1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place Si4707 as close as possible to antenna jack and keep the FMI traces as short as possible.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (VIO + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4707 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI.

Table 3. DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{FM}		—	19.1	23	mA
Interface Supply Current	I_{IO}		—	320	600	µA
V_{DD} Powerdown Current[1]	I_{DDPD}		—	10	20	µA
V_{IO} Powerdown Current[1]	I_{IOPD}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[2]	V_{IH}		0.7 x VIO	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 x VIO	V
High Level Input Current[2]	I_{IH}	V_{IN} = VIO = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OUT} = 500 µA	0.8 x VIO	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x VIO	V

Notes:

1. Specifications are guaranteed by characterization.
2. For input pins SCLK, SEN, SDIO, RST, and RCLK.
3. For output pins SDIO, GPO1, GPO2, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow$[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

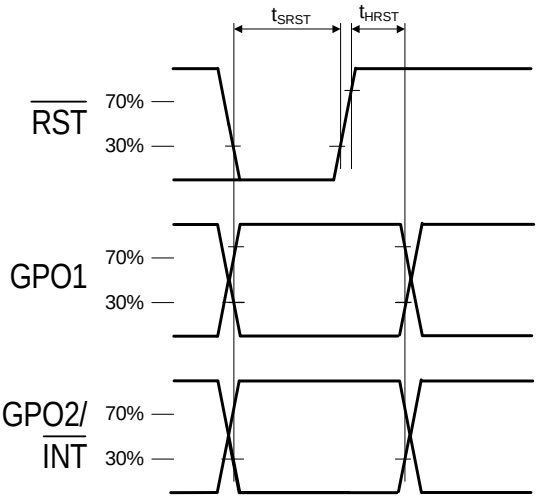


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4707 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

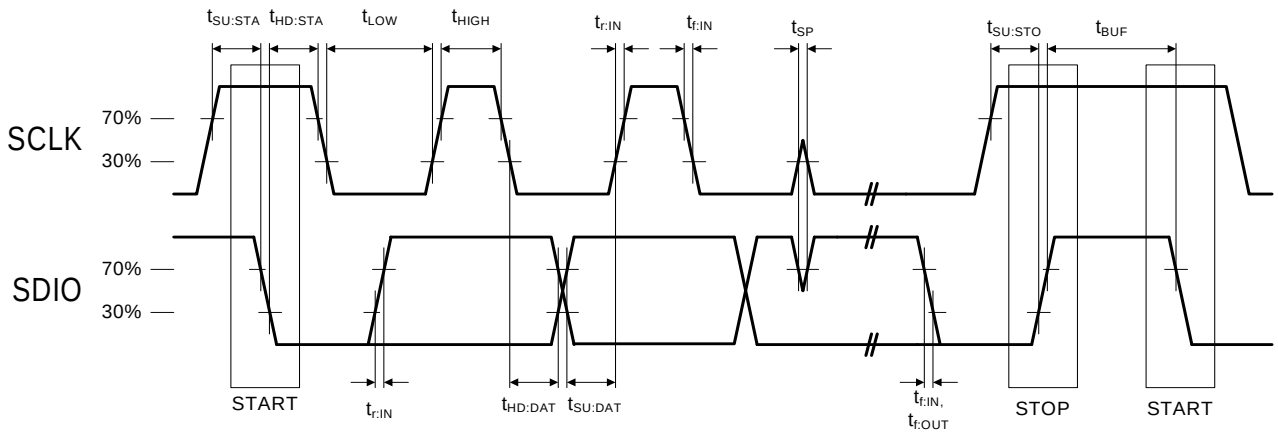


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

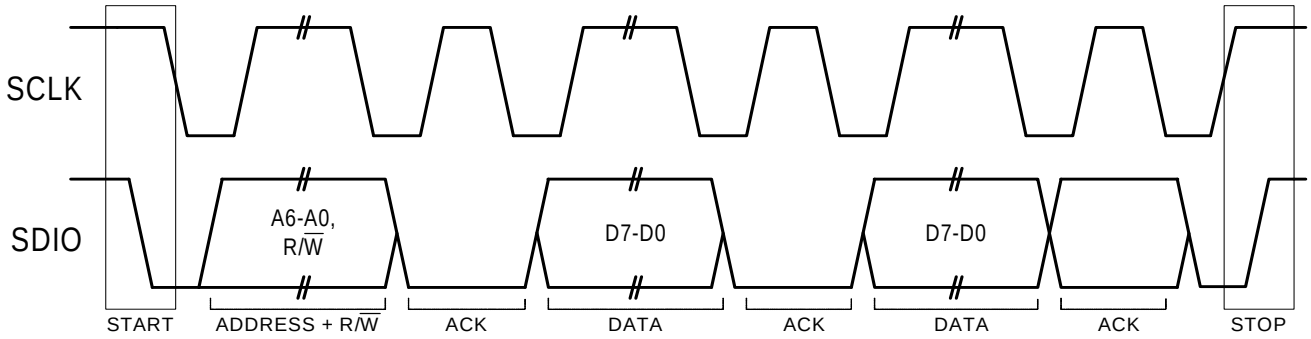


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

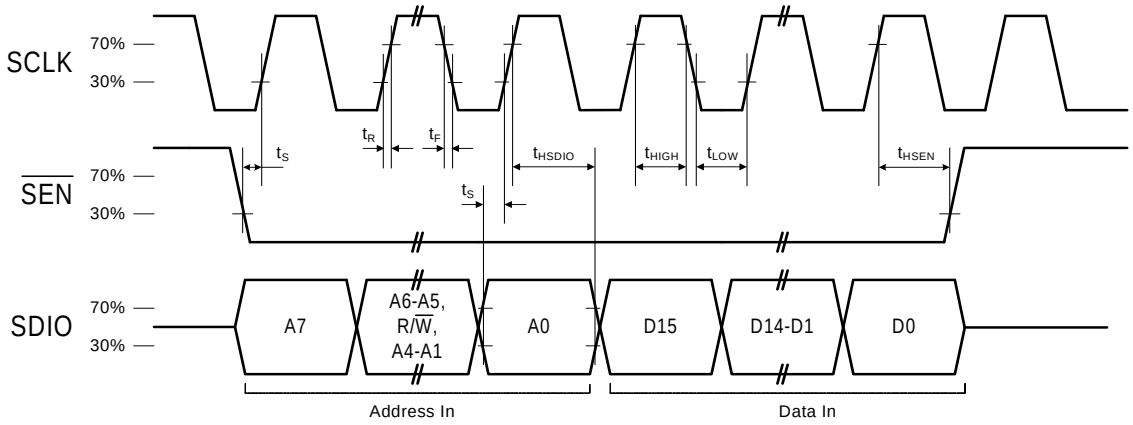


Figure 4. 3-Wire Control Interface Write Timing Parameters

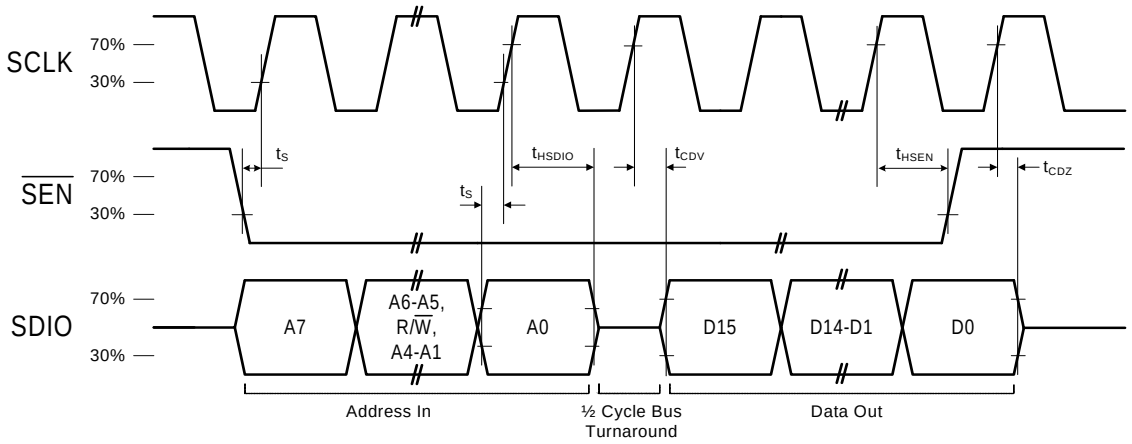


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

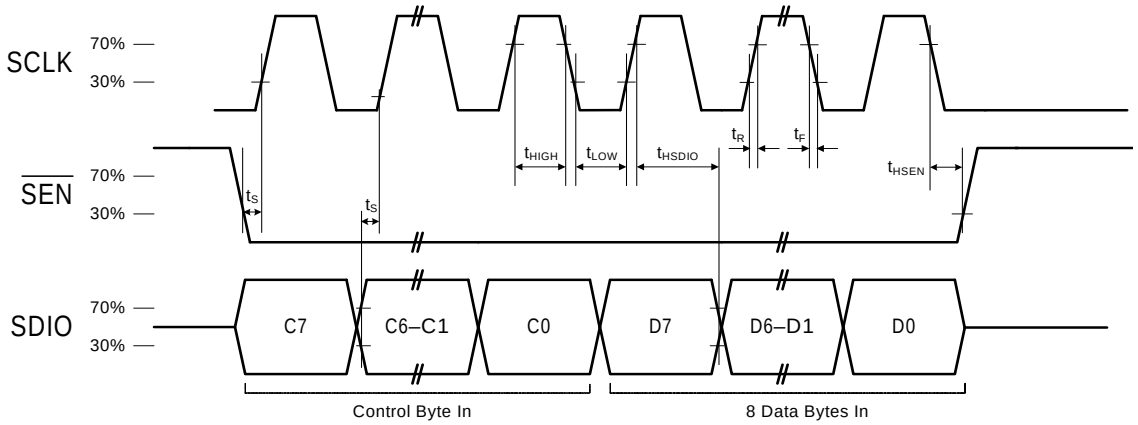


Figure 6. SPI Control Interface Write Timing Parameters

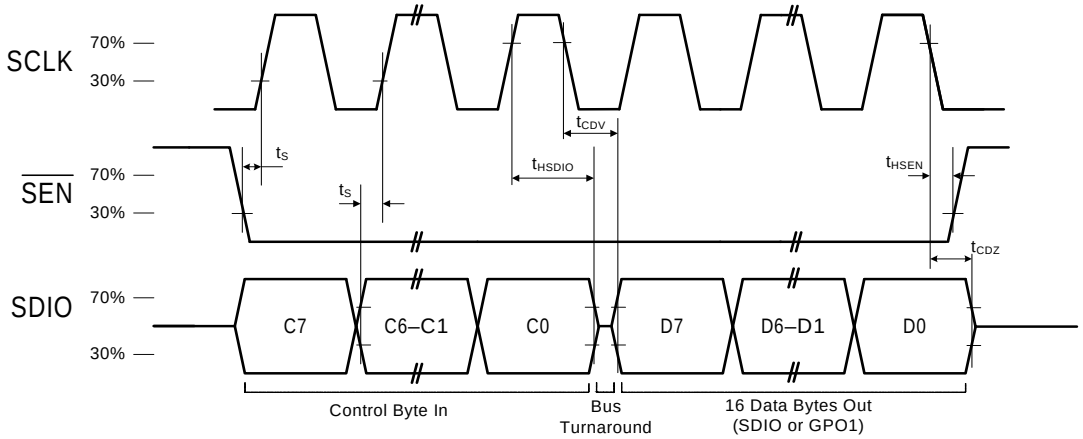


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. WB Receiver Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_R		162.4	—	162.55	MHz
Sensitivity[2,3,4]		SINAD = 12 dB	—	0.45	—	µV EMF
Adjacent Channel Selectivity		±25 kHz	—	55	—	dB
Audio S/N[2,3,4,5]			—	45	—	dB
Audio Frequency Reponse Low		–3 dB	—	—	300	Hz
Audio Frequency Reponse High		–3 dB	3	—	—	kHz
AFSK Trip Sensitivity[6]		100% of message correctly received	—	0.45	—	µV EMF

Notes:

1. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. F_{MOD} = 1 kHz.
3. Δf = 3 kHz.
4. B_{AF} = 300 Hz to 15 kHz, A-weighted.
5. V_{EMF} = 1 mV.
6. Δf = 4 kHz.

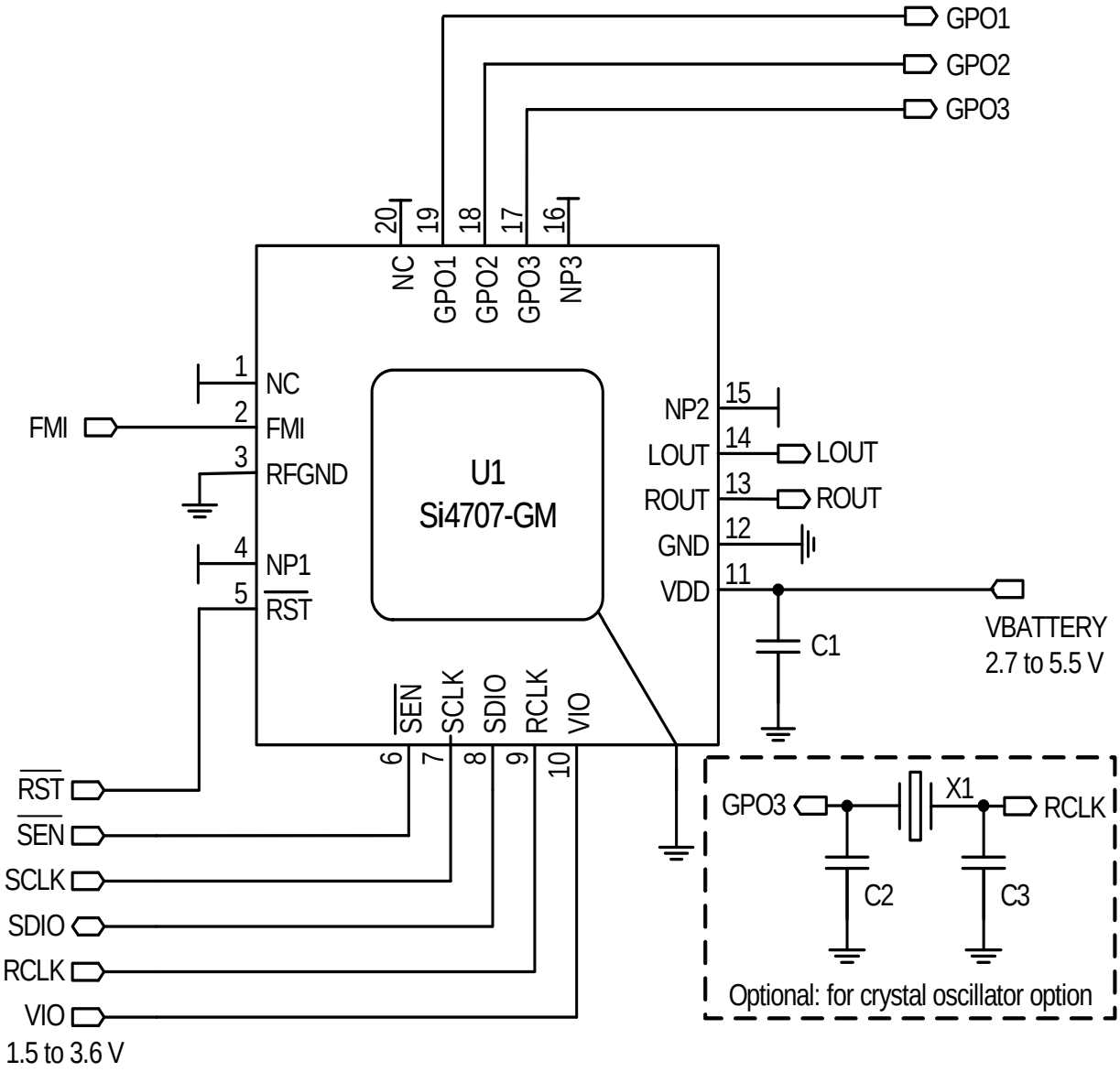
Table 9. Reference Clock and Crystal Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequency*			31.130	32.768	40,000.0	kHz
RCLK Frequency Tolerance			–50	—	50	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance			–50	—	50	ppm
Board Capacitance			—	—	3.5	pF

***Note:** The Si4707 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See AN332, Table 6 for more details.

2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. Pins 4, 15, and 16 are unused; recommend connecting to ground.
5. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
6. Pin 2 connects to the WB antenna interface.
7. Place Si4707 as close as possible to antenna jack and keep the FMI trace as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4707 WB + SAME Receiver	Silicon Laboratories
Optional Components		
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson

4. Functional Description

4.1. Overview

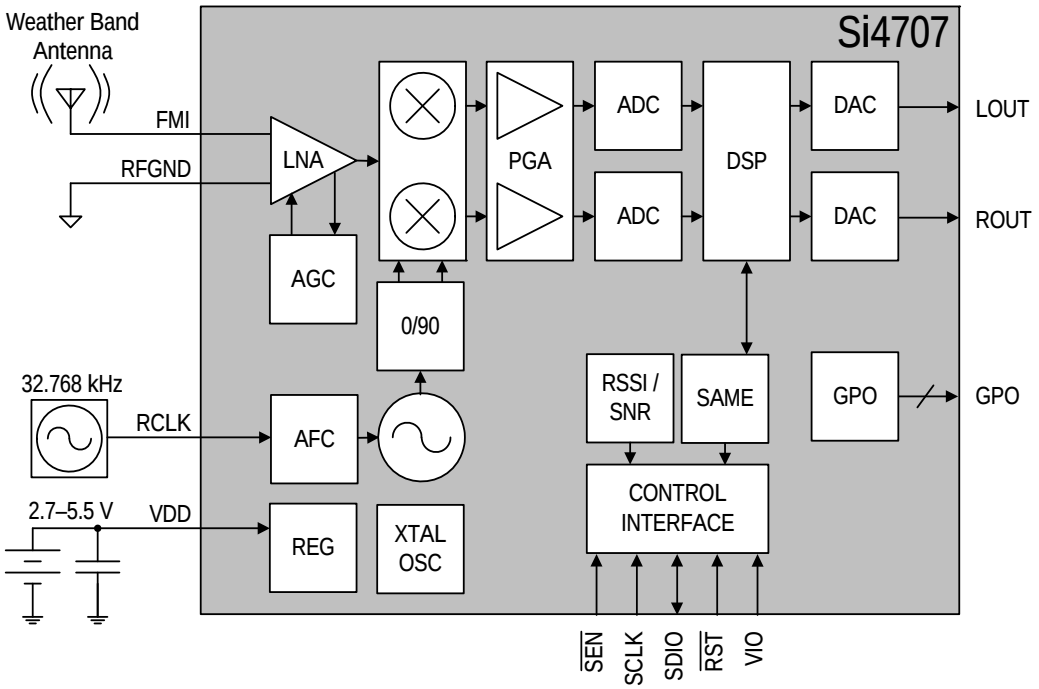


Figure 8. Functional Block Diagram

The Si4707 is the industry's first weather band (WB) radio receiver IC to include a specific area message encoding (SAME) processor. Offering unmatched integration and PCB space savings, the Si4707 requires only one external component and less than 15 mm^2 of board area. Available in a tiny 3 x 3 mm QFN package, it eliminates the need for a front-end tuner IC, external ADC, DSP processor, RAM, and numerous discrete components found in traditional SAME weather band radios. The Si4707 weather band receiver provides the space savings and low power consumption necessary for portable devices while delivering the high performance and design simplicity desired for all weather alert radios.

Leveraging Silicon Laboratories' proven and patented Si4700/01 FM tuner's digital low intermediate frequency (low-IF) receiver architecture, the Si4707 delivers superior RF performance combined with sophisticated digital processing to yield best-in-class audio quality and SAME data sensitivity.

The high integration and complete system production test simplifies design in, increases system quality, and improves manufacturability.

The Si4707 is a feature-rich solution including 1050 Hz tone detection, automatic frequency control, dynamic channel bandwidth filters, and digital tuning. In addition, the Si4707 provides a programmable reference clock and supports an I^2C compatible 2-wire control interface, SPI, and a Si4700/01 backwards compatible 3-wire control interface.

The Si4707 incorporates a digital processor to provide SAME data, advance error correction, and SAME data quality metrics. Using this feature, the Si4707 enables broadcast alert data such as severe thunderstorm warning or flash flood watch to be displayed to the user.

4.2. Block Diagram Description

The Si4707 IC integrates the voltage-controlled oscillator (VCO) and frequency synthesizer and accepts a wide-range of programmable reference clocks (RCLK). The IC also supports a dedicated external crystal with an integrated crystal oscillator. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the RCLK and adjusted with an automatic frequency control (AFC) servo loop during reception. The VCO frequency is modified according to the target frequency and varies according to the tuned channel.

The Si4707 uses a digital low-IF architecture, integrating the entire analog receive chain for WB. The IC also integrates the functionality of most external components typically found in competing solutions and performs all processing in an on-chip digital signal processor (DSP) and microcontroller (MCU) core. The analog chain includes a dedicated low-noise amplifier (LNA), automatic gain control (AGC), image-reject quadrature mixer, programmable gain amplifier (PGA), and a set of delta-sigma high-performance ADCs. The LNA block receives wide-band frequency input at the FMI input pin. The on-chip resistor blocks control the gain of the external WB antenna network. The LNA gain is dynamically controlled by the AGC loop, contingent on the RF peak detectors and signal strength. The receive path continues to dedicated quadrature mixers that downconvert the received signal from RF to low-IF, filter for out-of-band interferers, and perform a transfer function to shift the tuned frequency to DC. A single pair of PGAs filters the multiplexed (MPX) mixer output from interferers and amplifies the signal again before delivering it to two high-resolution analog-to-digital converters (ADC). The digital core performs channel selection and filtering, digital calibrated tuning, FM demodulation, and SAME demodulation/decoding. The core also performs signal quality processing including received signal strength indicators (RSSI) and SNR.

4.3. Weather Band Receiver

The Si4707 supports weather band reception from 162.4 to 162.55 MHz. The highly-integrated Si4707 meets NOAA and Weather Radio Canada specifications, receives all seven specified frequencies, implements narrow-band FM de-emphasis, and supports 1050 Hz alert tone detection. In addition, the Si4707 provides advanced features not available on conventional radios, such as an AFC, a dynamic channel bandwidth filter, and RSSI and SNR receive signal quality indicators.

The AFC locks on to the strongest signal within a narrow, adjustable frequency range to compensate for any potential frequency errors such as crystal tolerance or transmit frequency errors. The AFC ensures the channel filter is always centered on the desired channel providing optimal reception. The dynamic channel bandwidth feature utilizes a wide filter in strong signal conditions to provide best sound quality and a narrower filter in weak conditions to provide best sensitivity.

4.4. DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. Weather band stations broadcast in mono only, so LOUT and ROUT audio will be the same. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

4.5. SAME Processor

The Si4707 implements a high-performance SAME processor for demodulation, byte-wise data quality metrics, and advanced error correction beyond the commonly used polling method. The SAME decoder draws on soft decision decoding techniques to provide robust performance and delivers reception in environments where signal power is very low or compromised.

The Si4707 device stores the entire SAME message and provides a user programmable interrupt at the end of message detected, start of message detected, preamble detected, and/or header buffer ready. It also reports on the confidence level of each byte of data with a value of 0–3, with 3 representing the highest confidence level. This feature, unique to the Si4707, provides extra visibility into the message accuracy, which helps limit the number of false messages in poor reception areas.

4.6. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology, including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an AFC servo loop during reception. The tuning frequency can be directly programmed using the WB_TUNE_FREQ.

4.7. Reference Clock

The Si4707 reference clock is programmable, supporting RCLK frequencies in Table 9. Refer to Table 3, "DC Characteristics," on page 5 for switching voltage levels and Table 8, "WB Receiver Characteristics[1]," on page 11 for frequency tolerance information. Using RCLK is the recommended method in order to meet the ±50 ppm requirement.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 12. This mode is enabled using the POWER_UP command, see Table 11, "Si4707 Command Summary," on page 19.

The Si4707 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4707 is performing the tune function, the crystal oscillator may experience jitter, which may result in lower SNR.

4.8. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4707 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4707 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor, which is connected while RST is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins that differ from these states. See Table 10.

Table 10. Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of RST, the pins GPO1 and GPO2 are used as general purpose output (O) pins as described in Section "4.9. GPO Outputs". In any bus mode, commands may only be sent after VIO and VDD supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.8.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4707 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4707 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4707 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to eight data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4707 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4707.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

4.8.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 3-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4707 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

4.8.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives one additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).

- 0xA0 = read a response (device drives one additional byte on GPO1).
- 0xE0 = read a response (device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly eight data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly one byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep $\overline{SEN}$ low until all bytes have transferred. A transaction may be aborted at any time by setting $\overline{SEN}$ high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

4.9. GPO Outputs

The Si4707 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high impedance. The GPO pins can be reconfigured as specialized functions. GPO2/INT can be configured to provide interrupts and GPO3 can be configured to provide external crystal support.

4.10. Firmware Upgrades

The Si4707 contains on-chip program RAM to accommodate minor changes to the firmware. This allows Silicon Laboratories to provide future firmware updates to optimize the characteristics of new radio designs and those already deployed in the field.

4.11. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

4.12. Programming with Commands

To ease development time and offer maximum customization, the Si4707 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties and responses.

To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command. A complete list of commands is available in Table 11, “Si4707 Command Summary,” on page 19.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. A complete list of properties is available in Table 12, “Si4707 Property Summary,” on page 20.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a one-byte status update, which indicates interrupt and clear-to-send status information. For a detailed description of the commands and properties for the Si4707, see “AN332: Si47xxProgramming Guide.”

5. Commands and Properties

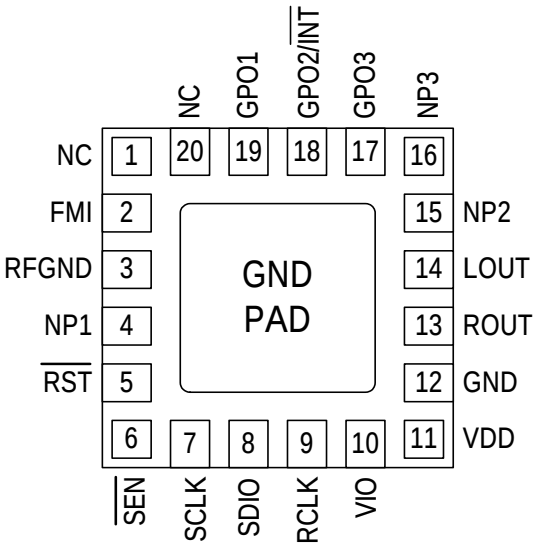
Table 11. Si4707 Command Summary

Cmd	Name	Description
0x01	POWER_UP	Powerup device.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Powerdown device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Read interrupt status bits.
0x15	PATCH_ARGS	Reserved command used for firmware file downloads.
0x16	PATCH_DATA	Reserved command used for firmware file downloads.
0x50	WB_TUNE_FREQ	Selects the WB tuning frequency.
0x52	WB_TUNE_STATUS	Queries the status of the previous WB_TUNE_FREQ command.
0x53	WB_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.
0x54	WB_SAME_STATUS	Returns SAME information for the current channel.
0x55	WB_ASQ_STATUS	Queries the status of the 1050 Hz alert tone.
0x57	WB_AGC_STATUS	Queries the status of the AGC.
0x58	WB_AGC_OVERRIDE	Enable or disable the WB AGC.
0x80	GPO_CTL	Configures GPO3 as output or Hi-Z.
0X81	GPO_SET	Sets GPO3 output level (low or high).

Table 12. Si4707 Property Summary

Prop	Name	Description	Default
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently in FM mode.	0x0000
0x5108	WB_MAX_TUNE_ERROR	Maximum change in frequencies from the WB_TUNE_FREQ to which the AFC will lock.	0x000F
0x5200	WB_RSQ_INTERRUPT_SOURCE	Configures interrupts related to RSQ metrics. All interrupts are disabled by default.	0x0000
0x5201	WB_RSQ_SNR_HIGH_THRESHOLD	Sets high threshold for SNR interrupt. The default is 0 dB.	0x007F
0x5202	WB_RSQ_SNR_LOW_THRESHOLD	Sets low threshold for SNR interrupt. The default is 0 dB.	0x0000
0x5203	WB_RSQ_RSSI_HIGH_THRESHOLD	Sets high threshold for RSSI interrupt. The default is 0 dB.	0x007F
0x5204	WB_RSQ_RSSI_LOW_THRESHOLD	Sets low threshold for RSSI interrupt. The default is 0 dB.	0x0000
0x5600	WB_ASQ_INTERRUPT_SOURCE	Configures 1050 Hz alert tone interrupts. All interrupts are disabled by default.	0x0000
0x5500	WB_SAME_INTERRUPT_SOURCE	Configures SAME interrupt sources. All interrupts are disabled by default.	0x0000

6. Pin Descriptions: Si4707-B20



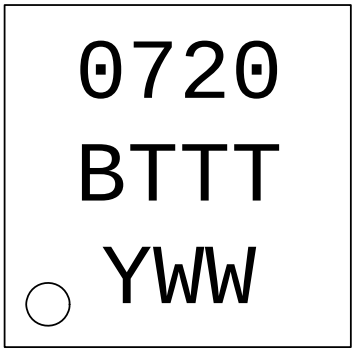
Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	WB RF input. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	NP1	Unused. Recommend connect to ground.
5	$\overline{\text{RST}}$	Device reset (active low) input.
6	$\overline{\text{SEN}}$	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	VIO	I/O supply voltage.
11	V_{DD}	Supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT	Right audio line output in analog.
14	LOUT	Left audio line output in analog.
15	NP2	Unused. Recommend connect to ground.
16	NP3	Unused. Recommend connect to ground.
17	GPO3	General purpose output or crystal oscillator.
18	GPO2/$\overline{\text{INT}}$	General purpose output or interrupt pin.
19	GPO1	General purpose output.

7. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4707-B20-GM	WB Radio and SAME Receiver	QFN Pb-free	–20 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

8. Package Markings (Top Marks)

8.1. Top Mark



8.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	07= Si4707
	Firmware Revision	20 = Firmware Revision 2.0
Line 2 Marking:	Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

9. Package Outline: Si4707 QFN

Figure 9 illustrates the package details for the Si4707. Table 13 lists the values for the dimensions shown in the illustration.

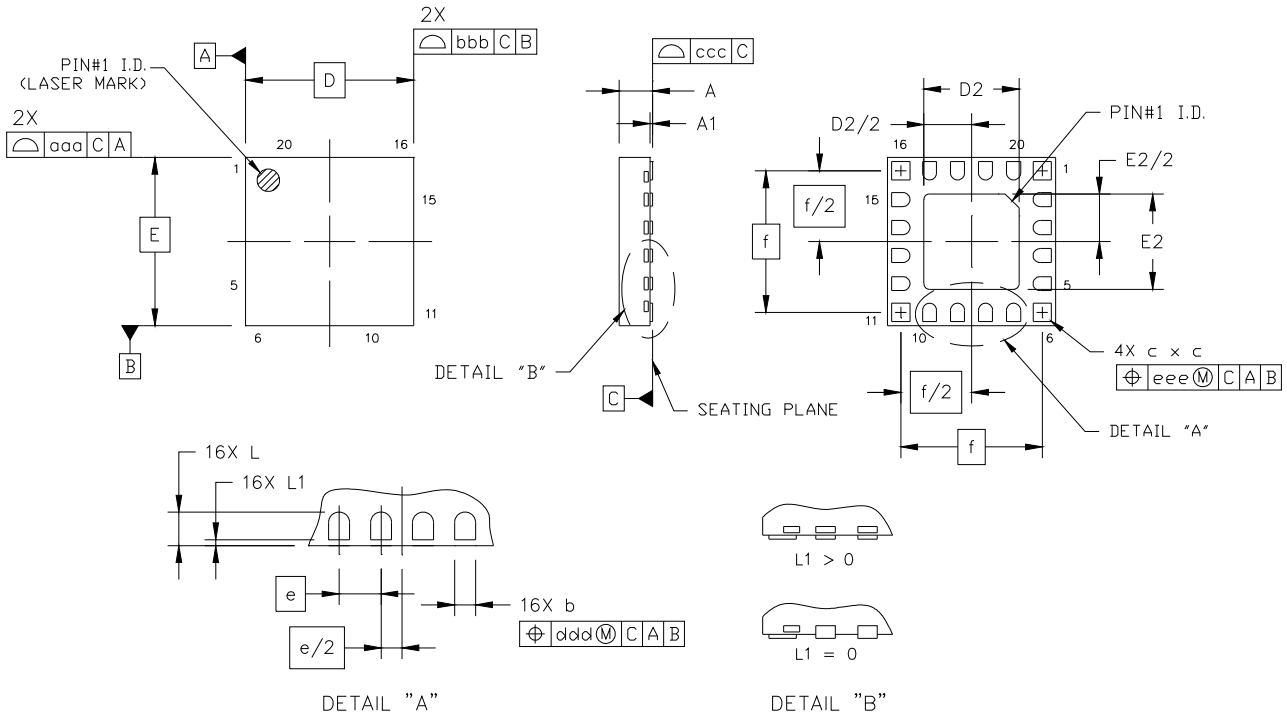


Figure 9. 20-Pin Quad Flat No-Lead (QFN)

Table 13. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

10. PCB Land Pattern: Si4707 QFN

Figure 10 illustrates the PCB land pattern details for the Si4707-GM. Table 14 lists the values for the dimensions shown in the illustration.

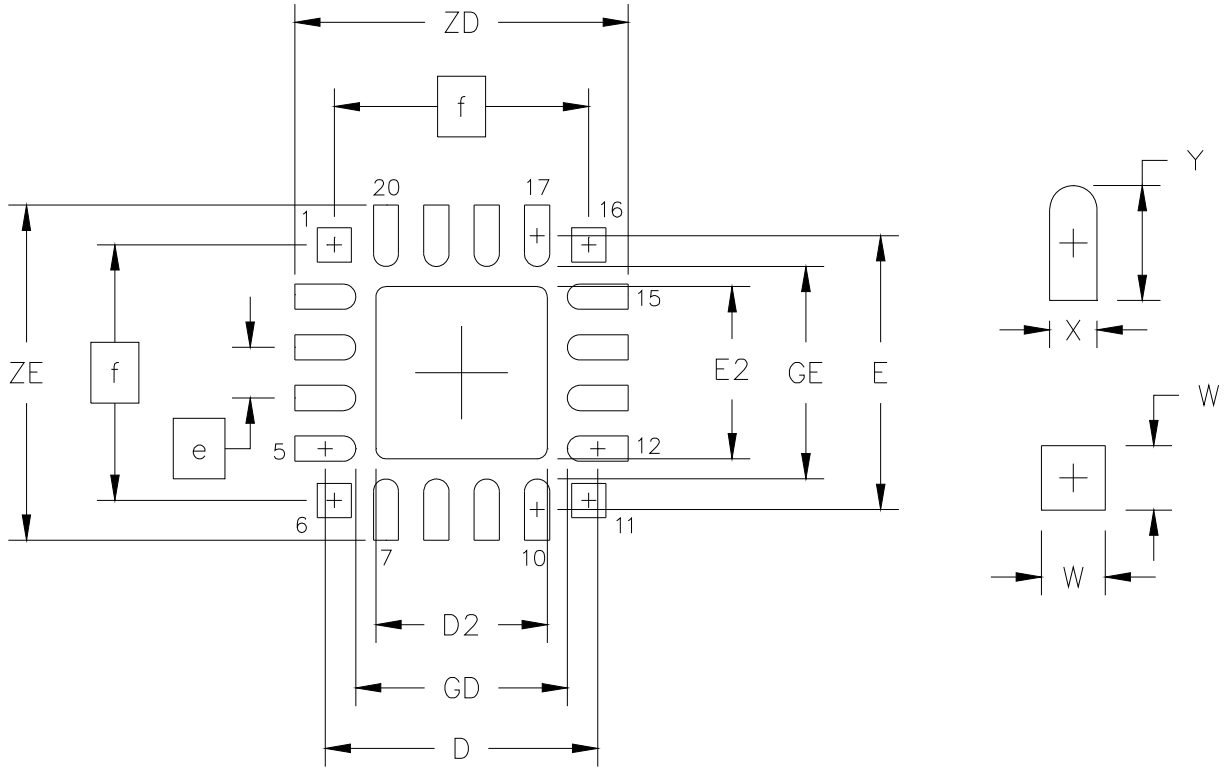


Figure 10. PCB Land Pattern

Table 14. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. Additional Reference Resources

- AN332: Si47xx Programming Guide
- AN383:Si47xx Antenna, Schematic, Layout, and Design Guidelines
- AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure
- AN344: Si4706/07/4x Programming Guide
- Si47xx Customer Support Site: http://www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, register at http://www.mysilabs.com and send user's first and last name, company, NDA reference number, and mysilabs user name to fminfo@silabs.com. Silicon Labs recommends an all lower case user name.

Document Change List

Revision 0.1 to Revision 0.8

- Updated Table 5, “2-Wire Control Interface Characteristics[1,2,3],” on page 7.
- Updated Table 8, “WB Receiver Characteristics[1],” on page 11.
- Updated Table 11, “Si4707 Command Summary,” on page 19.
- Updated the title of AN383 to ”Si47xx Antenna, Schematic, Layout, and Design Guidelines.”

NOTES:

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