EFR32ZG14 Z-Wave 700 调制解调器 SoC 数据表

Silicon Labs Z-Wave 700 调制解调器 SoC EFR32ZG14 是一款适用于智能家居应用中的网关和控制器的理想解决方案，这些应用包括智能家居网关、智能扬声器、机顶盒、U 盘等等。

这款单芯片解决方案采用行业领先的低功耗 Gecko 技术。EFR32ZG14 具有卓越的无线电灵敏度，有助于扩大 Z-Wave 网状网络的范围。

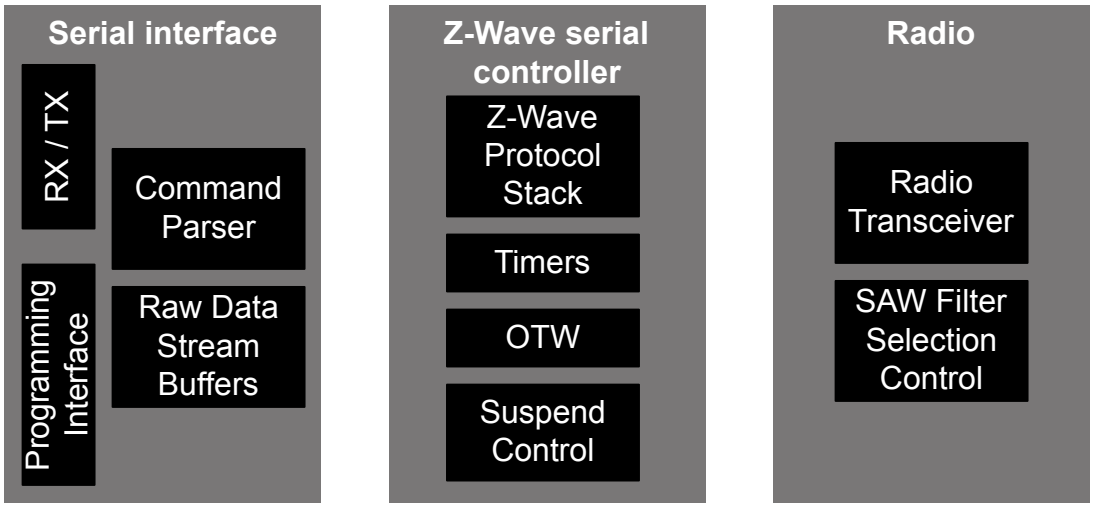
EFR32ZG14 应用包括适用于以下应用的 Z-Wave 控制器和网关：

- 智能家居
- 安全
- 照明
- 健康和保健
- 测量
- 楼宇自动化

该调制解调器 SoC 元件仅适用于 Z-Wave 控制器和网关，不能用于终端设备。

主要特点

- TX 功率高达 13 dBm
- 100 kbps 条件下，RX 灵敏度为 -98.8 dBm
- 32 位 ARM® Cortex®-M4（内核为 39 MHz）



1. 功能列表

EFR32ZG14 的重要功能如下所列。

- **低功耗无线片上系统**。
  - 高性能 32 位 39 MHz ARM Cortex®-M4，带有 DSP 指令和浮点单元，可实现高效的信号处理
  - 1 GHz 以下无线电操作
  - 发射功率：高达 13 dBm
- **低功耗**
  - 10.5 mA 有效无线电 RX 电流
  - 10.5 mA 空闲/监听无线电 RX 电流
  - 38.8 mA 有效无线电 TX 电流（13 dBm 输出功率）
  - 12.9 mA 有效无线电 TX 电流（0 dBm 输出功率）
  - 在低功耗挂起模式中兼容 USB
- **高接收器性能**
  - 在 100 kbit/s GFSK、868 MHz 的条件下，灵敏度为 -98.6 dBm
  - 在 100 kbit/s GFSK、915 MHz 的条件下，灵敏度为 -98.8 dBm
- **支持的调制格式**
  - 2/4 (G)FSK，可配置完整波形
- **支持的协议：**
  - Z-Wave
- **广泛的 MCU 外围设备选择**
  - 5 个专用 GPIO，支持 UART 通信、挂起模式操作和可选的 SAW 滤波选择器
  - 内置电源监控
  - UART 串联接口
- **宽操作范围**
  - 1.8 至 3.8 V 单电源，支持集成 DC-DC
  - -40 °C 至 85 °C
- **QFN32 5x5 mm 封装**

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package
EFR32ZG14P231F256GM32-B	Z-Wave	Sub-GHz @ 13 dBm	256	32	16	QFN32

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3. System Overview

3.1 Introduction

The Z-Wave 700 EFR32ZG14 is a serial modem device which takes advantage of Silicon Labs EFR32 SoC technology to provide a low-power, high-performance Z-Wave gateway. The EFR32ZG14 consists of a simple serial port to communicate with the host controller, and a sub-GHz radio for RF communications to Z-Wave end devices. The Z-Wave protocol stack is fully implemented on chip, and a simple serial API is used for data and control.

3.2 Power Configuration

The EFR32ZG14 is powered from a single external supply voltage. An on-chip DC-DC converter provides energy efficiency for the radio and digital subsystems. On-chip supply monitors safely manage power-up, power-down, and brown-out conditions.

Typical power supply circuitry for the EFR32ZG14 is shown below. The main system supply should be attached to VREGVDD, AVDD and IOVDD, while the DC-DC regulates the digital (DVDD) and radio (RFVDD) supplies.

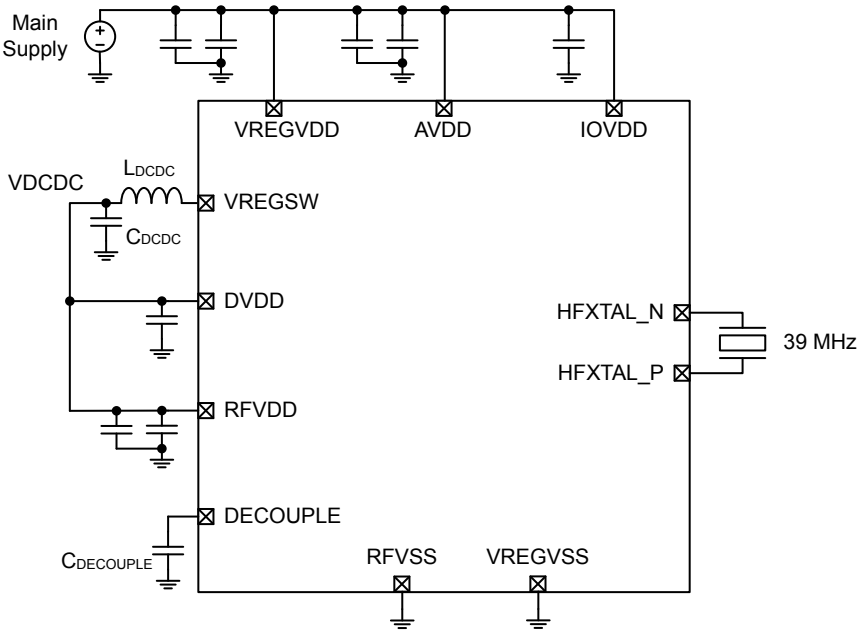


Figure 3.1. Power Supply Connections

3.2.1 Power Modes

The EFR32ZG14 uses different power modes during operation to minimize the energy consumed by the system. When the radio is active, either listening, receiving, or transmitting, the EFR32ZG14 manages thes power modes automatically, without requiring instruction from the host controller.

The host can also place the device into a low power standby state using the SUSPEND pin. When standby is active, the radio and serial interfaces are shut down and any RF connections are terminated. The system will re-establish communication when standby is released.

3.3 Radio Interface

The EFR32ZG14 includes a sub-GHz radio capable of implementing Z-Wave protocol. The differential radio interface connects to an external IPD circuit and antenna, as shown in Figure 3.2 Radio Interface on page 6.

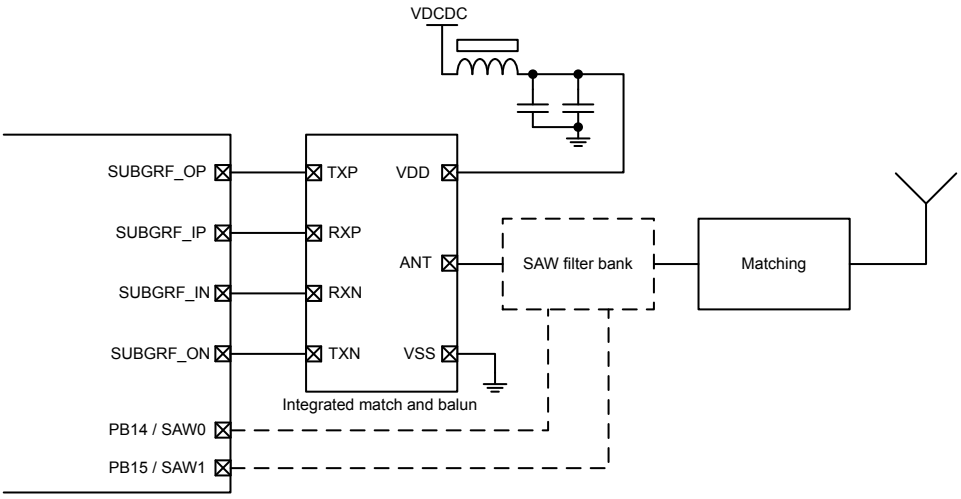


Figure 3.2. Radio Interface

For Z-Wave gateways outside EU frequency and with LTE embedded, it is recommended to analyze the specific need for a SAW filter in depth.

Optionally, a SAW filter bank can be added and controlled via the SAW0 and SAW1 output pins for operation in different regions. Table 3.1 SAW Filter Selection on page 6 details the logic output levels for different SAW filters.

Table 3.1. SAW Filter Selection

SAW1 / PB15	SAW0 / PB14	Saw Filter
0	0	H SAW Filter Selected
0	1	E SAW Filter Selected
1	0	U SAW Filter Selected

Note: The state 1, 1 for SAW1, SAW0 is undefined.

Consult with Z-Wave Global Regions frequency list to identify country specific frequency and corresponding SAW filter.

In systems where switchable filtering is not required, SAW0 and SAW1 should be left unconnected, and the appropriate RF filtering should be used.

3.4 Embedded Interface

A host controller communicates with the EFR32ZG14 using a serial API over a standard 115,200 baud UART serial interface, shown in Figure 3.3 Host Interface Connections on page 7. The RESETn signal is an active-low reset which brings the EFR32ZG14 back to its initial power-on state. An optional SUSPEND signal may also be used to place the EFR32ZG14 modem in a low power mode when radio functions are not required. The host may also supply a programming interface to update EFR32ZG14 firmware.

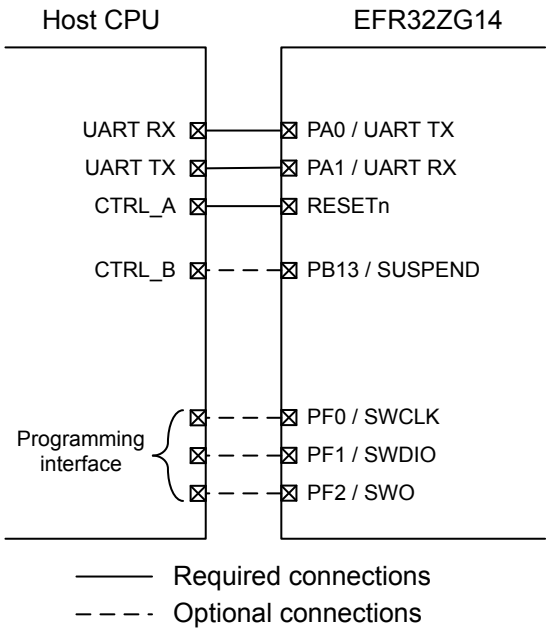


Figure 3.3. Host Interface Connections

More details of the serial API are found in INS12350 “Serial API Host Appl. Prg. Guide”.

3.5 Device Software

The EFR32ZG14 is based on a re-programmable system-on-chip MCU + radio solution. Software is provided as a pre-compiled binary image that may be installed through a standard ARM SWD interface. The binary is available for download at https://www.silabs.com.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω source or load.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on I/O pins	V_{DIGPIN}		-0.3	—	IOVDD+0.3	V
Voltage on HFXTAL_N and HFXTAL_P pins	V_{HFXTAL}		-0.3	—	1.4	V
Absolute voltage on Sub-GHz RF pins	$V_{MAXSUBG}$	Pins SUBGRF_OP and SUBGRF_ON	-0.3	—	3.3	V
		Pins SUBGRF_IP and SUBGRF_IN,	-0.3	—	0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD, RFVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[1]	T_A	-G temperature grade	-40	25	85	°C
AVDD supply voltage[2]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[2 3]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[4 5]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)[2]	dV_{DD}		—	—	0.1	V

Note:

1. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
4. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
5. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	2-Layer PCB, Air velocity = 0 m/s	—	82.1	—	°C/W
		2-Layer PCB, Air velocity = 1 m/s	—	64.7	—	°C/W
		2-Layer PCB, Air velocity = 2 m/s	—	56.3	—	°C/W
		4-Layer PCB, Air velocity = 0 m/s	—	36.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.6	—	°C/W

4.1.4 DC-DC Converter

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCDC nominal output capacitor[1]	C_{DCDC}	25% tolerance	4.7	4.7	4.7	µF
DCDC nominal output inductor[1]	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH

Note:
1. Refer to the Z-Wave Hardware Implementation Guidelines for component selection to achieve optimal performance.

4.1.5 Current Consumption

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = 1.8 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current During Active Radio Reception	I_{ACTIVE_RX}		—	10.5	—	mA
Current With Radio Listening, No Active Reception	I_{LISTEN_RX}		—	10.5	—	mA
Current During Active Radio Transmission	I_{ACTIVE_TX}	Radio transmitter output power at 13 dBm	—	38.8	—	mA
		Radio transmitter output power at 4 dBm	—	17.2	—	mA
		Radio transmitter output power at 0 dBm	—	12.9	—	mA
CPU-Only Current	I_{CPU_ONLY}	CPU active without radio active	—	3.1	—	mA

4.1.6 Brown Out Detector (BOD)

Table 4.6. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	1.3	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	1.53	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.7 Sub-GHz RF Transceiver Characteristics

4.1.7.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External RF Supply. RFVDD and RF supply paths are filtered using ferrites. Crystal frequency = 39 MHz. RF frequency band 915 MHz.

Table 4.7. Sub-GHz RF Transmitter characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		902	—	930	MHz
Maximum TX Power[1]	$POUT_{MAX}$	4 dBm output power setting	—	4	—	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-30	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, T = 25 °C	—	1.9	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C	—	1.3	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T = 25 °C, Over specified RF tuning frequency range	—	0.5	—	dB
Spurious emissions of harmonics at 3 dBm output power, Conducted measurement, 3dBm match, Test Frequency = 908.4 MHz	$SPUR_{HARM\_FCC\_14}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-60.0	-42	dBm
		In non-restricted bands, per FCC Part 15.231	—	-58.0	-20	dBc
Spurious emissions out-of-band at 3 dBm output power, Conducted measurement, 3dBm match, Test Frequency = 908.4 MHz	$SPUR_{OOB\_FCC\_14}$	In non-restricted bands, per FCC Part 15.231	—	-74.0	-20	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-59.2	-46	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-72.6	-56	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-72.1	-52	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-66.1	-42	dBm
Power spectral density limit	PSD	PSD per FCC Part 15.247, 9.6Kbps	—	-0.7	—	dBm/ 3kHz
		PSD per FCC Part 15.247, 40Kbps	—	2.2	—	dBm/ 3kHz
		PSD per FCC Part 15.247, 100Kbps	—	-4.2	—	dBm/ 3kHz

Note:

1. The output power level can be adjusted to suit specific regulatory requirements for the region in which the device is used.

4.1.7.2 Sub-GHz RF Receiver Characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External RF Supply. RFVDD and RF supply paths are filtered using ferrites. Crystal frequency = 39 MHz. RF frequency band 915 MHz.

Table 4.8. Sub-GHz RF Receiver Characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		902	—	930	MHz
Max usable input level, 1% FER	SAT_{100K}	Desired is reference 100 kbps GFSK signal[1]	—	10	—	dBm
Sensitivity[2] [3]	SENS	Desired is reference 100 kbps GFSK signal[1], 1% FER, frequency = 916 MHz, T ≤ 85 °C	—	-98.8	—	dBm
		Desired is reference 40 kbps 2FSK signal[4], 1% FER, frequency = 908.4 MHz, T ≤ 85 °C	—	-102.8	—	dBm
		Desired is reference 9.6 kbps 2FSK signal[5], 1% FER, frequency = 908.42 MHz, T ≤ 85 °C	—	-103.9	—	dBm
Level above which RFSENSE will trigger[6]	$RFSENSE_{TRIG}$	CW at 915 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger[6]	$RFSENSE_{THRES}$	CW at 915 MHz	—	-50	—	dBm
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 1% FER, frequency = 916 MHz	—	33	—	dB
		Desired is reference 40 kbps 2FSK signal[4] at 3dB above sensitivity level, 1% FER, frequency = 908.4 MHz	—	34.3	—	dB
		Desired is reference 9.6 kbps 2FSK signal[5] at 3dB above sensitivity level, 1% FER, frequency = 908.42 MHz	—	34.7	—	dB
Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, frequency = 916 MHz	$C/I_{BLOCKER\_100}$	Interferer CW at Desired ± 1 MHz	—	47.1	—	dB
		Interferer CW at Desired ± 2 MHz	—	52.7	—	dB
		Interferer CW at Desired ± 5 MHz	—	61.3	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	65.7	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	78.0	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal[4] at 3dB above sensitivity level, frequency = 908.4 MHz	$C/I_{BLOCKER\_40}$	Interferer CW at Desired ± 1 MHz	—	53.1	—	dB
		Interferer CW at Desired ± 2 MHz	—	59.3	—	dB
		Interferer CW at Desired ± 5 MHz	—	71.6	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	79.3	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	82.2	—	dB
Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal[5] at 3dB above sensitivity level, frequency = 908.42 MHz	$C/I_{BLOCKER\_9p6}$	Interferer CW at Desired ± 1 MHz	—	54.3	—	dB
		Interferer CW at Desired ± 2 MHz	—	60.4	—	dB
		Interferer CW at Desired ± 5 MHz	—	72.7	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	80.1	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	83.5	—	dB
Intermod selectivity, 1% FER. CW interferers at 400 kHz and 800 kHz offsets	C/I_{IM}	Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, frequency = 916 MHz	—	31.0	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216-960 MHz	—	-59.9	-49.2	dBm
		Above 960 MHz	—	-55.7	-41.2	dBm
Max spurious emissions during active receive mode,per ARIB STD-T108 Section 3.3	$SPUR_{RX\_ARIB}$	Below 710 MHz, RBW=100kHz	—	-66.3	-54	dBm
		710-900 MHz, RBW=1MHz	—	-70.8	-55	dBm
		900-915 MHz, RBW=100kHz	—	-70.4	-55	dBm
		915-930 MHz, RBW=100kHz	—	-70.7	-55	dBm
		930-1000 MHz, RBW=100kHz	—	-70.8	-54	dBm
		Above 1000 MHz, RBW=1MHz	—	-69.3	-47	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Minimum Packet Error Rate floor will be ~0.5% for desired input signal levels between specified datasheet sensitivity level and -10dBm.
3. Minimum Packet Error Rate floor will be ~ 1% for desired input signal levels > -10dBm.
4. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
5. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + 20k + Δf/2), '1' = Transition from (F_center + 20k - Δf/2)
6. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.
7. Minimum Packet Error Rate floor for signals in presecene of blocker will increase above 1% for blocker levels above -30dBm.

4.1.7.3 Sub-GHz RF Transmitter characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External RF Supply. RFVDD and RF supply paths are filtered using ferrites. Crystal frequency = 39 MHz. RF frequency band 868 MHz.

Table 4.9. Sub-GHz RF Transmitter characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		863	—	876	MHz
Maximum TX Power[1]	$POUT_{MAX}$	13 dBm output power setting	—	13	—	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-30	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, T = 25 °C	—	2.4	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C	—	1.3	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T = 25 °C, Over specified RF tuning frequency range	—	0.4	—	dB
Spurious emissions of harmonics, Conducted measurement, Test Frequency = 868.4 MHz	$SPUR_{HARM\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1	—	-39	-30	dBm
Spurious emissions out-of-band, Conducted measurement, Test Frequency = 868.4 MHz	$SPUR_{OOB\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-69.6	-54	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-69.8	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-64.9	-30	dBm

Note:

1. The output power level can be adjusted to suit specific regulatory requirements for the region in which the device is used.

4.1.7.4 Sub-GHz RF Receiver Characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External RF Supply. RFVDD and RF supply paths are filtered using ferrites. Crystal frequency = 39 MHz. RF frequency band 868 MHz.

Table 4.10. Sub-GHz RF Receiver Characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		863	—	876	MHz
Max usable input level, 1% FER	SAT_{100k}	Desired is reference 100 kbps GFSK signal[1]	—	10	—	dBm
Sensitivity[2] [3]	SENS	Desired is reference 100 kbps GFSK signal[1], 1% FER, frequency = 869.85 MHz, T ≤ 85 °C	—	-98.6	—	dBm
		Desired is reference 40 kbps 2FSK signal[4], 1% FER, frequency = 868.4 MHz, T ≤ 85 °C	—	-102.3	—	dBm
		Desired is reference 9.6 kbps 2FSK signal[5], 1% FER, frequency = 868.42 MHz, T ≤ 85 °C	—	-103.3	—	dBm
Level above which RFSENSE will trigger[6]	$RFSENSE_{TRIG}$	CW at 868 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger[6]	$RFSENSE_{THRES}$	CW at 868 MHz	—	-50	—	dBm
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 100kbps GFSK signal[1] at 3dB above sensitivity level, 1% FER, frequency = 869.85 MHz	—	33.6	—	dB
		Desired is reference 40 kbps 2FSK signal[4] at 3dB above sensitivity level, 1% FER, frequency = 868.4 MHz	—	35.4	—	dB
		Desired is reference 9.6 kbps 2FSK signal[5] at 3dB above sensitivity level, 1% FER, frequency = 868.42 MHz	—	35.5	—	dB
Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal[1] at 3 dB above sensitivity level, frequency = 869.85 MHz	$C/I_{BLOCKER\_100}$	Interferer CW at Desired ± 1 MHz	—	49.2	—	dB
		Interferer CW at Desired ± 2 MHz	—	55.6	—	dB
		Interferer CW at Desired ± 5 MHz	—	67.3	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	74.3	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	79.0	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal[4] at 3 dB above sensitivity level, frequency = 868.4 MHz	$C/I_{BLOCKER\_40}$	Interferer CW at Desired ± 1 MHz	—	53.4	—	dB
		Interferer CW at Desired ± 2 MHz	—	59.4	—	dB
		Interferer CW at Desired ± 5 MHz	—	71.9	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	79.4	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	83.2	—	dB
Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal[5] at 3 dB above sensitivity level, frequency = 868.42 MHz	$C/I_{BLOCKER\_9p6}$	Interferer CW at Desired ± 1 MHz	—	54.5	—	dB
		Interferer CW at Desired ± 2 MHz	—	60.4	—	dB
		Interferer CW at Desired ± 5 MHz	—	73.0	—	dB
		Interferer CW at Desired ± 10 MHz[7]	—	80.0	—	dB
		Interferer CW at Desired ± 100 MHz[7]	—	84.3	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode	$SPUR_{RX}$	30 MHz to 1 GHz	—	-54.4	—	dBm
		1 GHz to 12 GHz	—	-63.8	—	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Minimum Packet Error Rate floor will be ~0.5% for desired input signal levels between specified datasheet sensitivity level and -10dBm.
3. Minimum Packet Error Rate floor will be ~ 1% for desired input signal levels > -10dBm.
4. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
5. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + 20k + Δf/2), '1' = Transition from (F_center + 20k - Δf/2)
6. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.
7. Minimum Packet Error Rate floor for signals in presecene of blocker will increase above 1% for blocker levels above -30dBm.

4.1.8 High-Frequency Crystal Oscillator (HFXO)

Table 4.11. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency[1]	f_{HFXO}		39	39	39	MHz
Frequency tolerance for the crystal	FT_{HFXO}	-40 to 85 °C, 5 years of aging	-25	—	25	ppm

Note:
1. Refer to the Z-Wave Hardware Implementation Guidelines for recommended crystals.

4.1.9 I/O Characteristics

Table 4.12. I/O Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	All inputs	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	All inputs	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 20 mA, IOVDD ≥ 3 V	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 20 mA, IOVDD ≥ 3 V	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	Input pin voltage ≤ IOVDD , T ≤ 85 °C	—	0.1	30	nA
I/O pin pull-up/pull-down resistor[1]	R_{PUD}		30	40	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	45	ns
Output fall time, From 70% to 30% of V_{IOVDD}	t_{IOOF}	All outputs, C_L = 50 pF	—	1.8	—	ns
Output rise time, From 30% to 70% of V_{IOVDD}	t_{IOOR}	All outputs, C_L = 50 pF	—	2.2	—	ns

Note:
1. GPIO pull-ups are referenced to the IOVDD supply, except for RESETn, which connects to AVDD.

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

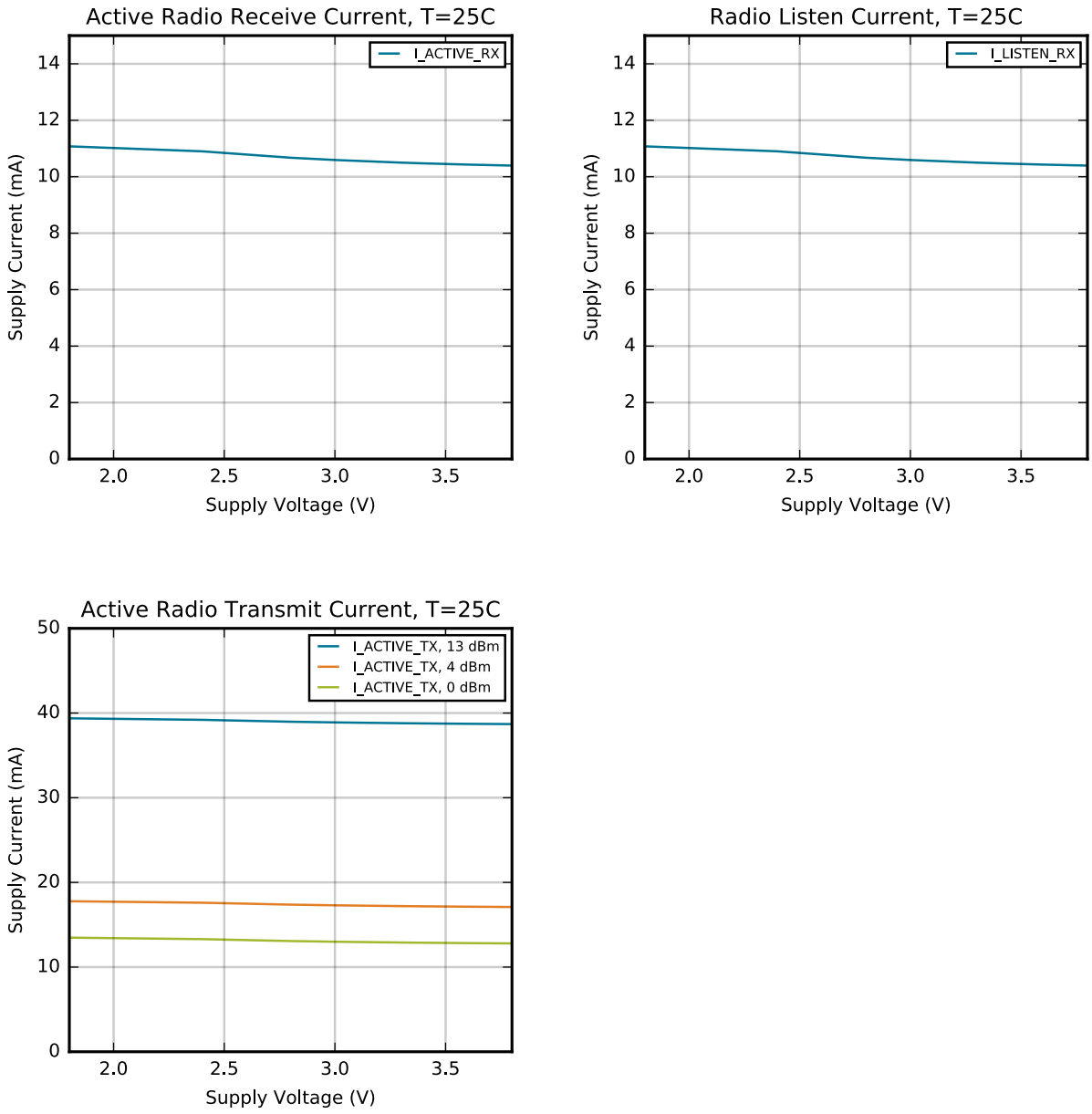


Figure 4.1. Supply Current vs. Supply Voltage

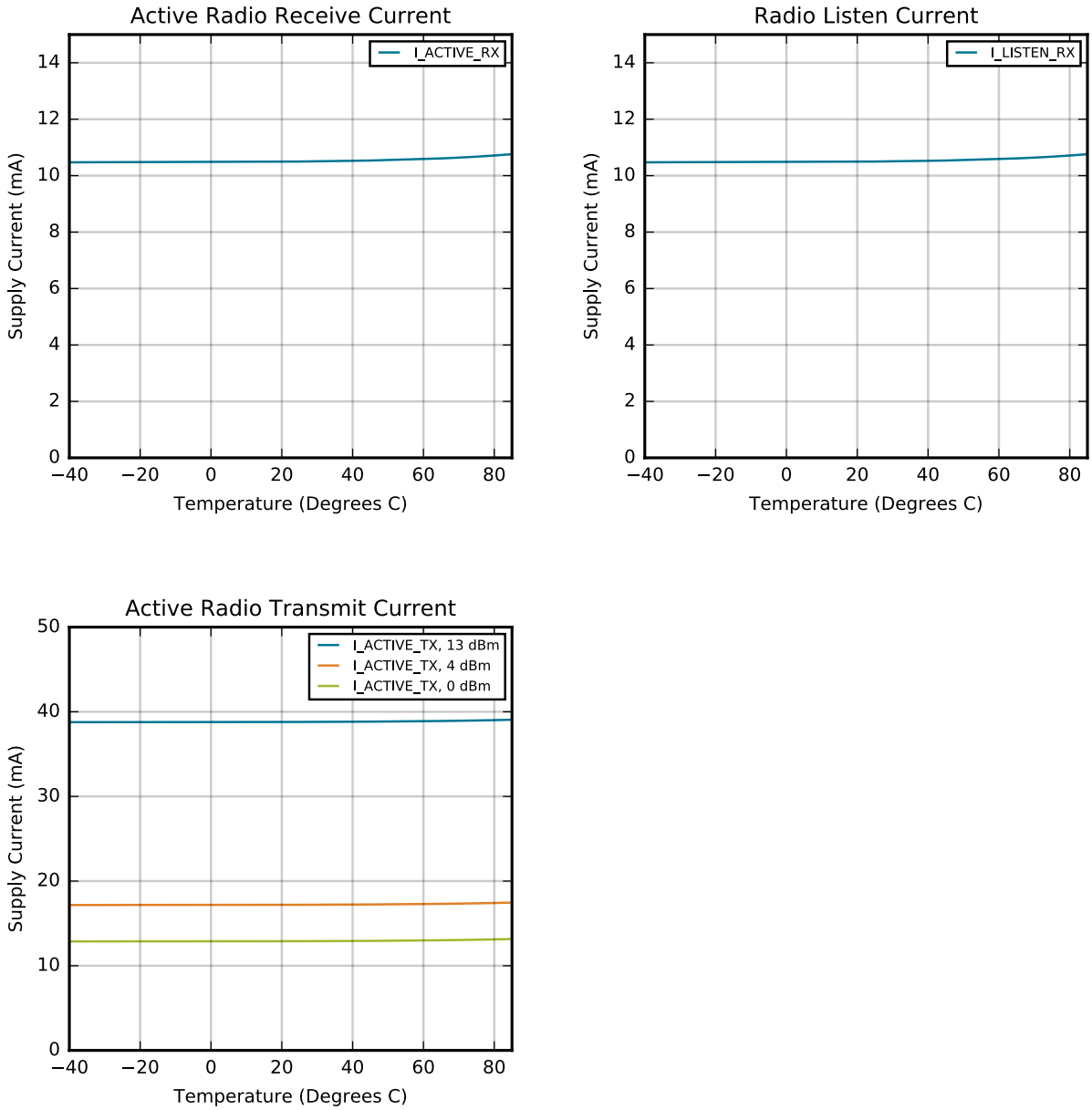


Figure 4.2. Supply Current vs. Temperature

4.2.2 Z-Wave Radio

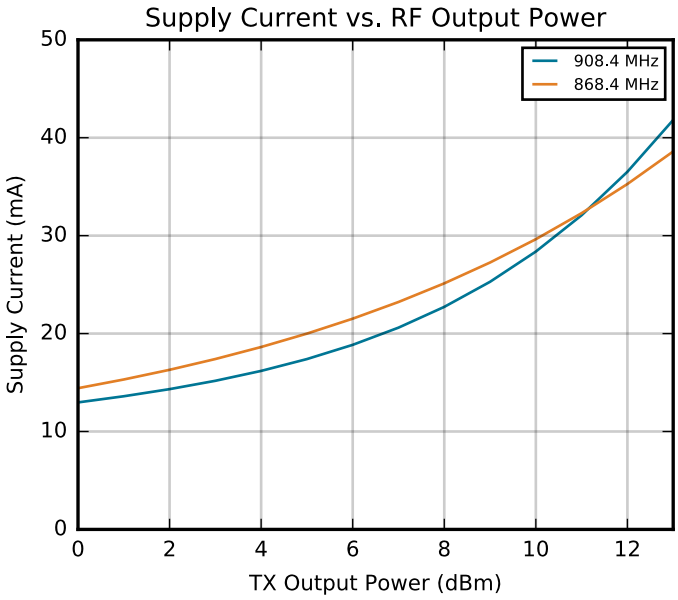


Figure 4.3. RF Transmitter Output Power

5. Typical Connection Diagrams

Typical connections for the EFR32ZG14 are shown in Figure 5.1 Typical System Connections on page 22. Refer to the design files for BRD4201 for more specific details on component choice.

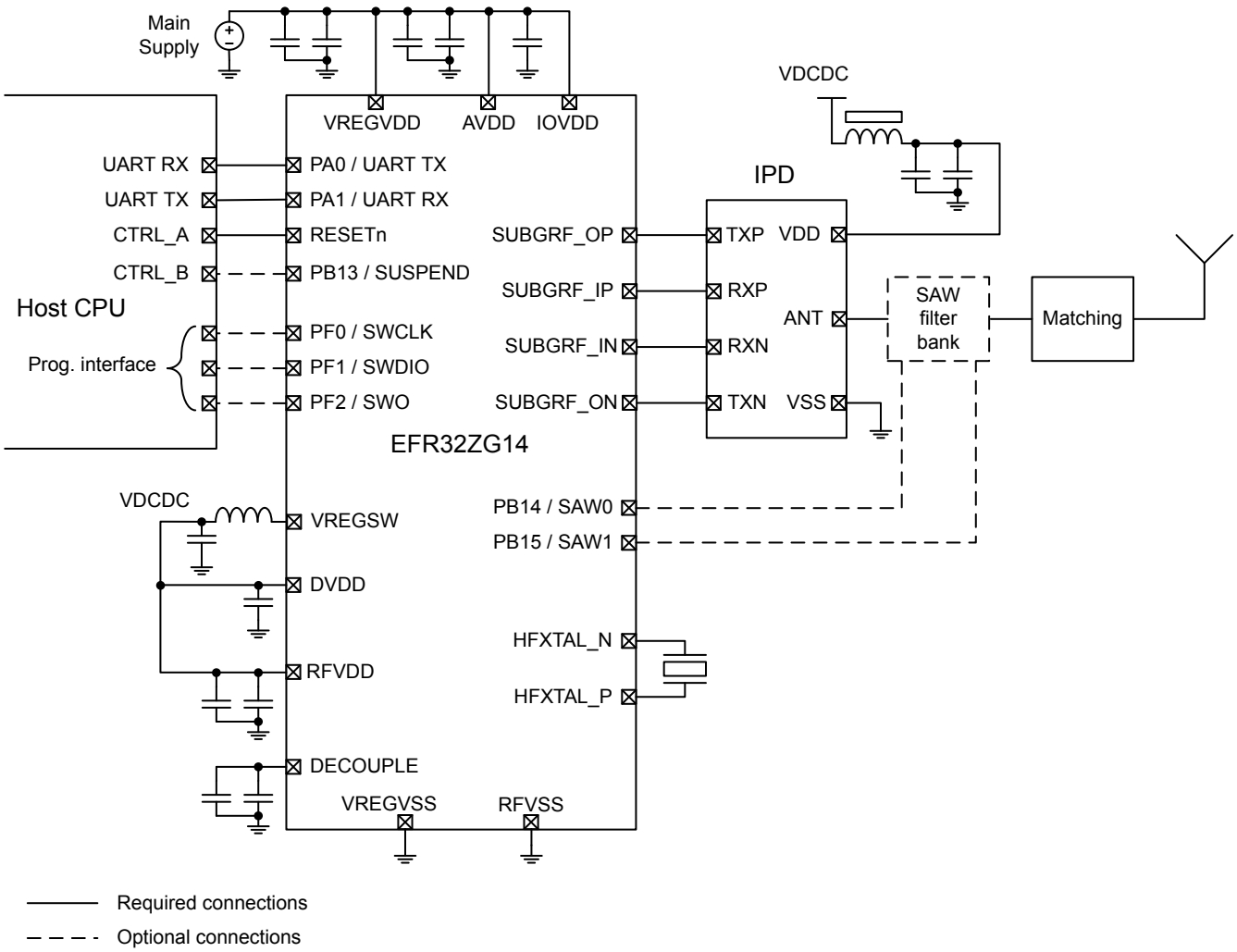


Figure 5.1. Typical System Connections

6. EFR32ZG14 Device Pinout

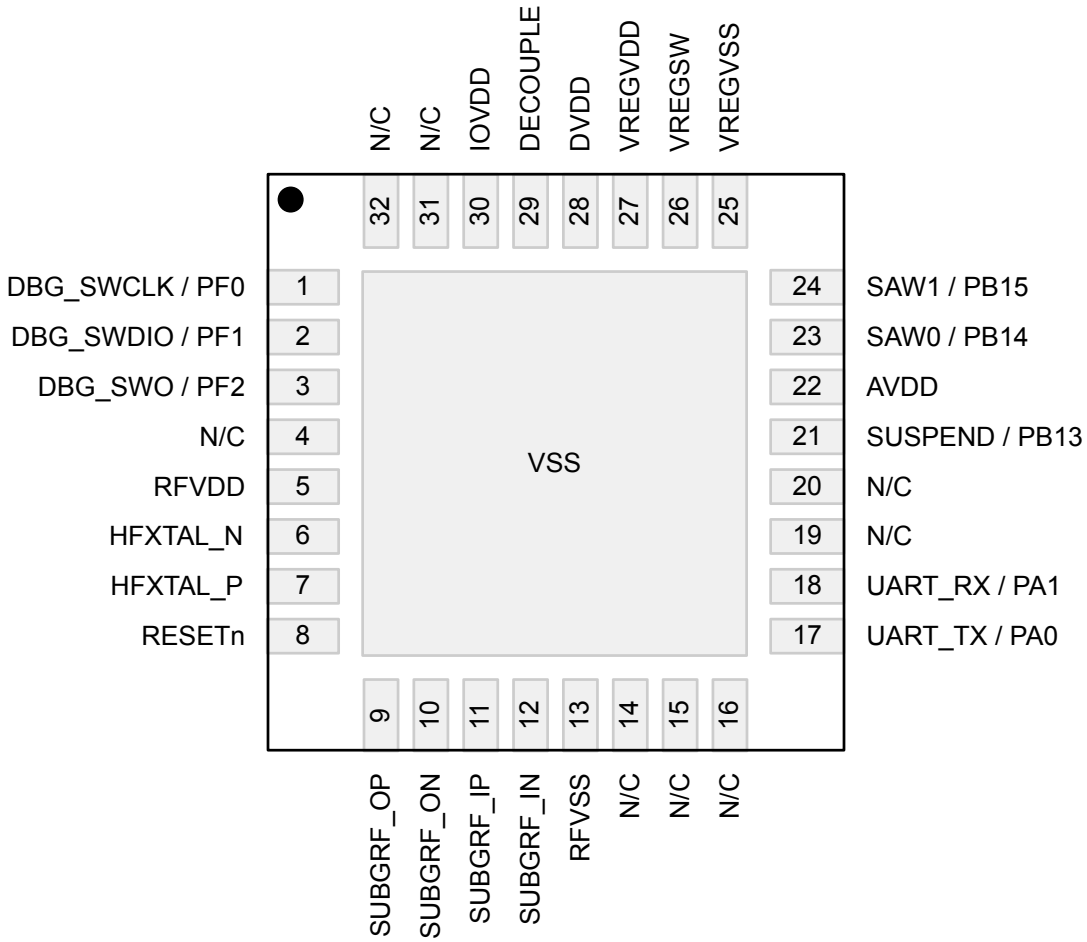


Figure 6.1. EFR32ZG14 Device Pinout

Table 6.1. EFR32ZG14 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	DBG_SWCLK - Serial Wire Debug Clock
PF1	2	DBG_SWDIO - Serial Wire Debug Data I/O	PF2	3	DBG_SWO - Serial Wire Viewer Output
N/C	4, 14, 15, 16, 19, 20, 31, 32	No Connect	RFVDD	5	Radio power supply
HFXTAL_N	6	High Frequency Crystal input pin.	HFXTAL_P	7	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	8	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	9	Sub GHz Differential RF output, positive path.
SUBGRF_ON	10	Sub GHz Differential RF output, negative path.	SUBGRF_IP	11	Sub GHz Differential RF input, positive path.
SUBGRF_IN	12	Sub GHz Differential RF input, negative path.	RFVSS	13	Radio Ground
PA0	17	UART_TX - UART Serial Data Output	PA1	18	UART_RX - UART Serial Data Input
PB13	21	SUSPEND - Suspend Input	AVDD	22	Analog power supply.
PB14	23	SAW0 - Saw Filter Select 0 Output	PB15	24	SAW1 - Saw Filter Select 1 Output
VREGVSS	25	Voltage regulator VSS	VREGSW	26	DCDC regulator switching node
VREGVDD	27	Voltage regulator VDD input	DVDD	28	Digital power supply.
DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	IOVDD	30	Digital IO power supply.

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

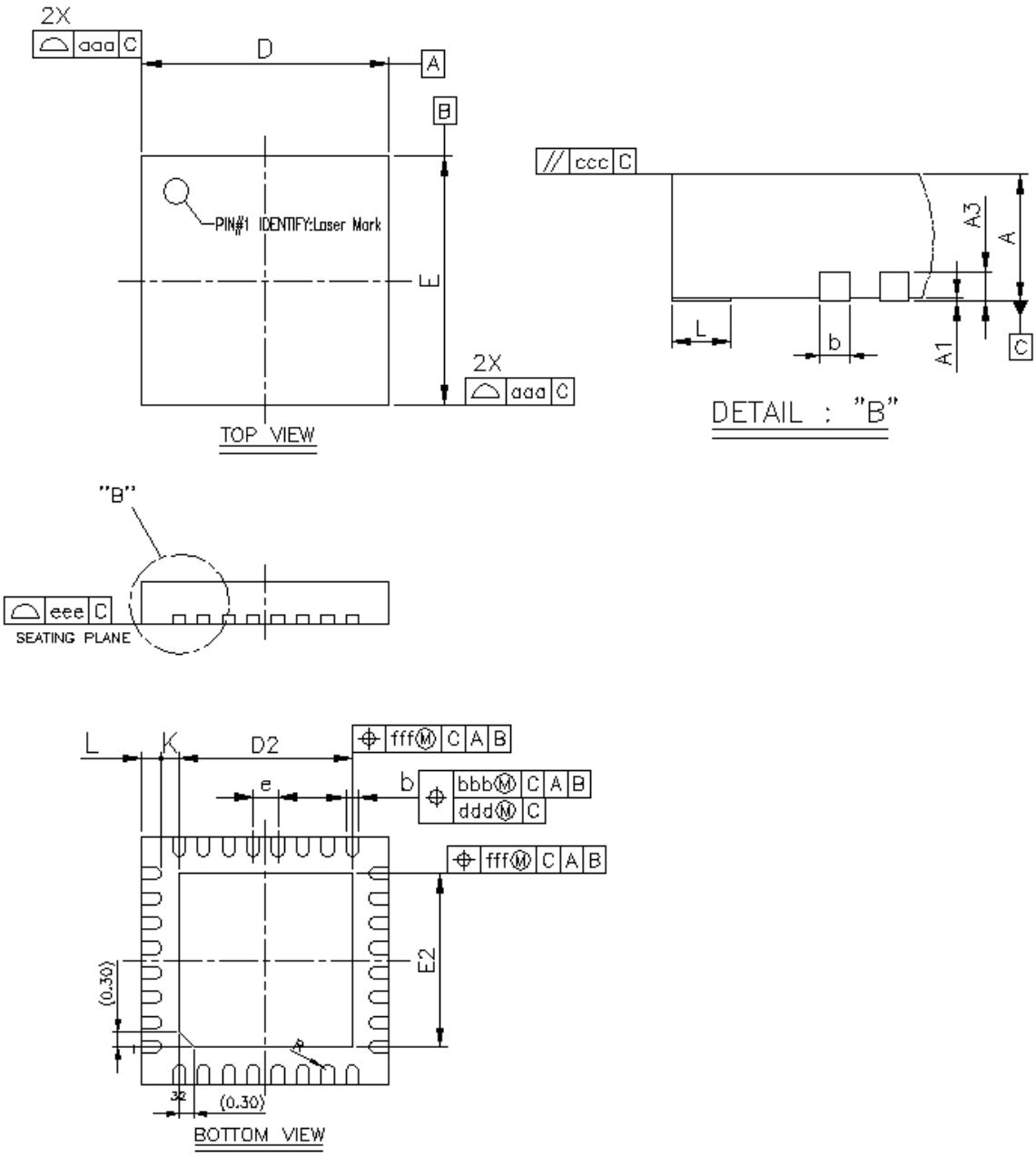


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

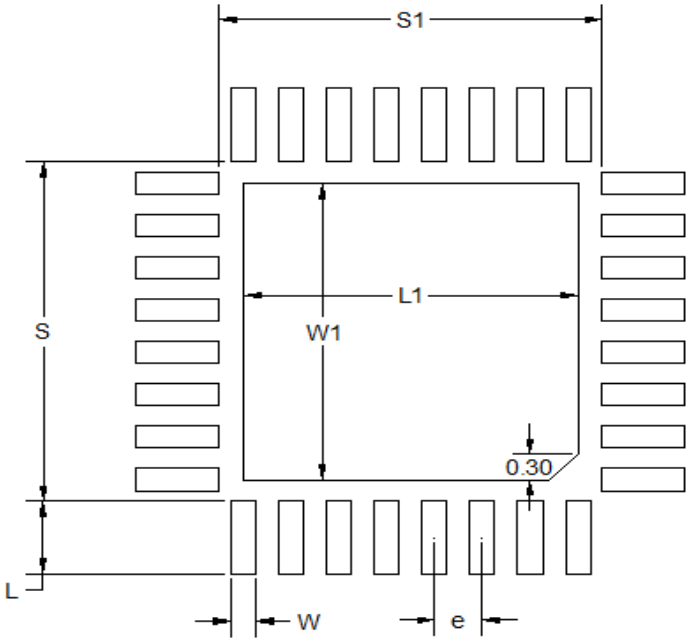


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN32 Package Marking

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
  1. Family Code (Z)
  2. G (Gecko)
  3. Series (1)
  4. Device Configuration (4)
  5. Performance Grade (P)
  6. Feature Code (2)
  7. TRX Code (3 = TXRX)
  8. Band (1 = Sub-GHz)
  9. Flash (G = 256K)
  10. Temperature Grade (G = -40 to 85)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

8. Revision History

Revision 1.0

January 2019

- Updated electrical characteristics with latest characterization results.

Revision 0.2

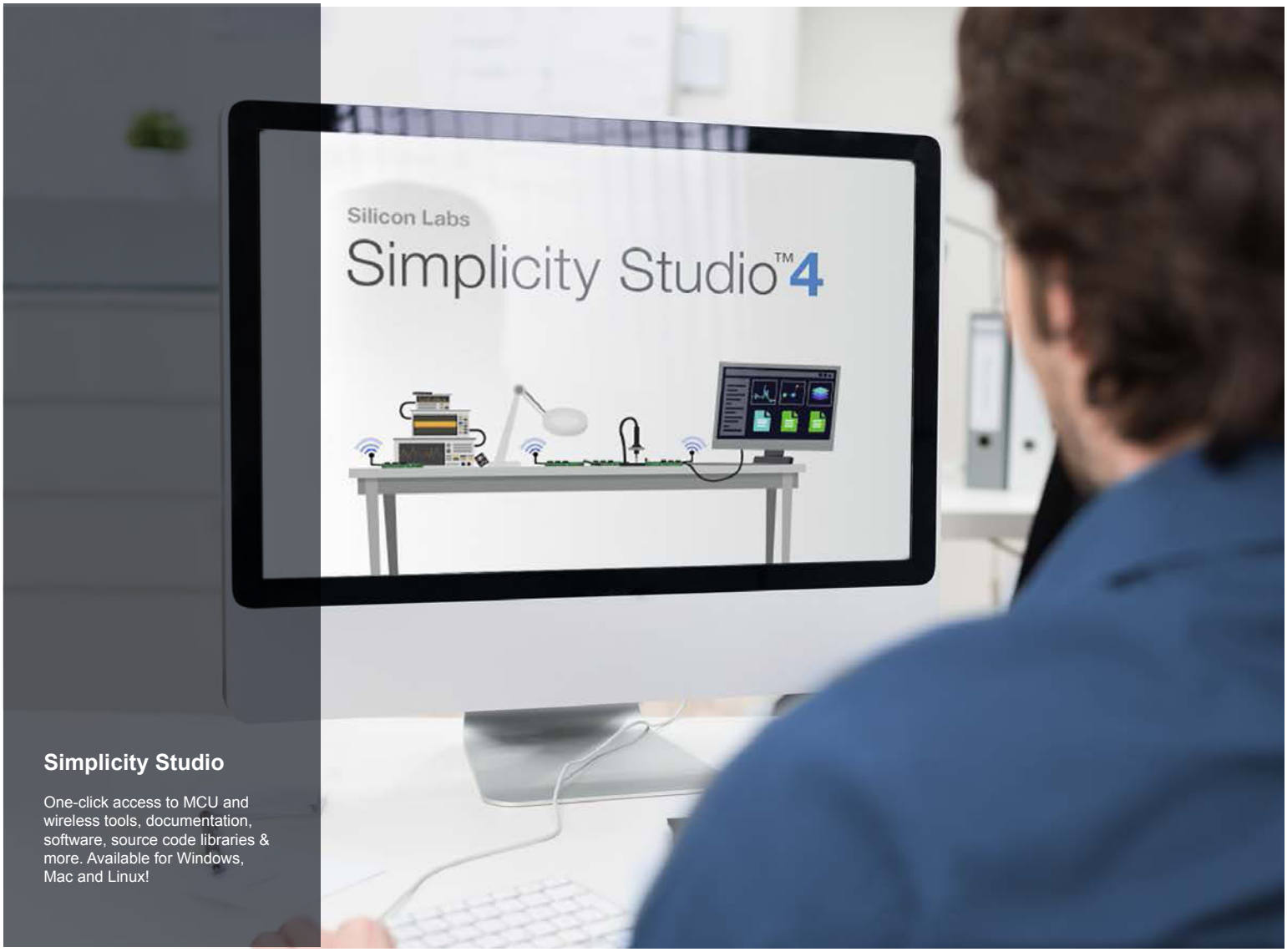
December 2018

- Required crystal frequency changed to 39 MHz.
- Updated electrical characteristics with latest characterization estimates.
- Table 4.7 Sub-GHz RF Transmitter characteristics for 915 MHz Band on page 12: PSD conditions updated to specify PSD at each data rate.

Revision 0.1

September, 2018

Initial release.



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