# MGM210P Wireless Gecko Multi-Protocol Module Data Sheet

The MGM210P is a module designed and built to meet the performance, security, and reliability requirements of line-powered IoT products for mesh networks.

Based on the EFR32MG21 SoC, it enables Zigbee®, OpenThread®, Bluetooth® and multi-protocol connectivity (Zigbee + Bluetooth) while delivering best-in-class RF range and performance, future-proof capability for feature and OTA firmware updates, state-of-the-art security, low active current consumption, and a temperature rating suited for operation in demanding environmental conditions.

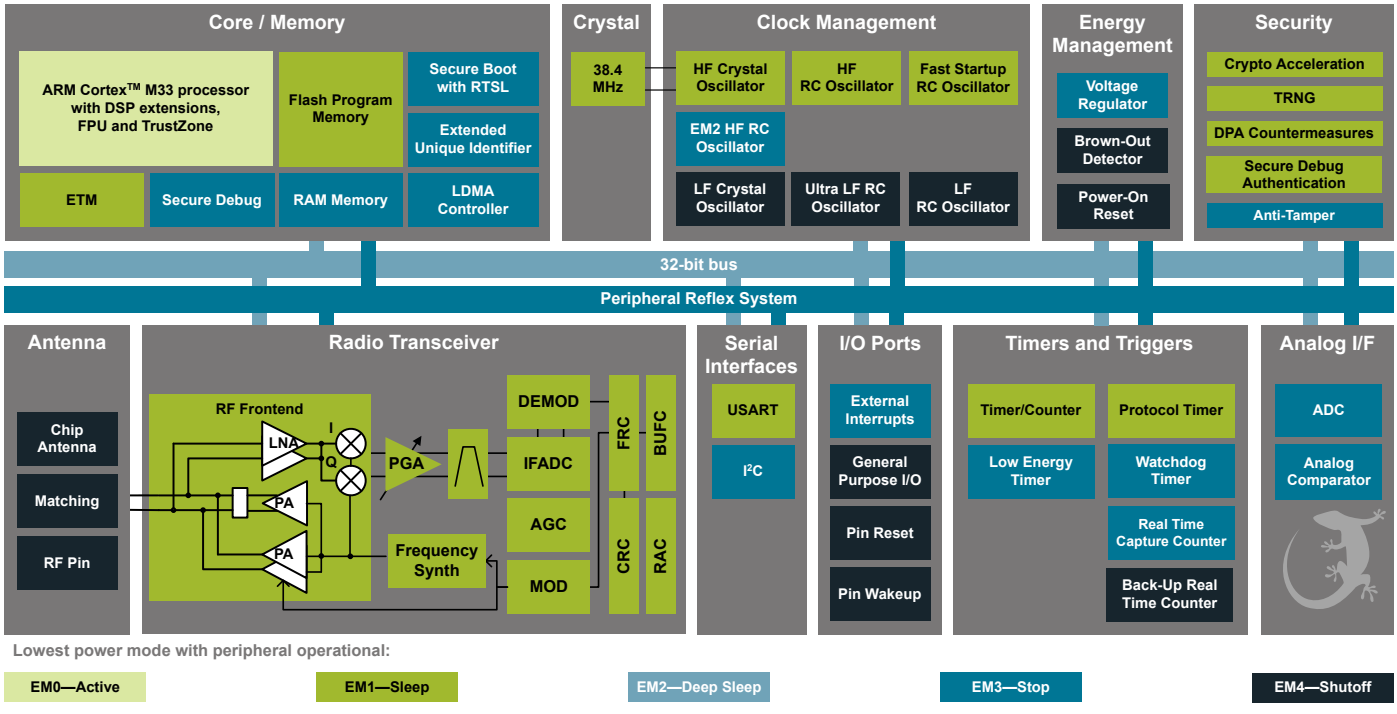
The MGM210P is a complete solution that comes with robust and fully-upgradeable software stacks, world-wide regulatory certifications, advanced development and debugging tools, and support that will simplify and minimize the development cycle and deployment of your end-product helping to accelerate its time-to-market.

The MGM210P is targeted for a broad range of applications, including:

- Smart home
- Connected lighting
- Building automation and security

**KEY FEATURES**

- Zigbee, OpenThread, Bluetooth 5.x, and multi-protocol connectivity
- Built-in antenna and RF pin
- +10 and +20 dBm TX power variants
- -103.9 dBm 802.15.4 RX sensitivity
- -97.0 dBm Bluetooth RX sensitivity at 1 Mbps
- 32-bit ARM Cortex-M33 core at 38.4 MHz
- 1024/96 kB of Flash/RAM memory
- Secure Vault Mid or High
- Optimal set of MCU peripherals
- 20 GPIO pins
- -40 to +125 °C
- 12.9 mm x 15.0 mm x 2.2 mm



# 1. Features

- **Supported Protocols**
  - Zigbee
  - OpenThread
  - Bluetooth 5.x
  - Bluetooth Mesh
  - Multi-protocol (Zigbee + Bluetooth 5.x)
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +20 dBm
  - 32-bit ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 1024 kB flash program memory
  - 96 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **Receiver Performance**
  - -103.9 dBm sensitivity (1% PER) at 250 kbps O-QPSK DSSS
  - -104.5 dBm sensitivity (0.1% BER) at 125 kbps GFSK
  - -100.1 dBm sensitivity (0.1% BER) at 500 kbps GFSK
  - -97.0 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
  - -94.1 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Current Consumption**
  - 9.4 mA RX current at 250 kbps O-QPSK DSSS
  - 9.3 mA RX current at 1 Mbps GFSK
  - 16.1 mA TX current at 0 dBm (MGM210Px22)
  - 34.1 mA TX current at 10 dBm (MGM210Px22)
  - 181.3 mA TX current at 20 dBm (MGM210Px32)
  - 50.9 µA/MHz in Active Mode (EM0)
  - 5.1 µA EM2 DeepSleep current (RTCC running from LFXO, Bluetooth Stack not running)
  - 8.5 µA EM2 DeepSleep current (RTCC running from LFXO, Bluetooth Stack running)
- **Regulatory Certifications**
  - CE and UKCA - EU and UK
  - FCC - USA
  - ISED - Canada
  - MIC - Japan
  - KC - South Korea
- **Operating Range**
  - 1.71 to 3.8 V
  - -40 to +125°C
- **Dimensions**
  - 12.9 mm x 15.0 mm x 2.2 mm
- **Security**[2]
  - Secure Boot with Root of Trust and Secure Loader (RTSL)[1]
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH (P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug Interface lock/unlock
  - DPA Countermeasures[1]
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
- **MCU Peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - 20 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 3 × 16-bit Timer/Counter (3 Compare/Capture/PWM channels)
  - 1 × 32-bit Timer/Counter (3 Compare/Capture/PWM channels)
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 2 × Watchdog Timer
  - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/$I^2S$)
  - 2 × $I^2C$ interface with SMBus support

1. With Secure Engine (SE) firmware v1.1.2 or newer
2. See Table 3.2 Security Features and Levels on page 7 for details on security level differences between MGM210PB and MGM210PA part numbers.

# 2. Ordering Information

**Table 2.1. Ordering Information**

| Ordering Code | Protocol Stack | TX Power | Secure Vault | Antenna | Flash (kB) | RAM (kB) | GPIO | Temp Range | Packaging |
|---|---|---|---|---|---|---|---|---|---|
| MGM210PA22JIA2 | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 10 dBm | Mid | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Cut Tape |
| MGM210PA22JIA2R | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 10 dBm | Mid | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Reel |
| MGM210PA32JIA2 | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 20 dBm | Mid | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Cut Tape |
| MGM210PA32JIA2R | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 20 dBm | Mid | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Reel |
| MGM210PB22JIA2 | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 10 dBm | High | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Cut Tape |
| MGM210PB22JIA2R | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 10 dBm | High | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Reel |
| MGM210PB32JIA2 | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 20 dBm | High | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Cut Tape |
| MGM210PB32JIA2R | • Zigbee<br>• OpenThread<br>• Bluetooth 5.x | 20 dBm | High | Built-in and RF pin | 1024 | 96 | 20 | -40 to 125 °C | Reel |

Bluetooth 5.x: As the Bluetooth standard evolves, Silicon Labs is regularly adding new features. For more information on supported Bluetooth capabilities, visit https://www.silabs.com/bluetooth-hardware.

All MGM210P devices operate in the 2.4 GHz ISM frequency band.

Refer to 4.5 RF Transmitter General Characteristics for maximum TX power figures.

End-product manufacturers must verify that the module is configured to comply with the proper regulatory limits for each region, in accordance with the formal certification test reports for the device.

MGM210P modules are pre-programmed with UART XMODEM bootloader.

Devices may be referred to by their product family name (e.g. MGM210P), model name (MGM210P22A / MGM210P32A) or full ordering code throughout this document.

The **SLWSTK6102A Wireless Gecko Module Starter Kit** is available for MGM210P evaluation and development, as well as the **SLWRB4308A** (+20 dBm TX, Secure Vault Mid), **SLWRB4308B** (+10 dBm TX, Secure Vault Mid), **SLWRB4308C** (+20 dBm TX, Secure Vault High) and **SLWRB4308D** (+10 dBm TX, Secure Vault High) radio boards.

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# 3. System Overview

## 3.1 Block Diagram

The MGM210P module is a highly-integrated, high-performance system with all the hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple protocols.

Built around the EFR32MG21 Wireless Gecko SoC, the MGM210P includes, both, a built-in antenna and a 50 Ω-matched RF pin, RF matching networks (optimized for transmit power efficiency), supply decoupling and filtering components, a 38.4 MHz reference crystal, and an RF shield. Also, it allows using an external 32 kHz crystal as a low frequency reference signal via GPIO pins. A 32.768 kHz crystal provides an accurate timing reference for low energy modes.

Since the RF matching networks are optimized for transmit power efficiency, modules rated for +20 dBm will show non-optimal current consumption and performance when operated at a lower output power (e.g. +10 or 0 dBm). The same applies for modules rated for +10 dBm.

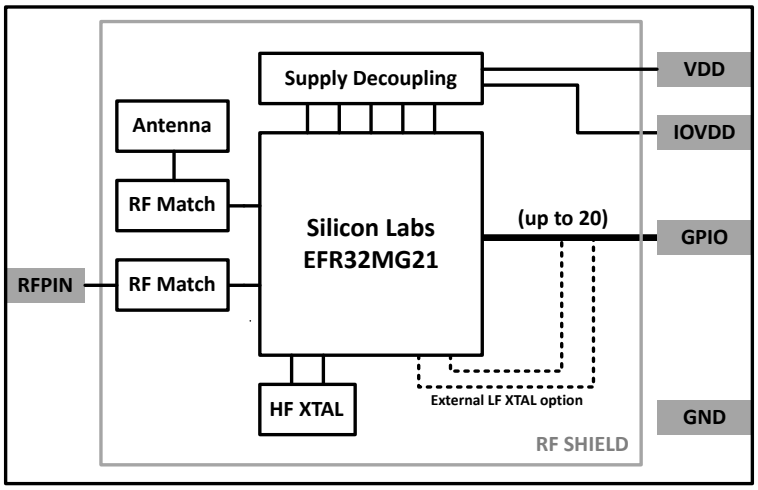


**Figure 3.1. MGM210P Block Diagram**

## 3.2 EFR32MG21 SoC

The EFR32MG21 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 1 MB of Flash memory, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. Consult the EFR32xG21 Wireless Gecko Reference Manual and the EFR32MG21 Data Sheet for details.

## 3.3 Antenna

MGM210P modules include a built-in antenna with the characteristics detailed in the table below. They also include a 50 Ω-matched RF pin to enable the use of an external antenna instead of the one built-in. See Section 4.17.1 Antenna Radiation and Efficiency and Section 11.1 Qualified Antennas for other relevant details. Antenna diversity is not supported.

**Table 3.1. Antenna Efficiency and Peak Gain**

| Parameter | With optimal layout | Note |
|---|---|---|
| Efficiency | -1 to -2 dB | Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to the Design Guidelines for recommendations to achieve optimal antenna performance. |
| Peak gain | 1.86 dBi | |

### 3.4 Power Supply

The MGM210P requires a single nominal supply level of 3.0 V to operate. However, it can support use cases needing different levels for the main supply (VDD) and for digital IO (IOVDD).

The DECOUPLE pin exposes the SoC's on-chip digital supply regulator output and allows introducing an external digital supply source via a PMIC, for example. The default recommendation is to leave the DECOUPLE pin disconnected.

All necessary components for supply decoupling and filtering are included in the module.

### 3.5 Security

MGM210P modules support one of two levels in the Security Portfolio offered by Silicon Labs: Secure Vault Mid or Secure Vault High.

Secure Vault is a collection of technologies that deliver state-of-the-art security and upgradability features to protect and future-proof IoT devices against costly threats, attacks and tampering. Secure Vault Mid is the hardware-based subsystem at the core of Secure Vault that enables a subset of its features only. MGM210PB part numbers support Secure Vault High and MGM210PA part numbers support Secure Vault Mid.

**Table 3.2. Security Features and Levels**

| Feature | Secure Vault | |
|---|---|---|
| | Mid | High |
| Secure Boot with Root of Trust and Secure Loader (RTSL) | X | X |
| Cryptographic Accelerator | X | X |
| ARM TrustZone | X | X |
| True Random Number Generator (TRNG) | X | X |
| Secure Debug with Lock/Unlock | X | X |
| DPA Countermeasures | X | X |
| Secure Key Management with PUF | | X |
| Anti-Tamper | | X |
| Secure Attestation | | X |

#### 3.5.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

### 3.5.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192, P-256, P-384, and P-521 for Elliptic Curve Diffie-Hellman (ECDH) key derivation, and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for Edwards-curve Digital Signature Algorithm (EdDSA) sign and verify operations.

Secure Vault also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE) and Password-Based Key Derivation Function 2 (PBKDF2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

### 3.5.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

### 3.5.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

### 3.5.5 Differential Power Analysis (DPA) Countermeasures

The AES and ECC accelerators have DPA countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

### 3.5.6 Secure Key Management with Physically Unclonable Function (PUF)

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a PUF to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

### 3.5.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

### 3.5.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

# 4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A$=25 °C and VDD supply at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

## 4.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -50 | — | +150 | °C |
| Voltage on any supply pin | $V_{DDMAX}$ | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on VDD supply pin | $V_{DDRAMPMAX}$ | | — | — | 1.0 | V / µs |
| DC voltage on any GPIO pin | $V_{DIGPIN}$ | | -0.3 | — | $V_{IOVDD}$ + 0.3 | V |
| DC voltage on RESETn pin[1] | $V_{RESETn}$ | | -0.3 | — | 3.8 | V |
| Total current into VDD power lines | $I_{VDDMAX}$ | Source | — | — | 200 | mA |
| Total current into GND pin | $I_{GNDMAX}$ | Sink | — | — | 200 | mA |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |

**Note:**

1. The RESETn pin has a pull-up device to the VDD supply. For minimum leakage, RESETn should not exceed the voltage at VDD.

### 4.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specifed over this operating range, unless otherwise noted.

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating ambient temperature range | $T_A$ | -I temperature grade | -40 | — | +125 | ° C |
| VDD Supply Voltage | $V_{DD}$ | | 1.71 | 3.0 | 3.8 | V |
| IOVDD operating supply voltage (All IOVDD pins) | $V_{IOVDD}$ | | 1.71 | 3.0 | 3.8 | V |
| HCLK and Core frequency | $f_{HCLK}$ | MODE = WS1, RAMWSEN = 1[1] | — | — | 80 | MHz |
| | | MODE = WS1, RAMWSEN = 0[1] | — | — | 50 | MHz |
| | | MODE = WS0, RAMWSEN = 0[1] | — | — | 39 | MHz |
| PCLK frequency | $f_{PCLK}$ | | — | — | 50 | MHz |
| EM01 Group A clock frequency | $f_{EM01GRPACLK}$ | | — | — | 80 | MHz |
| HCLK Radio frequency | $f_{HCLKRADIO}$ | | — | 38.4 | — | MHz |
| External Clock Input | $f_{CLKIN}$ | VSCALE2 or VSCALE1, IOVDD ≥ 2.7 V | — | — | 40 | MHz |
| DPLL Reference Clock | $f_{DPLLREFCLK}$ | VSCALE2 or VSCALE1 | — | — | 40 | MHz |

**Note:**

1. Flash wait states are set by the MODE field in the MSC_READCTRL register. RAM wait states are enabled by setting the RAMWSEN bit in the SYSYCFG_DMEM0RAMCTRL register.

### 4.3 MCU Current Consumption at 3.0V

Unless otherwise indicated, typical conditions are: VDD = 3.0 V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.3. MCU Current Consumption at 3.0V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled[1] | $I_{ACTIVE}$ | 80 MHz HFRCO, CPU running Prime from flash | — | 50.9 | — | µA/MHz |
| | | 80 MHz HFRCO, CPU running while loop from flash | — | 45.6 | 55.5 | µA/MHz |
| | | 80 MHz HFRCO, CPU running CoreMark loop from flash | — | 59.8 | — | µA/MHz |
| | | 38.4 MHz crystal, CPU running while loop from flash | — | 63.8 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled[1] | $I_{EM1}$ | 80 MHz HFRCO | — | 28.7 | 37.6 | µA/MHz |
| | | 38.4 MHz crystal | — | 46.9 | — | µA/MHz |
| Current consumption in EM2 mode | $I_{EM2}$ | Full RAM retention and RTC running from LFXO (Bluetooth Stack not running) | — | 5.1 | — | µA |
| | | Full RAM retention, RTCC running, and Bluetooth Stack running from LFXO | — | 8.5 | — | µA |
| | | 1 bank (16 kB) RAM retention and RTC running from LFRCO | — | 4.5 | 10.5 | µA |
| Current consumption in EM3 mode | $I_{EM3}$ | Full RAM retention and RTC running from ULFRCO | — | 4.8 | 11.4 | µA |
| | | 1 bank (16 kB) RAM retention and RTC running from ULFRCO | — | 4.3 | — | µA |
| Current consumption in EM4 mode | $I_{EM4}$ | No BURTC, no LF oscillator | — | 0.21 | 0.5 | µA |
| Current consumption during reset | $I_{RST}$ | Hard pin reset held | — | 146 | — | µA |
| Current consumption per retained 16kB RAM bank in EM2 | $I_{RAM}$ | | — | 0.10 | — | µA |

**Note:**

1. The typical EM0/EM1 current measurement includes some current consumed by the security core for periodical housekeeping purposes. This does not include current consumed by user-triggered security operations, such as cryptographic calculations.

### 4.4 Radio Current Consumption at 3.0V

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VDD = 3.0V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.4. Radio Current Consumption at 3.0V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception | $I_{RX\_ACTIVE}$ | 125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.3 | — | mA |
| | | 500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.3 | — | mA |
| | | 1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.3 | — | mA |
| | | 2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.9 | — | mA |
| | | 802.15.4 receiving frame, f = 2.4 GHz, ZigBee stack running | — | 9.4 | — | mA |
| Current consumption in receive mode, Stack running | $I_{RX\_LISTEN}$ | 125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.1 | — | mA |
| | | 500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.1 | — | mA |
| | | 1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running | — | 9.1 | — | mA |
| | | 2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooh stack running | — | 9.8 | — | mA |
| | | 802.15.4, f = 2.4 GHz, ZigBee stack running | — | 9.2 | — | mA |
| Current consumption in transmit mode | $I_{TX}$ | f = 2.4 GHz, CW, 10 dBm Module, 0 dBm output power | — | 16.1 | — | mA |
| | | f = 2.4 GHz, CW, 10 dBm Module, 10 dBm output power | — | 34.1 | — | mA |
| | | f = 2.4 GHz, CW, 20 dBm Module, 10 dBm output power, VDD = 3.0 V | — | 59.7 | — | mA |
| | | f = 2.4 GHz, CW, 20 dBm Module, $P_{OUT}$ = 19.6 dBm, VDD = 3.3 V[1] | — | 181.3 | — | mA |
| | | f = 2.4 GHz, CW, 20 dBm Module, $P_{OUT}$ =19.2 dBm, VDD = 3.3 V [2] | — | 173 | — | mA |

**Note:**

1. The maximum power for when not using Bluetooth Low-Energy is limited to 19.6 dBm.
2. The maximum power for Bluetooth Low-Energy is limited to 19.2 dBm.

### 4.5 RF Transmitter General Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. Measured with RF center frequency of 2.45 GHz on RF2G4_IO2 port.

**Table 4.5. RF Transmitter General Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |
| Maximum TX output power [1] | $POUT_{MAX}$ | 20 dBm Module, VDD = 3.3V[2] | — | 19.6 | — | dBm |
| | | 20 dBm Module, BLE, VDD = 3.3V[3] | — | 19.2 | — | dBm |
| | | 10 dBm Module | — | 10 | — | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | 20 dBm Module, VDD = 3.3 V | — | -20.5 | — | dBm |
| | | 10 dBm Module | — | -19.3 | — | dBm |
| Output power step size | $POUT_{STEP}$ | 10 dBm Module, -5 dBm < $P_{OUT}$ < 0 dBm | — | 1.5 | — | dB |
| | | 10 dBm Module, 0 dBm < $P_{OUT}$ < 10 dBm | — | 1.0 | — | dB |
| | | 20 dBm Module, 0 dBm < $P_{OUT}$ < 5 dBm | — | 0.7 | — | dB |
| | | 20 dBm Module, 5 dBm < $P_{OUT}$ < $POUT_{MAX}$ | — | 0.5 | — | dB |
| Output power variation vs VDD supply voltage, Freq = 2450MHz | $POUT_{VAR\_V}$ | 20 dBm Module, $P_{OUT}$ = $POUT_{MAX}$ VDD swept from 3.0V to 3.8V. | — | 1.0 | — | dB |
| | | 10 dBm Module, $P_{OUT}$ = $POUT_{MAX}$ VDD swept from 1.8V to 3.0V. | — | 0.2 | — | dB |
| Output power variation vs temperature, Freq = 2450MHz | $POUT_{VAR\_T}$ | 20 dBm Module, $P_{OUT}$ = $POUT_{MAX}$, VDD = 3.3V, temperature swept from -40 to +125 °C. | — | 1.5 | — | dB |
| | | 10 dBm Module, $P_{OUT}$ = $POUT_{MAX}$, VDD = 3.0V, temperature swept from -40 to +125 °C. | — | 0.3 | — | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | 20 dBm Module, $P_{OUT}$ = $POUT_{MAX}$, VDD = 3.3V, Freq. swept from 2400 to 2483.5 MHz | — | 0.2 | — | dB |
| | | 10 dBm Module, $P_{OUT}$ = $POUT_{MAX}$, VDD = 3.0V, Freq. swept from 2400 to 2483.5 MHz | — | 0.2 | — | dB |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the TX Power column of the Ordering Information Table.
2. The maximum power when not using Bluetooth Low-Energy.
3. The maximum power for Bluetooth Low-Energy.

### 4.6 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. Measured with RF center frequency of 2.45 GHz on RF2G4_IO2 port.

**Table 4.6. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error vector magnitude per 802.15.4-2011 | EVM | 20 dBm Module, Average across frequency, signal is DSSS-OQPSK reference packet, VDD = 3.3 V, $P_{out}$ = $POUT_{MAX}$ | — | 2.7 | — | % rms |
| | | 10 dBm Module, Average across frequency, signal is DSSS-OQPSK reference packet, $P_{out}$ = 10 dBm | — | 2.7 | — | % rms |

### 4.7 RF Receiver General Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. Measured with RF center frequency of 2.45 GHz on RF2G4_IO2 port.

**Table 4.7. RF Receiver General Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |

### 4.8 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz. Measured on RF2G4_IO2.

**Table 4.8. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rx Max Strong Signal Input Level for 1% PER | $RX_{SAT}$ | Signal is reference signal[1], packet length is 20 octets | — | 10 | — | dBm |
| Co-channel interferer rejection, 1% PER | CCR | Desired signal 3 dB above sensitivity limit | — | -0.2 | — | dB |
| Sensitivity, 1% PER | SENS | Signal is reference signal, packet length is 20 octets | — | -103.9 | — | dBm |
| Image rejection, 1% PER, desired is reference signal at 3 dB above reference sensitivity level[2] | IR | Interferer is CW in image band[3] | — | 43.5 | — | dB |
| Blocking rejection of all other channels, 1% PER, desired is reference signal at 3 dB above reference sensitivity level[2], interferer is reference signal | BLOCK | Interferer frequency < desired frequency -3 channel spacing | — | 57.6 | — | dB |
| | | Interferer frequency > desired frequency +3 channel spacing | — | 57.5 | — | dB |
| RSSI resolution | $RSSI_{RES}$ | -100 dBm to +5 dBm | — | 0.25 | — | dB |
| RSSI accuracy in the linear region as defined by 802.15.4-2003 | $RSSI_{LIN}$ | | — | +/-6 | — | dB |
| Adjacent channel rejection, Interferer is reference signal, 1% PER, desired is reference signal at 3 dB above reference sensitivity level[2] | $ACR_{REF1}$ | Interferer is reference signal at +1 channel spacing | — | 39.9 | — | dB |
| | | Interferer is reference signal at -1 channel spacing | — | 39.2 | — | dB |
| Alternate channel rejection, interferer is reference signal, 1% PER, desired is reference signal at 3 dB above reference sensitivity level[2] | $ACR_{REF2}$ | Interferer is reference signal at +2 channel spacing | — | 51.1 | — | dB |
| | | Interferer is reference signal at -2 channel spacing | — | 51.6 | — | dB |

**Note:**

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

### 4.9 RF Receiver Characteristics for Bluetooth Low Energy at 1 Mbps

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz. Measured on RF2G4_IO2.

**Table 4.9. RF Receiver Characteristics for Bluetooth Low Energy at 1 Mbps**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Signal is reference signal, packet length is 37 bytes[1] | — | 10 | — | dBm |
| Sensitivity | SENS | Signal is reference signal, 37 byte payload[1] | — | -97.0 | — | dBm |
| | | With non-ideal signals[2 1] | — | -96.7 | — | dBm |
| Signal to co-channel interferer | $C/I_{CC}$ | (see notes)[1 3] | — | +6.6 | — | dB |
| N ± 1 Adjacent channel selectivity | $C/I_1$ | Interferer is reference signal at +1 MHz offset[1 4 3 5] | — | -8.3 | — | dB |
| | | Interferer is reference signal at -1 MHz offset[1 4 3 5] | — | -8.7 | — | dB |
| N ± 2 Alternate channel selectivity | $C/I_2$ | Interferer is reference signal at +2 MHz offset[1 4 3 5] | — | -42.1 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[1 4 3 5] | — | -48.9 | — | dB |
| N ± 3 Alternate channel selectivity | $C/I_3$ | Interferer is reference signal at +3 MHz offset[1 4 3 5] | — | -42.4 | — | dB |
| | | Interferer is reference signal at -3 MHz offset[1 4 3 5] | — | -54.8 | — | dB |
| Selectivity to image frequency | $C/I_{IM}$ | Interferer is reference signal at image frequency with 1 MHz precision[1 5] | — | -42.1 | — | dB |
| Selectivity to image frequency ± 1 MHz | $C/I_{IM\_1}$ | Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5] | — | -42.4 | — | dB |
| | | Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5] | — | -8.3 | — | dB |
| Intermodulation performance | IM | n = 3 [6] | — | -23 | — | dBm |

**Note:**

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

### 4.10 RF Receiver Characteristics for Bluetooth Low Energy at 2 Mbps

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz. Measured on RF2G4_IO2.

**Table 4.10. RF Receiver Characteristics for Bluetooth Low Energy at 2 Mbps**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | SAT | Signal is reference signal, packet length is 37 bytes[1] | — | 10 | — | dBm |
| Sensitivity | SENS | Signal is reference signal, 37 byte payload[1] | — | -94.1 | — | dBm |
| | | With non-ideal signals[2 1] | — | -93.9 | — | dBm |
| Signal to co-channel interferer | $C/I_{CC}$ | (see notes)[1 3] | — | +6.0 | — | dB |
| N ± 1 Adjacent channel selectivity | $C/I_1$ | Interferer is reference signal at +2 MHz offset[1 4 3 5] | — | -8.0 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[1 4 3 5] | — | -8.8 | — | dB |
| N ± 2 Alternate channel selectivity | $C/I_2$ | Interferer is reference signal at +4 MHz offset[1 4 3 5] | — | -42.2 | — | dB |
| | | Interferer is reference signal at -4 MHz offset[1 4 3 5] | — | -50.3 | — | dB |
| N ± 3 Alternate channel selectivity | $C/I_3$ | Interferer is reference signal at +6 MHz offset[1 4 3 5] | — | -54.4 | — | dB |
| | | Interferer is reference signal at -6 MHz offset[1 4 3 5] | — | -55.4 | — | dB |
| Selectivity to image frequency | $C/I_{IM}$ | Interferer is reference signal at image frequency with 1 MHz precision[1 5] | — | -8.0 | — | dB |
| Selectivity to image frequency ± 1 MHz | $C/I_{IM\_1}$ | Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 5] | — | -42.2 | — | dB |
| | | Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 5] | — | +6.0 | — | dB |
| Intermodulation performance | IM | n = 3[6] | — | -22.3 | — | dBm |

**Note:**

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

### 4.11 RF Receiver Characteristics for Bluetooth Low Energy at 500 kbps

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz. Measured on RF2G4_IO2.

**Table 4.11. RF Receiver Characteristics for Bluetooth Low Energy at 500 kbps**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | SAT | Signal is reference signal, packet length is 37 bytes[1] | — | 10 | — | dBm |
| Sensitivity | SENS | Signal is reference signal[1] | — | -100.1 | — | dBm |
| | | With non-ideal signals[2 1] | — | -99.3 | — | dBm |
| Signal to co-channel interferer | $C/I_{CC}$ | (see notes)[1 3] | — | +2.1 | — | dB |
| N ± 1 Adjacent channel selectivity | $C/I_1$ | Interferer is reference signal at +1 MHz offset[1 4 3 5] | — | -9.0 | — | dB |
| | | Interferer is reference signal at -1 MHz offset[1 4 3 5] | — | -9.5 | — | dB |
| N ± 2 Alternate channel selectivity | $C/I_2$ | Interferer is reference signal at +2 MHz offset[1 4 3 5] | — | -44.4 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[1 4 3 5] | — | -51.9 | — | dB |
| N ± 3 Alternate channel selectivity | $C/I_3$ | Interferer is reference signal at +3 MHz offset[1 4 3 5] | — | -44.3 | — | dB |
| | | Interferer is reference signal at -3 MHz offset[1 4 3 5] | — | -58.3 | — | dB |
| Selectivity to image frequency | $C/I_{IM}$ | Interferer is reference signal at image frequency with 1 MHz precision[1 5] | — | -44.4 | — | dB |
| Selectivity to image frequency ± 1 MHz | $C/I_{IM\_1}$ | Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5] | — | -44.3 | — | dB |
| | | Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5] | — | -9.0 | — | dB |

**Note:**

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -72 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

### 4.12 RF Receiver Characteristics for Bluetooth Low Energy at 125 kbps

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VDD = 3.0V. RF center frequency 2.45 GHz. Measured on RF2G4_IO2.

**Table 4.12. RF Receiver Characteristics for Bluetooth Low Energy at 125 kbps**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level | SAT | Signal is reference signal, packet length is 37 bytes[1] | — | 10 | — | dBm |
| Sensitivity | SENS | Signal is reference signal[1] | — | -104.5 | — | dBm |
| | | With non-ideal signals[2 1] | — | -104.2 | — | dBm |
| Signal to co-channel interferer | $C/I_{CC}$ | (see notes)[1 3] | — | +0.8 | — | dB |
| N ± 1 Adjacent channel selectivity | $C/I_1$ | Interferer is reference signal at +1 MHz offset[1 4 3 5] | — | -13.1 | — | dB |
| | | Interferer is reference signal at -1 MHz offset[1 4 3 5] | — | -13.6 | — | dB |
| N ± 2 Alternate channel selectivity | $C/I_2$ | Interferer is reference signal at +2 MHz offset[1 4 3 5] | — | -49.5 | — | dB |
| | | Interferer is reference signal at -2 MHz offset[1 4 3 5] | — | -56.9 | — | dB |
| N ± 3 Alternate channel selectivity | $C/I_3$ | Interferer is reference signal at +3 MHz offset[1 4 3 5] | — | -47.0 | — | dB |
| | | Interferer is reference signal at -3 MHz offset[1 4 3 5] | — | -63.1 | — | dB |
| Selectivity to image frequency | $C/I_{IM}$ | Interferer is reference signal at image frequency with 1 MHz precision[1 5] | — | -49.5 | — | dB |
| Selectivity to image frequency ± 1 MHz | $C/I_{IM\_1}$ | Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5] | — | -47.0 | — | dB |
| | | Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5] | — | -13.1 | — | dB |

**Note:**

1. 0.1% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -79 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

### 4.13 High-Frequency Crystal

**Table 4.13. High-Frequency Crystal**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal frequency | $f_{HFXTAL}$ | | — | 38.4 | — | MHz |
| Initial calibrated accuracy | $ACC_{HFXTAL}$ | | -10 | — | +10 | ppm |
| Temperature drift | $DRIFT_{HFXTAL}$ | Across specified temperature range | -30 | — | +30 | ppm |

### 4.14 Low Frequency Crystal Oscillator

**Table 4.14. Low Frequency Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $F_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported Crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | GAIN = 0 | — | — | 80 | kΩ |
| | | GAIN = 1 to 3 | — | — | 100 | kΩ |
| Supported range of crystal load capacitance [1] | $C_{L\_LFXO}$ | GAIN = 0 | 4 | — | 6 | pF |
| | | GAIN = 1 | 6 | — | 10 | pF |
| | | GAIN = 2 (see note[2]) | 10 | — | 12.5 | pF |
| | | GAIN = 3 (see note[2]) | 12.5 | — | 18 | pF |
| Current consumption | $I_{CL12p5}$ | ESR = 70 kΩ, $C_L$ = 12.5 pF, GAIN[3] = 2, AGC[4] = 1 | — | 357 | — | nA |
| Startup Time | $T_{STARTUP}$ | ESR = 70 kΩ, $C_L$ = 7 pF, GAIN[3] = 1, AGC[4] = 1 | — | 63 | — | ms |
| On-chip tuning cap step size | $SS_{LFXO}$ | | — | 0.26 | — | pF |
| On-chip tuning capacitor value at minimum setting[5] | $C_{LFXO\_MIN}$ | CAPTUNE = 0 | — | 4 | — | pF |
| On-chip tuning capacitor value at maximum setting[5] | $C_{LFXO\_MAX}$ | CAPTUNE = 0x4F | — | 24.5 | — | pF |

**Note:**

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

### 4.15 GPIO Pins

Unless otherwise indicated, typical conditions are: VDD = IOVDD = 3.0 V.

**Table 4.15. GPIO Pins**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Leakage current | $I_{LEAK\_IO}$ | MODEx = DISABLED, IOVDD = 1.71V | — | 1.9 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.0 V | — | 2.5 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V $T_A$ = 125 °C | — | — | 200 | nA |
| Input low voltage[1] | $V_{IL}$ | Any GPIO pin | — | — | 0.3 * IOVDD | V |
| Input high voltage[1] | $V_{IH}$ | Any GPIO pin | 0.7 * IOVDD | — | — | V |
| Output low voltage | $V_{OL}$ | Sinking 20mA, IOVDD = 3.0 V | — | — | 0.2 * IOVDD | V |
| | | Sinking 8mA, IOVDD = 1.71 V | — | — | 0.4 * IOVDD | V |
| Output high voltage | $V_{OH}$ | Sourcing 20mA, IOVDD = 3.0 V | 0.8 * IOVDD | — | — | V |
| | | Sourcing 8mA, IOVDD = 1.71 V | 0.6 * IOVDD | — | — | V |
| GPIO rise time | $T_{GPIO\_RISE}$ | IOVDD = 3.0V, $C_{load}$ = 50pF, SLEWRATE = 4, 10% to 90% | — | 8.4 | — | ns |
| | | IOVDD = 1.7V, $C_{load}$ = 50pF, SLEWRATE = 4, 10% to 90% | — | 13 | — | ns |
| GPIO fall time | $T_{GPIO\_FALL}$ | IOVDD = 3.0V, $C_{load}$ = 50pF, SLEWRATE = 4, 90% to 10% | — | 7.1 | — | ns |
| | | IOVDD = 1.7V, $C_{load}$ = 50pF, SLEWRATE = 4, 90% to 10% | — | 11.9 | — | ns |
| Pull up/down resistance[2] | $R_{PULL}$ | Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0. | 35 | 44 | 55 | kΩ |
| Maximum filtered glitch width | $T_{GF}$ | MODE = INPUT, DOUT = 1 | — | 26 | — | ns |
| RESETn low time to ensure pin reset | $T_{RESET}$ | | 100 | — | — | ns |

**Note:**

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to VDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to VDD.

### 4.16 Microcontroller Peripherals

The MCU peripherals set available in MGM210P modules includes:

- 12-bit 1 Msps ADC
- Analog Comparators
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- $I^2C$ peripheral interfaces
- 12 Channel Peripheral Reflex System

For details on their electrical performance, consult the relevant portions of Section 4 in the SoC's datasheet.

To learn which GPIO ports provide access to every peripheral, consult Section 6.3 Analog Peripheral Connectivity and 6.4 Digital Peripheral Connectivity.

### 4.17 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

### 4.17.1 Antenna Radiation and Efficiency

Typical MGM210P radiation patterns and efficiency for the on-board chip antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.

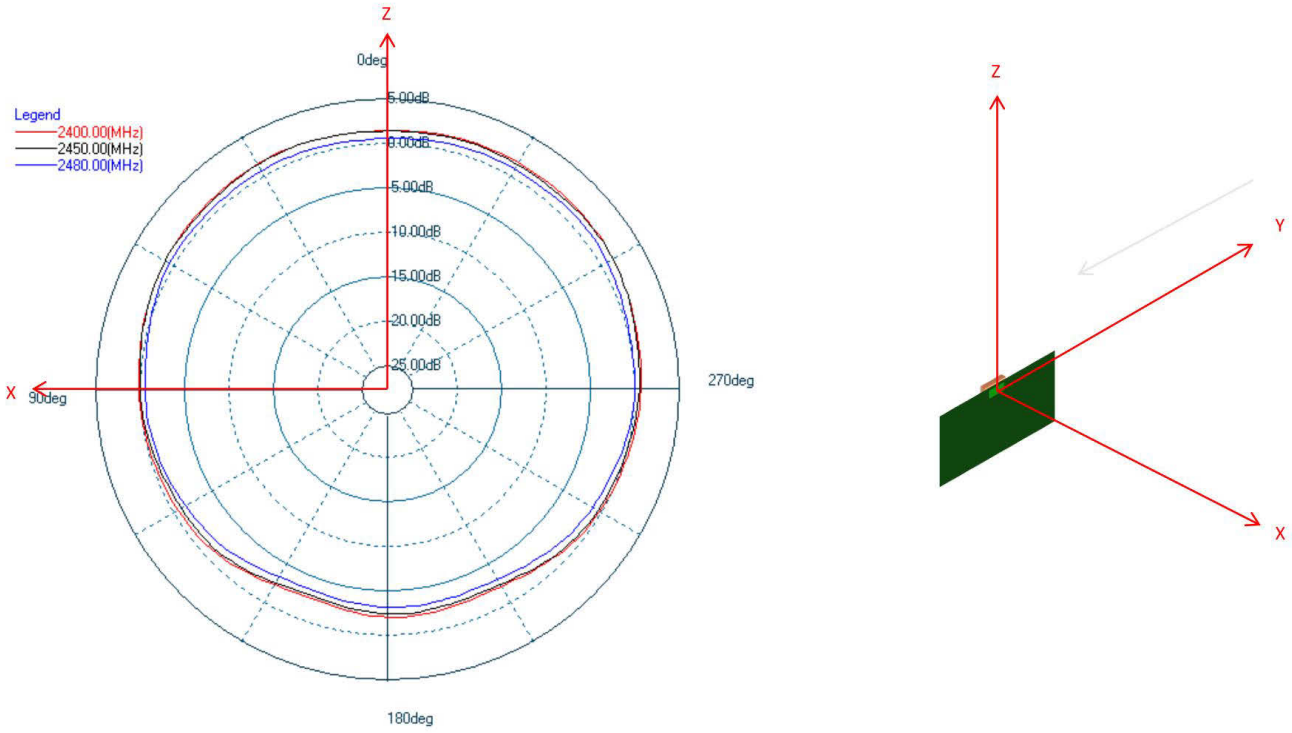


**Figure 4.1. Typical 2D Antenna Radiation Patterns - Phi 0$^{o}$ (Side View) Gain (dBi)**

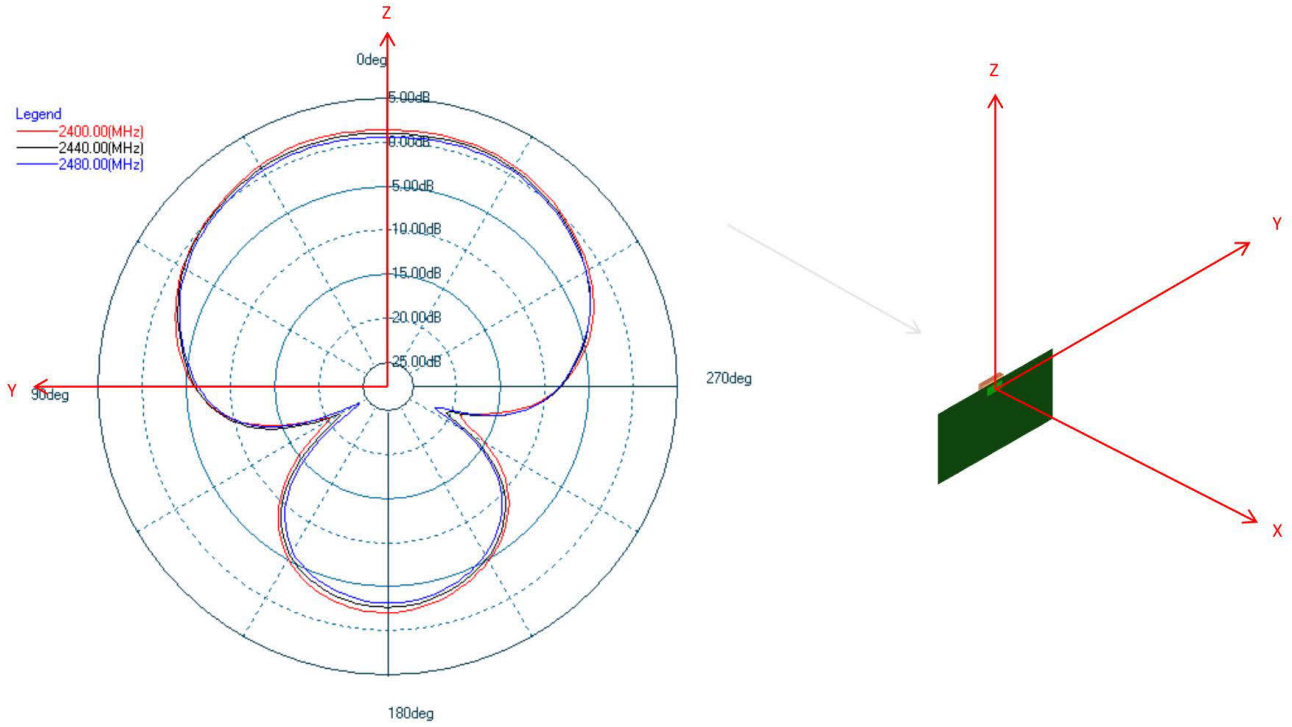


**Figure 4.2. Typical 2D Antenna Radiation Patterns - Phi 90$^{o}$ (Top View) Gain (dBi)**

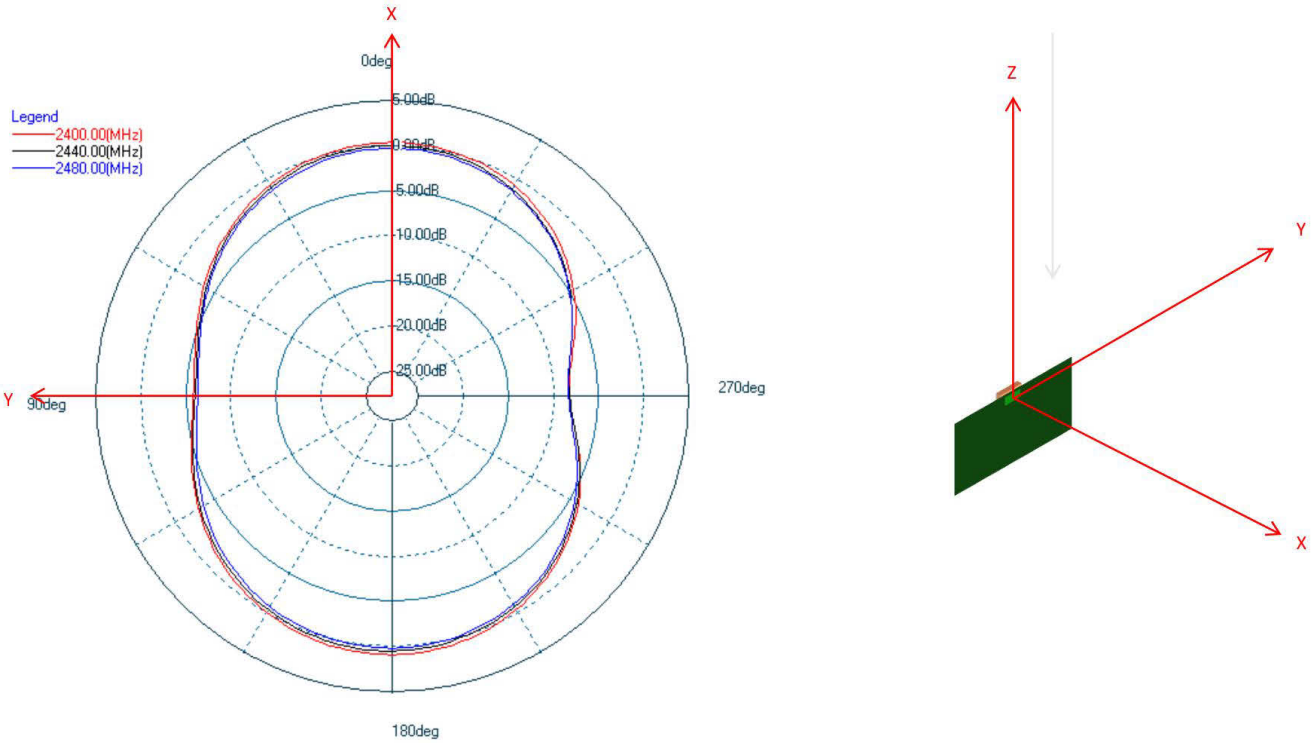


**Figure 4.3. Typical 2D Antenna Radiation Patterns - Theta 90$^{o}$ (Front View) Gain (dBi)**

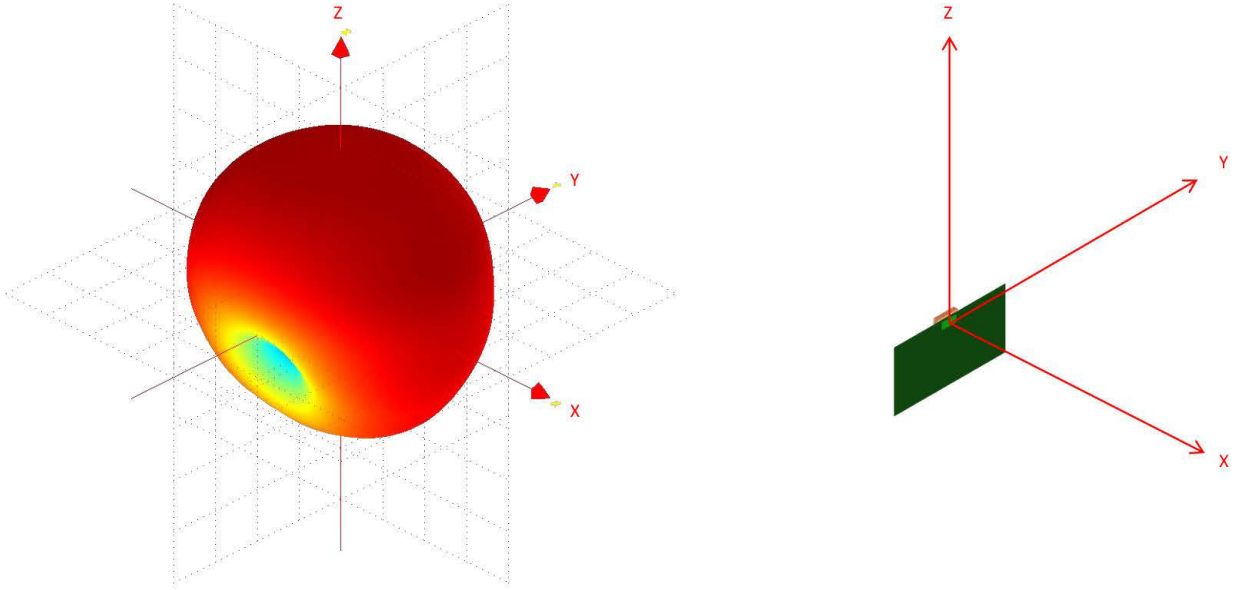


**Figure 4.4. 3D Radiation Pattern at 2440MHz**

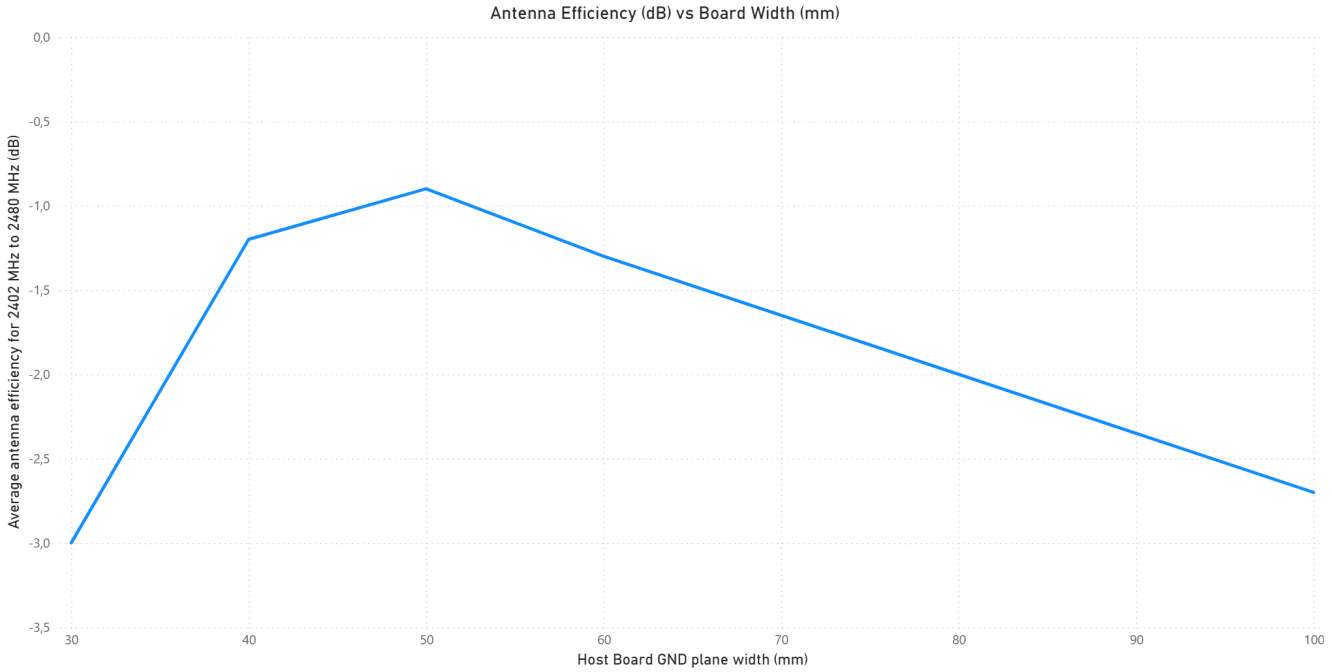


**Figure 4.5. Efficiency of the Built-in Antenna as Function of the Carrier Board Width (mm)**

# 5. Reference Diagrams

The interconnection labels in the following diagrams correspond to supported pin functions as described in Sections 7.5 Debug, 7.6 Packet Trace Interface (PTI) and 6.4 Digital Peripheral Connectivity.

## 5.1 Network Co-Processor (NCP) Application with UART Host

The MGM210P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, refer to *AN958: Debugging and Programming Interfaces for Custom Designs*. For an example of how to enable the virtual COM port (VCOM) when relevant, see radio board user guides UG388 or UG389.

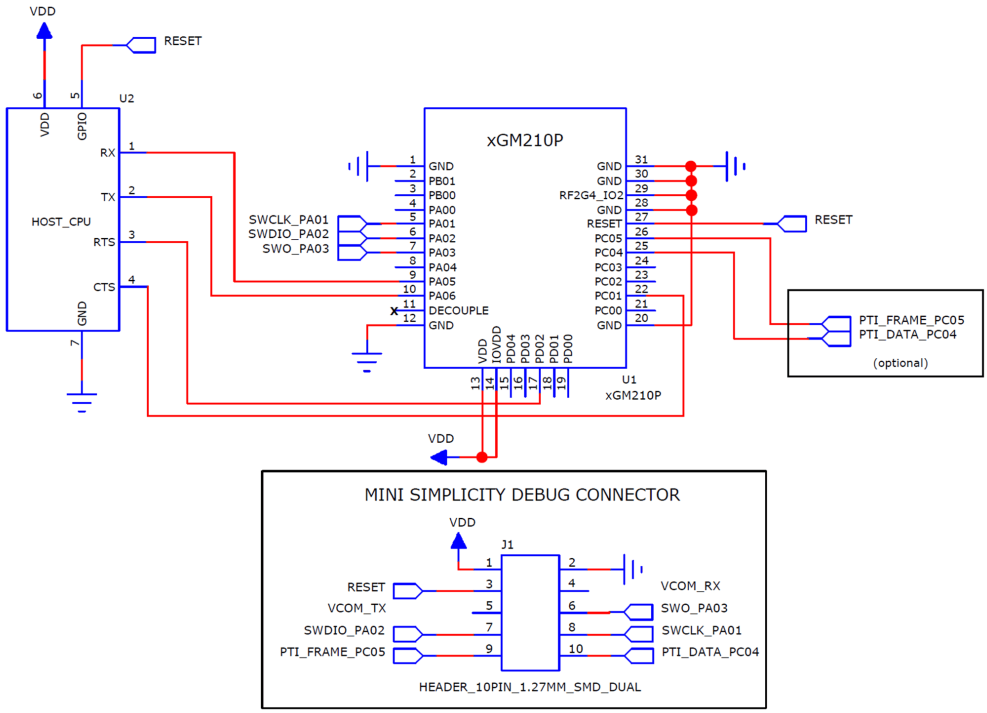


**Figure 5.1. UART NCP Configuration**

In systems where IOVDD is not equal to VDD, pin 1 of the mini simplicity debug connector should be connected to the IOVDD pin of the MGM210P module, and the module should be powered through an external power supply.

If the host CPU is operated at a different voltage level than the MGM210P, then IOVDD and pin 1 of the mini simplicity debug connector should be powered with the same voltage level as the host CPU or, else, an external voltage level shifter will be required.

## 5.2 SoC Application

The MGM210P can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, refer to *AN958: Debugging and Programming Interfaces for Custom Designs*. For an example of how to enable the virtual COM port (VCOM) when relevant, see radio board user guides UG388 or UG389.

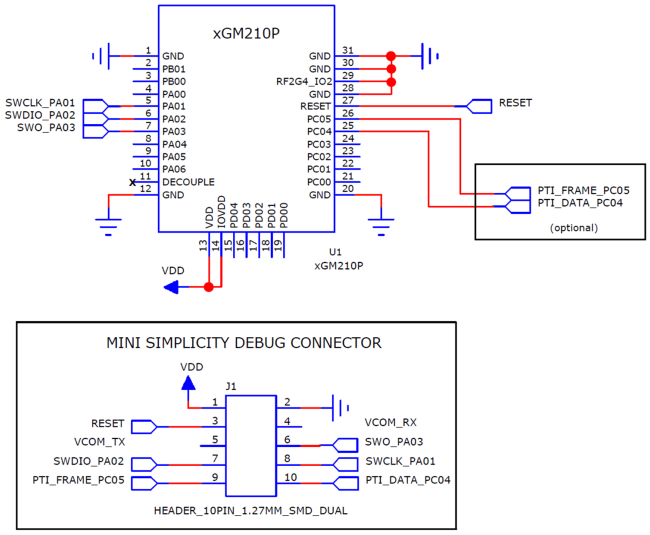


**Figure 5.2. Stand-Alone SoC Configuration**

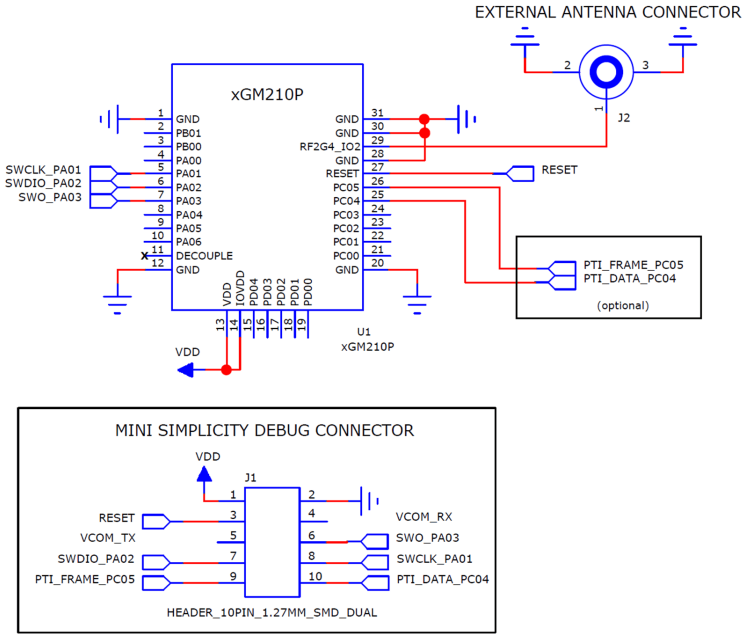


**Figure 5.3. Stand-Alone SoC Configuration with External Antenna**

**Note:** It is recommended to add an external low frequency crystal (LF XTAL) for Bluetooth operation.

# 6. Pin Definitions

## 6.1 Module Pinout

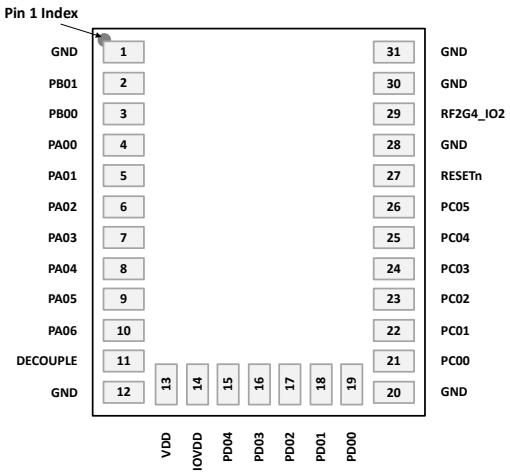


**Figure 6.1. MGM210P Module Pinout**

The next table shows the MGM210P pinout and general descriptions for each pin. Refer to Sections 6.2 Alternate Pin Functions, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity for details on functions and peripherals supported by GPIOs.

**Table 6.1. MGM210P Module Pin Definitions**

| Pin Name | No. | Description | Pin Name | No. | Description |
|---|---|---|---|---|---|
| GND | 1 | Ground | PB01 | 2 | GPIO |
| PB00 | 3 | GPIO | PA00 | 4 | GPIO |
| PA01 | 5 | GPIO | PA02 | 6 | GPIO |
| PA03 | 7 | GPIO | PA04 | 8 | GPIO |
| PA05 | 9 | GPIO | PA06 | 10 | GPIO |
| DECOUPLE | 11 | Decouple output for on-chip voltage regulator. **Do Not Connect** [3]. | GND | 12 | Ground |
| VDD | 13 | Power supply | IOVDD | 14 | Digital IO power supply |
| PD04 | 15 | GPIO | PD03 | 16 | GPIO |
| PD02 | 17 | GPIO | PD01 | 18 | GPIO |
| PD00 | 19 | GPIO | GND | 20 | Ground |
| PC00 | 21 | GPIO | PC01 | 22 | GPIO |
| PC02 | 23 | GPIO | PC03 | 24 | GPIO |
| PC04 | 25 | GPIO | PC05 | 26 | GPIO |
| RESETn | 27 | Reset Pin[1] | GND | 28 | Ground |
| RF2G4_IO2 | 29 | 2.4 GHz RF input/output[2] | GND | 30 | Ground |
| GND | 31 | Ground | | | |

| Pin Name | No. | Description | Pin Name | No. | Description |
|---|---|---|---|---|---|

**Note:**

1. Connected to pull-up resistor to VDD internally. External pull-up is not required.
2. 50 Ohm-matched RF pin for external antenna support. Connect to GND when not used.
3. The DECOUPLE pin exposes the SoC's on-chip digital supply regulator output and allows introducing an external digital supply source via a PMIC, for example. The default recommendation is to leave the DECOUPLE pin disconnected.

### 6.2 Alternate Pin Functions

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc.. The following table shows which module pins have alternate capabilities and the functions they support. Refer to the SoC's reference manual for more information.

**Table 6.2. GPIO Alternate Function Table**

| GPIO | Alternate Functions |
|---|---|
| PA00 | IADC0.VREFP |
| PA01 | GPIO.SWCLK |
| PA02 | GPIO.SWDIO |
| PA03 | GPIO.SWV |
| | GPIO.TDO |
| | GPIO.TRACEDATA0 |
| PA04 | GPIO.TDI |
| | GPIO.TRACECLK |
| PA05 | GPIO.EM4WU0 |
| PB01 | GPIO.EM4WU3 |
| PC00 | GPIO.EM4WU6 |
| PC05 | GPIO.EM4WU7 |
| PD00 | LFXO.LFXTAL_O |
| PD01 | LFXO.LFXTAL_I |
| | LFXO.LF_EXTCLK |
| PD02 | GPIO.EM4WU9 |

### 6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the SoC's Reference Manual for more details on the ABUS and analog peripherals.

**Table 6.3. ABUS Routing Table**

| Peripheral | Signal | PA | | PB | | PC | | PD | |
|---|---|---|---|---|---|---|---|---|---|
| | | EVEN | ODD | EVEN | ODD | EVEN | ODD | EVEN | ODD |
| ACMP0 | ana_neg | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ana_pos | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ACMP1 | ana_neg | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ana_pos | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| IADC0 | ana_neg | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ana_pos | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

### 6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are avaliable on each GPIO port.

**Table 6.4. DBUS Routing Table**

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| ACMP0.DIGOUT | Available | Available | Available | Available |
| ACMP1.DIGOUT | Available | Available | Available | Available |
| CMU.CLKIN0 | | | Available | Available |
| CMU.CLKOUT0 | | | Available | Available |
| CMU.CLKOUT1 | | | Available | Available |
| CMU.CLKOUT2 | Available | Available | | |
| FRC.DCLK | | | Available | Available |
| FRC.DFRAME | | | Available | Available |
| FRC.DOUT | | | Available | Available |
| I2C0.SCL | Available | Available | Available | Available |
| I2C0.SDA | Available | Available | Available | Available |
| I2C1.SCL | | | Available | Available |
| I2C1.SDA | | | Available | Available |
| LETIMER0.OUT0 | Available | Available | | |
| LETIMER0.OUT1 | Available | Available | | |
| PRS.ASYNCH0 | Available | Available | | |
| PRS.ASYNCH1 | Available | Available | | |
| PRS.ASYNCH10 | | | Available | Available |
| PRS.ASYNCH11 | | | Available | Available |
| PRS.ASYNCH2 | Available | Available | | |
| PRS.ASYNCH3 | Available | Available | | |
| PRS.ASYNCH4 | Available | Available | | |
| PRS.ASYNCH5 | Available | Available | | |
| PRS.ASYNCH6 | | | Available | Available |
| PRS.ASYNCH7 | | | Available | Available |
| PRS.ASYNCH8 | | | Available | Available |
| PRS.ASYNCH9 | | | Available | Available |
| PRS.SYNCH0 | Available | Available | Available | Available |
| PRS.SYNCH1 | Available | Available | Available | Available |
| PRS.SYNCH2 | Available | Available | Available | Available |
| PRS.SYNCH3 | Available | Available | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| TIMER0.CC0 | Available | Available | Available | Available |
| TIMER0.CC1 | Available | Available | Available | Available |
| TIMER0.CC2 | Available | Available | Available | Available |
| TIMER0.CDTI0 | Available | Available | Available | Available |
| TIMER0.CDTI1 | Available | Available | Available | Available |
| TIMER0.CDTI2 | Available | Available | Available | Available |
| TIMER1.CC0 | Available | Available | Available | Available |
| TIMER1.CC1 | Available | Available | Available | Available |
| TIMER1.CC2 | Available | Available | Available | Available |
| TIMER1.CDTI0 | Available | Available | Available | Available |
| TIMER1.CDTI1 | Available | Available | Available | Available |
| TIMER1.CDTI2 | Available | Available | Available | Available |
| TIMER2.CC0 | Available | Available | | |
| TIMER2.CC1 | Available | Available | | |
| TIMER2.CC2 | Available | Available | | |
| TIMER2.CDTI0 | Available | Available | | |
| TIMER2.CDTI1 | Available | Available | | |
| TIMER2.CDTI2 | Available | Available | | |
| TIMER3.CC0 | | | Available | Available |
| TIMER3.CC1 | | | Available | Available |
| TIMER3.CC2 | | | Available | Available |
| TIMER3.CDTI0 | | | Available | Available |
| TIMER3.CDTI1 | | | Available | Available |
| TIMER3.CDTI2 | | | Available | Available |
| USART0.CLK | Available | Available | Available | Available |
| USART0.CS | Available | Available | Available | Available |
| USART0.CTS | Available | Available | Available | Available |
| USART0.RTS | Available | Available | Available | Available |
| USART0.RX | Available | Available | Available | Available |
| USART0.TX | Available | Available | Available | Available |
| USART1.CLK | Available | Available | | |
| USART1.CS | Available | Available | | |
| USART1.CTS | Available | Available | | |
| USART1.RTS | Available | Available | | |
| USART1.RX | Available | Available | | |
| USART1.TX | Available | Available | | |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| USART2.CLK | | | Available | Available |
| USART2.CS | | | Available | Available |
| USART2.CTS | | | Available | Available |
| USART2.RTS | | | Available | Available |
| USART2.RX | | | Available | Available |
| USART2.TX | | | Available | Available |

# 7. Design Guidelines

## 7.1 Layout and Placement

For optimal performance of the MGM210P,

- Place the module aligned to the edge of the application PCB, as illustrated in the figures below.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB if you are going to use the on-board chip antenna
  - Antenna clearance area is not necessary if you are using an external antenna attached to the RF pin.
  - For external antenna use cases, use a 50 Ω grounded coplanar transmission line to trace the signal from the RF pin to an external RF connector if applicable (see Figure 7.2 Recommended Layout for MGM210P Using External Antenna on page 36).
  - A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency, which for 2.4 GHz is approximately 3.5 mm.
  - A U.FL connector can be used in the host PCB for the connection to an external antenna. The use of a U.FL connector is also recommended for conductive tests. The integrator must use a unique connector, such as a “reverse polarity SMA” or “reverse thread SMA”, if detachable antenna is offered with the host chassis. This is especially required for the FCC and ISED approvals to remain valid, and any other kind of direct connector to the antenna might require a permissive change.
  - A trace length of 2.6 mm was used in the certifications host board to connect the module RF pin to the U.FL connector.
  - For reference, Figure 7.4 RF Trace Design Example on page 37 shows a set of parameters for a 50 Ω trace. Trace impedance should always be matched to the particular stack-up used on the host board.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in contact with the antenna.

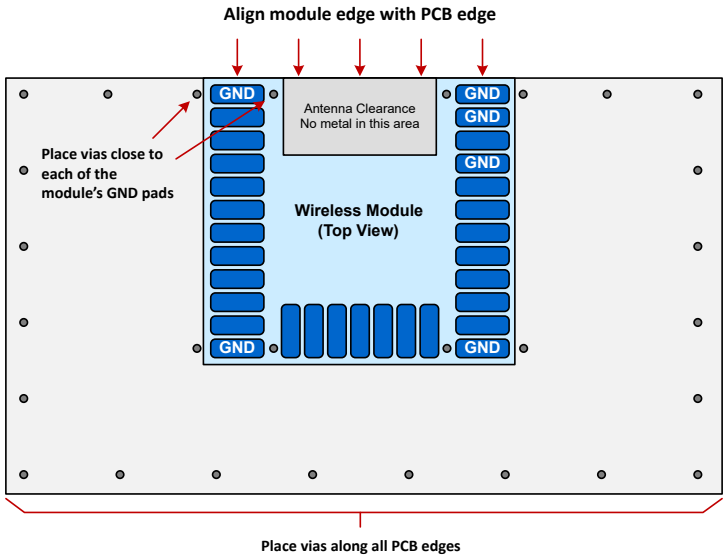


**Figure 7.1. Recommended Layout for MGM210P Using On-Board Chip Antenna**

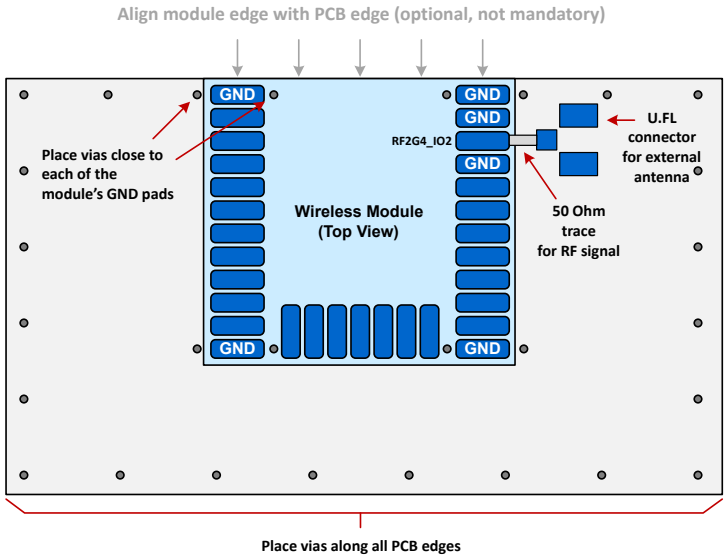


**Figure 7.2. Recommended Layout for MGM210P Using External Antenna**

The figure below illustrates layout scenarios to avoid that will lead to severely degraded RF performance for modules that use the on-board chip antenna. This recommendation is not applicable to design cases using an external antenna.

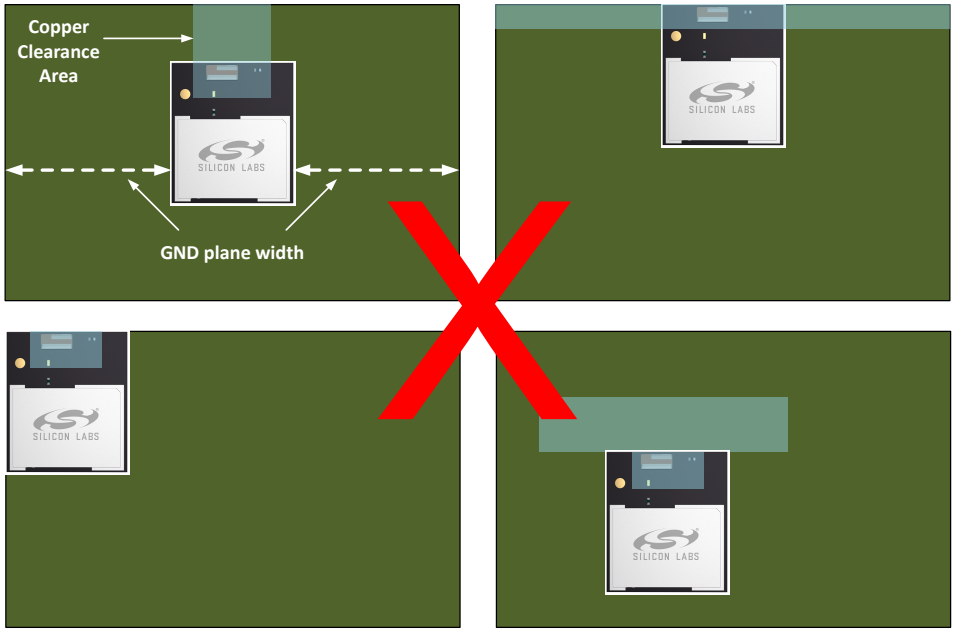


**Figure 7.3. Non-Optimal Layout Examples**

The width of the application PCB's GND plane under the module will impact the efficiency of the on-board chip antenna. To achieve optimal performance, a GND plane width of 50 mm is recommended. See Figure 4.1 Typical 2D Antenna Radiation Patterns - Phi 0º (Side View) Gain (dBi) on page 24 for reference.

| Lines | Parameters |
|---|---|
| f | 2.4 GHz |
| T | 0.018-0.035 mm |
| $\varepsilon_r$ | 4.6 |
| H | 0.325 mm |
| G | 0.25 mm |
| W | 0.45 mm |

**Notes:**

1. Characteristic impedance is not "super sensitive" to the gap value. It should be between 0.25 and 0.4 mm to have 47 through 53 Ω impedance.
2. Different impedance calculators may yield slightly different results.
3. *H* is the distance between the top and the first inner layer.

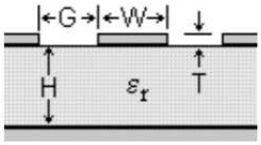


**Figure 7.4. RF Trace Design Example**

### 7.2 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

### 7.3 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

### 7.4 Reset

The MGM210P can be reset by pulling the RESET line low, by the internal watchdog timer, or by software command.

The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

### 7.5 Debug

See *AN958: Debugging and Programming Interfaces for Custom Designs*.

The MGM210P supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes. The table below lists the required pins for JTAG and SWD debug interfacing, which are also presented in Section 6.2 Alternate Pin Functions.

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

**Table 7.1. Debug Pins**

| Pin Name | Pin Number | JTAG Signal | SWD Signal | Comments |
|---|---|---|---|---|
| PA04 | 4 | TDI | N/A | This pin is disabled after reset. Once enabled the pin has a built-in pull-up. |
| PA03 | 3 | TDO | N/A | This pin is disabled after reset. |
| PA02 | 2 | TMS | SWDIO | Pin is enabled after reset and has a built-in pull-up. |
| PA01 | 1 | TCK | SWCLK | Pin is enabled after reset and has a built-in pull-down. |

### 7.6 Packet Trace Interface (PTI)

The MGM210P integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The PTI_DATA and PTI_FRAME signals can be accessed through any GPIO on ports C and D (see FRC.DOUT and FRC.DFRAME peripheral resources in Table 6.4 DBUS Routing Table on page 32).

# 8. Package Specifications

## 8.1 Package Outline

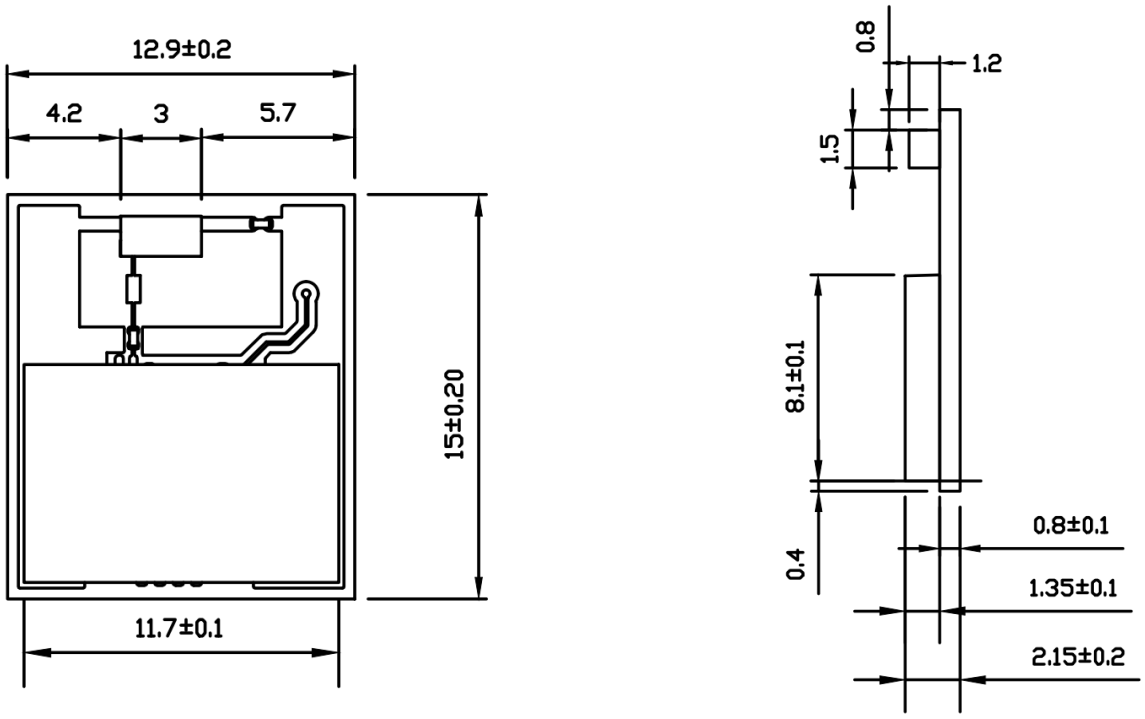


**Figure 8.1. Top and Side Views**

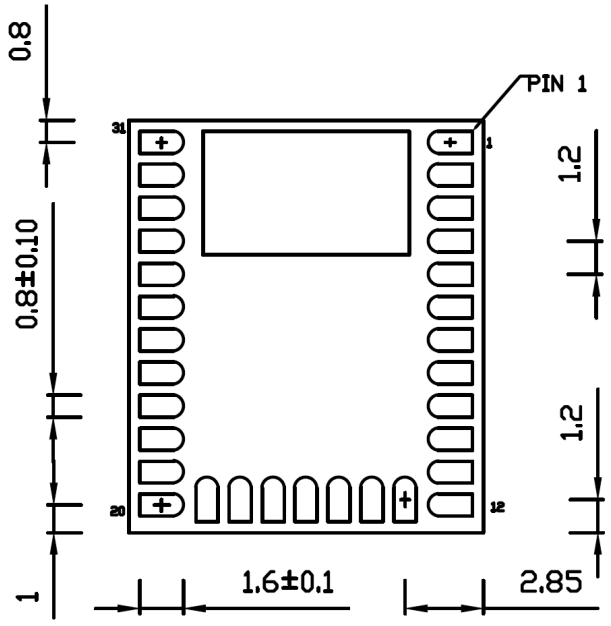


**Figure 8.2. Bottom View**

### 8.2 PCB Land Pattern

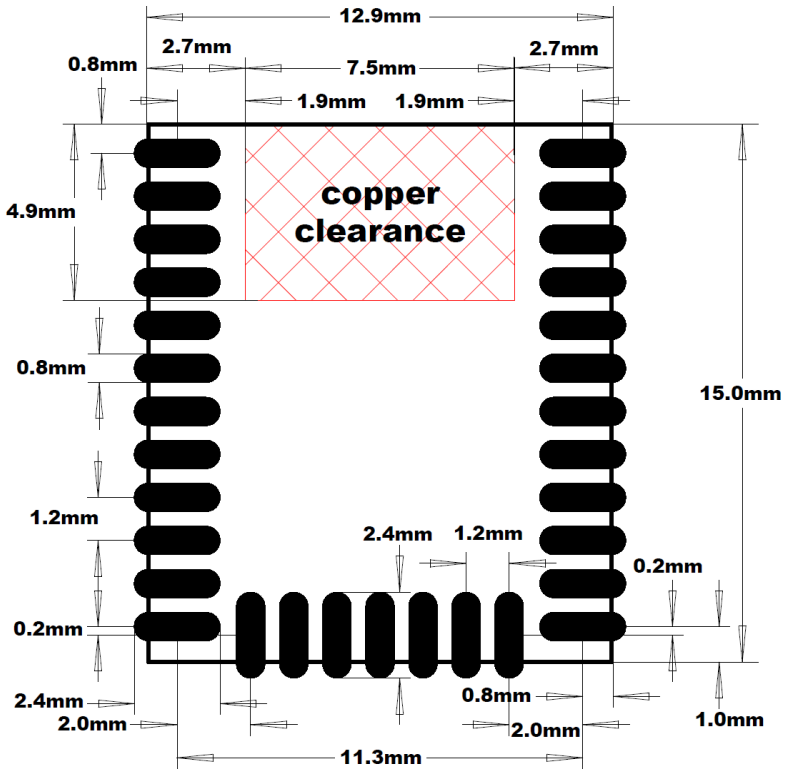


**Figure 8.3. Recommended Land Pattern for Built-in Antenna Use Case**

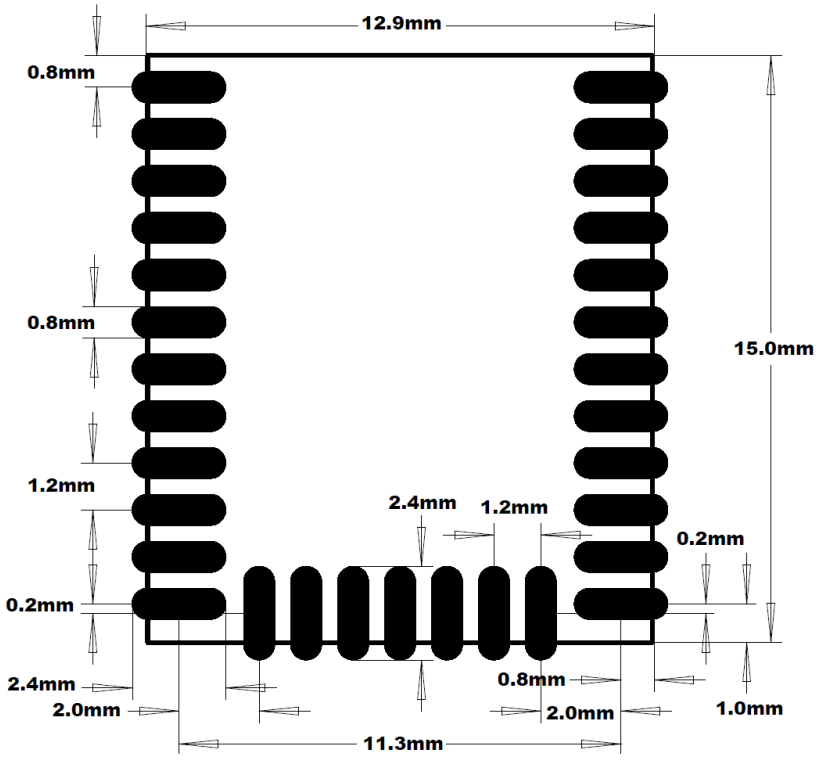


**Figure 8.4. Recommended Land Pattern for RF Pin Use Case**

### 8.3 Package Marking

The figure below shows the module markings engraved on the RF shield.

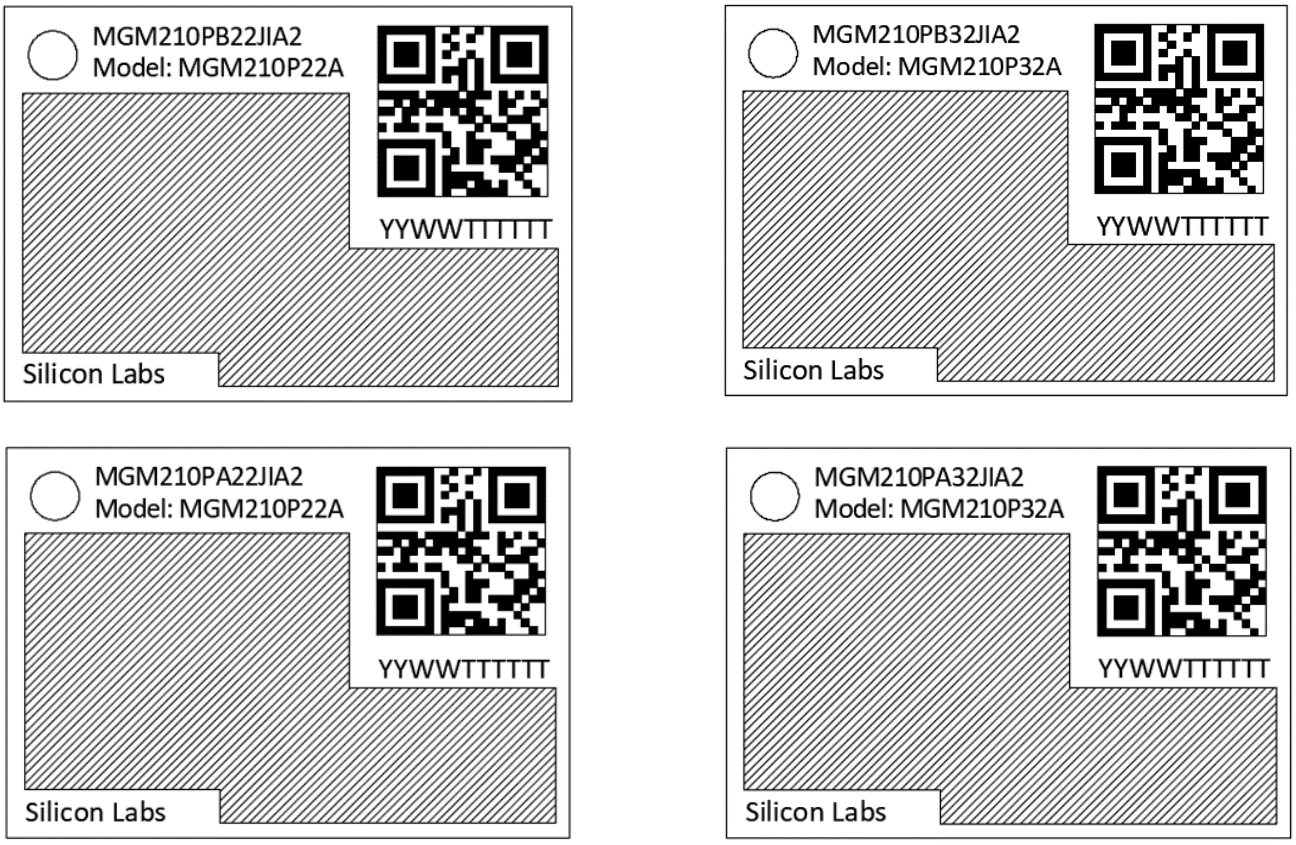


**Figure 8.5. MGM210P Top Marking**

**Mark Description**

The package marking consists of:

- MGM210Pxxxxxxx - Part number designation
- Model: MGM210Pxxx - Model number designation
- QR Code: YYWWMMABCDE
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – Manufacturing trace code. The first letter is the device revision
- Certification marks such as the CE logo, FCC and IC IDs, etc will be engraved on the grayed out area, according to regulatory body requirements

# 9. Soldering Recommendations

It is recommended that final PCB assembly of the MGM210P follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

**CLASS 1 General Electronic Products**

Includes products suitable for applications where the major requirement is function of the completed assembly.

**CLASS 2 Dedicated Service Electronic Products**

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

**CLASS 3 High Performance/Harsh Environment Electronic Products**

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

**Note:** General SMT application notes are provided in the AN1223 document.

# 10. Tape and Reel

## 10.1 Tape and Reel

MGM210P modules are delivered to the customer in cut tape (100 pcs) or reel (1000 pcs) packing with the dimensions below. All dimensions are given in mm unless otherwise indicated. Pin 1 is found in Quadrant 1 (upper left side of carrier) with respect to the direction of feed indicated by the arrow in the figure.

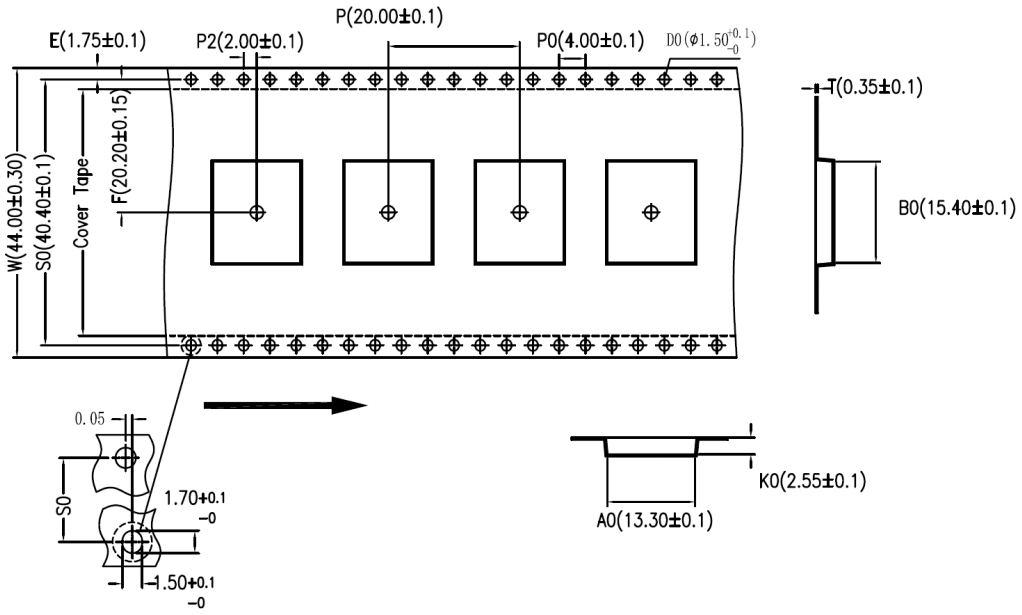


**Figure 10.1. Carrier Tape Dimensions**

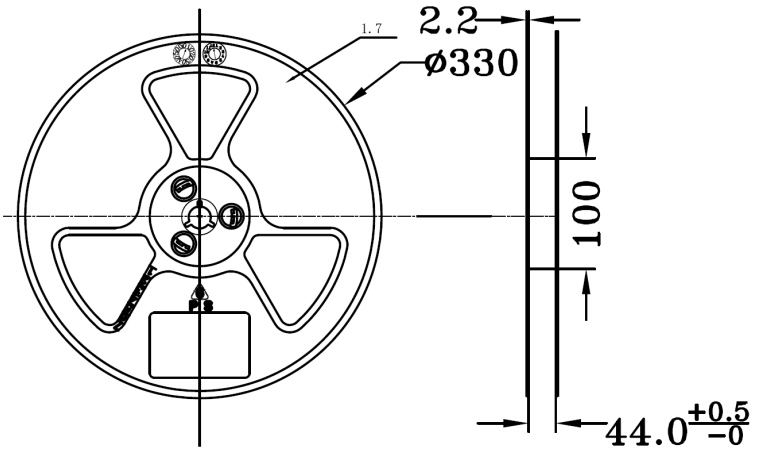


**Figure 10.2. Reel Dimensions**

## 10.2 Moisture Sensitivity Level

MGM210P modules are delivered in packing that conforms to moisture sensitivity level 3 (MSL3) requirements.

# 11. Certifications

This section details the regulatory certification status of the MGM210P modules in various regions. For certification purposes, the modules are mainly referred to by their formal Model Names of MGM210P32A and MGM210P22A.

The address of the modules' legal manufacturer and certification applicant is:

SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

The MGM210P32A and MGM210P22A modules have Brand Name of "SILICON LABS".

## 11.1 Qualified Antennas

MGM210P modules have been tested and certified both with the built-in antenna and with an external antenna attached to the RF pin (RF2G4_IO2). Performance characteristics for the built-in antenna are presented in Table 3.1 Antenna Efficiency and Peak Gain on page 6 and 4.17.1 Antenna Radiation and Efficiency. Details for the external antenna qualified are summarized in the table below.

**Table 11.1. Qualified External Antennas for MGM210P**

| Antenna Type | Maximum Gain | Impedance |
|---|---|---|
| Connectorized Coaxial Dipole | 2.14 dBi | 50 Ω |

Any antenna of the same general type and of equal or less directional gain as listed in the above table can be used in the regulatory areas that have a full modular radio approval (USA, Canada, Korea, Japan) as long as spot-check testing is performed to verify that no performance changes compromising compliance have been introduced. In countries applying the ETSI standards, like the EU countries, the radiated emissions are always tested with the end-product and the antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

If an antenna of a different type (such as a chip antenna, a PCB trace antenna or a patch) with a gain less than or equal to 2.14 dBi is needed, it can be added as a permissive change, requiring some radiated emission testing. Antenna types with more gain than 2.14 dBi may require a fully new certification. Since the exact permissive change procedure is chosen on a case by case basis, please consult your test house and/or certification body for understanding the correct approach. You might also want or need to get in touch with Silicon Labs for any authorization letter that your certification body might ask for.

## 11.2 CE and UKCA - EU and UK

The MGM210P modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU) and of the Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a MGM210P module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from https://www.silabs.com/.

### 11.3 FCC - USA

This device complies with Part 15 of the FCC Rules when operating with the embedded antenna or with the antenna type(s) listed in Table 11.1. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

#### FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance to the limit(s) exposed in the RF Exposure Analysis. This transmitter also meets the Portable requirements at distances equal or above 5 mm for the MGM210P22A and 36.17 mm for the MGM210P32A in the case of Zigbee, and respectively 5.3 mm and 44.03 mm in the case of Bluetooth Low Energy. These distances are reported for convenience also in Table 11.2. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

#### OEM Responsibilities to comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). Additionally, investigative measurements and spot checking are strongly recommended to verify that the full system compliance is maintained when the module is integrated, in accordance to the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide V01.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

  The end user manual shall include all required regulatory information/warnings as shown in this manual.

- **OEM/Host Manufacturer Responsibilities**

  OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment.

#### Separation

- To meet the SAR exemption for portable conditions, the minimum separation distance indicated in Table 11.2 must be maintained between the human body and the radiator (antenna) at all times. In particular, in the use case of Zigbee the minimum distance must be 5 mm for the MGM210P22A and 36.17 mm for the MGM210P32A, whereas in the use case of Bluetooth Low Energy the minimum distances must be 5.3 mm and 44.03 mm respectively.
- This transmitter module is tested in a standalone mobile RF exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation will be required, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that these conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF exposure in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The evaluation (SAR) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body as the grant holder's agent.

### End Product Labeling

MGM210P modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module FCC ID: QOQGM210P"**

Or

**"Contains FCC ID: QOQGM210P"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

### Class B Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

## 11.4 ISED - Canada

### ISED

This radio transmitter (IC: 5123A-GM210P) has been approved by *Innovation, Science and Economic Development Canada (ISED Canada, formerly Industry Canada*) to operate with the embedded antenna and with the antenna type(s) listed in Section 11.1 Qualified Antennas, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This device contains licence-exempt transmitter(s)/receiver(s) that comply with *Innovation, Science and Economic Development Canada*'s licence-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

### RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above 15 mm for the MGM210P22A and 35 mm for the MGM210P32A in the case of Zigbee, and respectively 20 mm and 40 mm in the case of Bluetooth Low Energy.

If the separation distance from the human body is less than the values stated above, which are also reported in Table 11.2 for convenience, the OEM integrator is responsible for evaluating the SAR.

### OEM Responsibilities to comply with IC Regulations

The module has been certified for integration into products only by OEM integrators under the following conditions:

- The antenna must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

**Important Note:** In the event that these conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF exposure in order for the ISED authorization to remain valid, and a permissive change will have to be applied with the help of the customer's own Telecommunication Certification Body typically acting as the certificate holder's agent.

### End Product Labeling

The MGM210P module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module IC: 5123A-GM210P** "

or

"**Contains IC: 5123A-GM210P"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

### CAN ICES-003 (B)

This Class B digital apparatus complies with Canadian ICES-003.

**ISED (Français)**

Le présent émetteur radio (IC: 5123A-GM210P) a été approuvé par Innovation, Sciences et Développement Économique Canada (ISED Canada, anciennement Industrie Canada) pour fonctionner avec l'antenne intégrée et le ou les types d'antenne énumérés à la section 11.1 Qualified Antennas, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste, ayant un gain supérieur au gain maximal indiqué, sont strictement interdits d'utilisation avec cet appareil. .

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNRd'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exemptsde licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil nedoit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptibled'en compromettre le fonctionnement.

**Déclaration d'exposition RF**

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation Portables, l'exposition aux fréquences radio ou l'évaluation du SAR n'est pas nécessaire lorsque les distances de séparation du corps humain sont égales ou supérieures à 15 mm pour le MGM210P22A et à 35 mm pour le MGM210P32A dans le cas de Zigbee, et respectivement à 20mm et à 40 mm dans le cas de Bluetooth Low Energy.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées ci-dessus, également indiquées dans le tableau 11.2 pour des raisons de commodité, l'intégrateur OEM est responsable de l'évaluation du SAR.

**Responsabilités du fabricant de se conformer à la réglementation IC**

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- L'antenne doit être installée de manière à maintenir une distance de séparation minimale, comme indiqué ci-dessus, entre le radiateur (antenne) et toutes les personnes.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

**Remarque Importante:** Au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, afin que l'autorisation ISED reste valable, et une modification permissive devra être appliquée à l'aide de propre organisme de certification de télécommunication du client en général agissant en tant que titulaire du certificat mandataire.

**Étiquetage des produits finis**

Les modules MGM210P est étiqueté avec son propre ID de certification.Si l'ID de certification n'est pas visible lorsque le module est installé dans un autre appareil, l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-GM210P** "

or

"**Contient IC: 5123A-GM210P"**

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

**CAN ICES-003 (B)**

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

### 11.5 MIC - Japan

The MGM210P22A low power variants are certified in Japan with number 020-190253.

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment places the certification mark and certification number on the outside of the host equipment. This combination of mark and number, and their relative placement, is depicted in Figure 9.1, and depending on the size of the module it might also appear on the top shield markings of the radio module. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

**Translation of the text:**

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" marking shown in the following figures must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Note that such section may be required to contain additional information if the end-device embedding the module is also subject to a telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan.


**Figure 11.1. GITEKI Mark and ID**

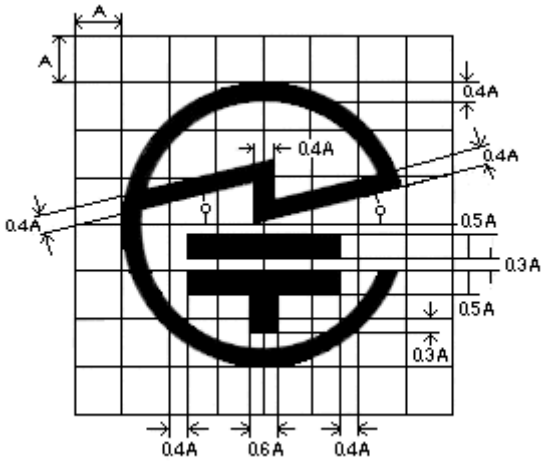


**Figure 11.2. Detail of GITEKI Mark**

### 11.6 KC - South Korea

The MGM210P22A low-power variants have a RF certification for import and use in South Korea. Their certification number is R-C-BGT-GM210P.

When integrating the RF-certified module, an end-product is exempted from doing the RF emission testing as long as the recommended design guidance is followed, and the approved antennas are used.

EMC testing, and any other relevant tests, might still be required for full compliance.

### 11.7 Proximity to Human Body

When using the module in an application where the radio is located close to the human body, the human RF exposure must be evaluated. FCC, ISED, and CE all have different standards for evaluating the RF exposure, and because of this, each standard requires a different minimum separation distance between the module and human body. Certification of MGM210P allows for the minimum separation distances detailed in the table below in Portable use cases (less than 20 cm from human body). The module is approved for the Mobile use case (more than 20 cm) without any need for RF exposure evaluation.

**Table 11.2. Minimum Separation Distances for SAR Evaluation Exemption**

| Certification | MGM210P22A | MGM210P32A |
|---|---|---|
| FCC | Bluetooth: 5.3 mm, Zigbee: 5 mm | Bluetooth: 44.03 mm, Zigbee: 36.17 mm |
| ISED | Bluetooth: 20 mm, Zigbee: 15 mm | Bluetooth: 40 mm, Zigbee: 35 mm |
| CE | The RF exposure must always be evaluated using the end-product when transmitting with power levels higher than 20 mW (13 dBm). | |

For FCC and ISED, using the module in end-products where the separation distance from the human body is smaller than that listed above is allowed but requires evaluation of the RF exposure in the final assembly and applying for a *Class 2 Permissive Change* or *Change of ID* to be applied to the existing FCC/ISED approvals of the module. For CE, RF exposure must be evaluated using the end-product in all cases when transmitting at more than the power level indicated in the table.

**Note:** Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

### 11.8 Bluetooth Qualification

The MGM210P modules come at launch with a pre-qualified Bluetooth Low Energy RF-PHY Tested Component having Declaration ID of D043475 and QDID of 129390, and having a listing date of 2019-04-02. Due to expiry, the Tested Component was renewed on 2024-02-21 with a new Declaration ID of D066522 and QDID of 231202.

Because the validity set by the SIG for Tested Components is currently of 3 years, during the product lifetime Silicon Labs will renew this Component as it expires, whenever applicable. Renewed Tested Components will come with new DIDs and QDIDs, and these will be then referred to in end-product listings. Such new DIDs and QDIDs can be discovered starting from the original ones.

This module's RF-PHY Tested Component should be combined with the latest Wireless Gecko Link Layer and Host pre-qualified Components by Silicon Labs, when in the process of qualifying an end-product embedding the MGM210P via the SIG's Launch Studio.

# 12. Revision History

### Revision 1.5

August, 2025

- Visual update to 4.17.1 Antenna Radiation and Efficiency

### Revision 1.4

May, 2024

- Changed mentions of "Secure Element" to "Secure Engine" and "Secure Vault".
- 2. Ordering Information: Changed Bluetooth version from 5.3 to 5.x and added note regarding Bluetooth 5.x support.
- 3.2 EFR32MG21 SoC: Removed reference to EFR32MG21B Data Sheet.
- 4.1 Absolute Maximum Ratings: Added "DC voltage on RESETn pin" specification and added note regarding RESETn pin's pullup to VDD.
- 4.2 General Operating Conditions: Added External Clock Input and DPLL Reference Clock maximum specifications.
- 4.2 General Operating Conditions: Removed Min and Max from HCLK Radio frequency.
- Changed symbol SAT to $RX_{SAT}$ in Table 4.8 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band on page 16 and Table 4.9 RF Receiver Characteristics for Bluetooth Low Energy at 1 Mbps on page 17.
- Added footnote about external capacitance to GAIN = 2 in Table 4.14 Low Frequency Crystal Oscillator on page 21
- 4.15 GPIO Pins:
  - Updated test condition for $V_{OL}$ and $V_{OH}$ from "IOVDD = 1.62 V" to "IOVDD = 1.71 V"
  - Added "RESETn low time to ensure pin reset" specification.
- Table 6.2 GPIO Alternate Function Table on page 30: Added VREFP pin.
- Updated 11. Certifications: Added MGM210P22A.
- Updated Bluetooth Qualification information.

### Revision 1.3

Decenber, 2022

- Updated supported Bluetooth version from 5.1 to 5.3
- Updated Bluetooth Qualification information.

### Revision 1.2

October, 2021

- Renamed Regulatory Certifications section in 1. Features for improved readability.
- Updated the Security column in Table 2.1 Ordering Information on page 3.
- Added low frequency crystal related information to 3.1 Block Diagram.
- Added information about Secure Vault devices to 3.2 EFR32MG21 SoC.
- Updated 3.5 Security and Table 3.2 Security Features and Levels on page 7 with Mid and High Secure Vault information.
- Added Table 4.14 Low Frequency Crystal Oscillator on page 21.
- Note about low frequency crystal added to 5.2 SoC Application.
- Corrected the length of the RF trace in 7.1 Layout and Placement.
- Renamed sub-section titles under for improved readability.
- Updated 11.2 CE and UKCA - EU and UK.

**Revision 1.1**

August, 2020

- Replaced Thread with OpenThread throughout document
- Updated security wording in Front Page and added Core/Memory and Security components to block diagram enabled with Secure Vault
- Updated list of security features and corrected number of 16-bit Timer/Counter (from 2 x to 3 x) in 1. Features
- Added MGM210PBxxxxxx part numbers to Table 2.1 Ordering Information on page 3 and updated footnotes
- Added 3.5 Security
- Added VCOM TX/RX pin labels to J1 connector in 5. Reference Diagrams and references to UG388/UG389 for example on how to enable VCOM
- Added footnote on DECOUPLE pin to Table 6.1 MGM210P Module Pin Definitions on page 29
- Added comment to Figure 7.3 Non-Optimal Layout Examples on page 36 noting that figure applies to module use cases with on-board chip antenna only
- Updated graphic type for Figure 8.1 Top and Side Views on page 39
- Removed top marking figures for MGM210P0 part numbers and added those for MGM210PB part numbers in 8.3 Package Marking
- Added comment on pin 1 orientation in 10.1 Tape and Reel
- Added 10.2 Moisture Sensitivity Level
- Added 11.8 Bluetooth Qualification

**Revision 1.0**

January, 2020

- Corrected LETIMER's lowest power mode in front page block diagram from EM2 to EM3
- Added RF Pin to front page block diagram
- Removed MGM210P0xxxxxx part numbers from Ordering Information table
- Replaced "Chip" with "Built-in" antenna throughout document
- Added sentence in Section 3.3 Antenna clarifying that antenna diversity is not supported
- Added text in Section 3.4 Power Supply about DECOUPLE pin
- Corrected lower limit for operating voltage range from 1.8 to 1.71 V in Section 4. Electrical Specifications
- Resolved remaining TBD entries in Section 4. Electrical Specifications
- Changed "3.3V" net label to "VDD" and connected pins U1.20 and U1.29 to GND in Section 5. Reference Diagrams
- Added supply connection recommendation for NCP use cases with different IOVDD and VDD levels in Section 5.1 Network Co-Processor (NCP) Application with UART Host
- Updated DECOUPLE pin description to "Do Not Connect", and added notes on RESET and RF2G4_IO2 pins to Table 6.1 MGM210P Module Pin Definitions on page 29
- Corrected edge-alignment placement recommendation to "Optional, not mandatory" in Figure 7.2 Recommended Layout for MGM210P Using External Antenna on page 36
- Added Sections 7.4 Reset, 7.5 Debug and 7.6 Packet Trace Interface (PTI)
- Renamed Section 8.1 Dimensions as 8.1 Package Outline
- Renamed Fig 8.1 Module Dimensions as Figure 8.1 Top and Side Views on page 39 and added Figure 8.2 Bottom View on page 39
- Added Japan and South Korea certifications

**Revision 0.5.1**

September, 2019

- Update wording for FCC and ISED certifications section
- Updated Design Guidelines

### Revision 0.5

September, 2019

- Initial Production Release.
- Updated with latest values, certifications, security, etc
- Updated with OPNs for Reel packaging
- Added System Overview
- Updated Electrical Specifications with latest values
- Added Reference Diagrams
- Updated wording and figures in Design Guidelines
- Updated figures in Package Specifications and added Marking section
- Added Tape and Reel dimensions
- Updated information
- General wording, spelling, and grammar fixes.

### Revision 0.1

April, 2019

- Initial Release.

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