

デュアル周波数水晶発振器 (XO) 100 kHz ~ 250 MHz

特長

- 100 kHz ~ 250 MHz の任意の周波数をサポート
- 選択可能な 2 つの出力周波数
- 低ジッタ動作
- 2 ~ 4 週間のリード・タイム
- 10 年エージングを含む総合安定度
- 水晶 ESR と DLD を含む包括的な生産試験範囲
- 電源ノイズをフィルタするオンチップ LDO レギュレータ
- 3.3、2.5、または 1.8 V 動作差動 (LVPECL、LVDS、HCSL) または CMOS の出力オプション
- オプションの内蔵 1:2 CMOS ファンアウト・バッファ
- OE および電源投入時のラント抑制機能
- 業界標準の 5x7、3.2x5、および 2.5x3.2 mm パッケージ
- 鉛フリー対応、RoHS 準拠
- -40 ~ 85 °C で動作

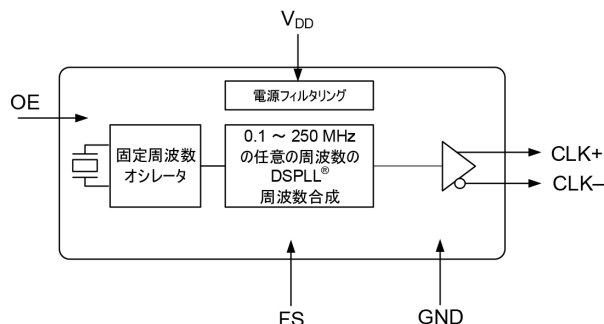
アプリケーション

- SONET/SDH/OTN
- ギガビット・イーサネット
- ファイバ・チャネル/SAS/SATA
- PCI Express
- 放送用ビデオ
- スイッチ/ルーター
- テレコム
- FPGA/ASIC クロック生成

説明

Si512/513 デュアル周波数 XO は、Silicon Laboratories の高度な PLL 技術を利用して、100 kHz ~ 250 MHz 範囲のすべての周波数を提供します。出力周波数ごとに異なる水晶が必要な従来の XO とは異なり、Si512/513 は 1 つの固定水晶と Silicon Labs 独自の任意の周波数合成を使用して、この周波数範囲のすべての周波数を生成します。この IC ベースのアプローチにより、水晶共振器の優れた信頼性、機械的な耐久性の向上、高い安定度が実現しています。さらに、本ソリューションは優れた電源ノイズ除去性能を備えているため、ノイズの多い環境で低ジッタ・クロック生成を簡素化できます。Si512/513 は、周波数、供給電圧、出力形式、出力イネーブル極性、安定度など、幅広いユーザ設定に合わせて工場出荷時に構成できます。詳細な構成は出荷時に工場プログラムされるため、カスタム周波数発振器に伴う長いリード・タイムや、単発的なエンジニアリング費用を排除できます。

機能ブロック・ダイアグラム

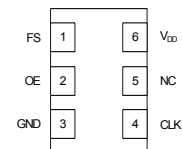


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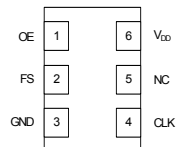
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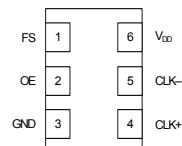
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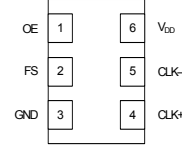
Si512 CMOS デュアル XO



Si513 CMOS デュアル XO



Si512 LVDS/LVPECL/HCSL/CMOS
デュアル XO



Si513 LVDS/LVPECL/HCSL/CMOS
デュアル XO

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1. Electrical Specifications

Table 1. Operating Specifications

$V_{DD} = 1.8\text{ V} \pm 5\%$, 2.5 or 3.3 V $\pm 10\%$, $T_A = -40$ to $+85\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	CMOS, 100 MHz, single-ended	—	21	26	mA
		LVDS (output enabled)	—	19	23	mA
		LVPECL (output enabled)	—	39	43	mA
		HCSL (output enabled)	—	41	44	mA
		Tristate (output disabled)	—	—	18	mA
FS, OE "1" Setting	V_{IH}	See Note	$0.80 \times V_{DD}$	—	—	V
FS, OE "0" Setting	V_{IL}	See Note	—	—	$0.20 \times V_{DD}$	V
FS, OE Internal Pull-Up/Pull-Down Resistor*	R_I		—	45	—	k Ω
Operating Temperature	T_A		-40	—	85	$^\circ\text{C}$

Note: Active high and active low polarity OE options available. Active high uses internal pull-up. Active low uses internal pull-down. See ordering information on page 12.

Table 2. Output Clock Frequency Characteristics

$V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ or }3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency	F_O	CMOS, Dual CMOS	0.1	—	212.5	MHz
	F_O	LVDS/LVPECL/HCSL	0.1	—	250	MHz
Total Stability*		Frequency Stability Grade C	-30		+30	ppm
		Frequency Stability Grade B	-50		+50	ppm
		Frequency Stability Grade A	-100		+100	ppm
Temperature Stability		Frequency Stability Grade C	-20		+20	ppm
		Frequency Stability Grade B	-25		+25	ppm
		Frequency Stability Grade A	-50		+50	ppm
Startup Time	T_{SU}	Minimum V_{DD} to output frequency (F_O) within specification	—	—	10	ms
Disable Time	T_D	$F_O \geq 10\text{ MHz}$	—	—	5	μs
		$F_O < 10\text{ MHz}$	—	—	40	μs
Enable Time	T_E	$F_O \geq 10\text{ MHz}$	—	—	20	μs
		$F_O < 10\text{ MHz}$	—	—	60	μs
Settling Time after FS Change	t_{FRQ}		—	—	10	ms

***Note:** Total stability includes initial accuracy, operating temperature, supply voltage change, load change, shock and vibration (not under operation), and 10 years aging at $40\text{ }^\circ\text{C}$.

Table 3. Output Clock Levels and Symmetry $V_{DD} = 1.8 \text{ V} \pm 5\%$, 2.5 or 3.3 V $\pm 10\%$, $T_A = -40$ to $+85$ °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CMOS Output Logic High	V_{OH}		$0.85 \times V_{DD}$	—	—	V
CMOS Output Logic Low	V_{OL}		—	—	$0.15 \times V_{DD}$	V
CMOS Output Logic High Drive	I_{OH}	3.3 V	-8	—	—	mA
		2.5 V	-6	—	—	mA
		1.8 V	-4	—	—	mA
CMOS Output Logic Low Drive	I_{OL}	3.3 V	8	—	—	mA
		2.5 V	6	—	—	mA
		1.8 V	4	—	—	mA
CMOS Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F	0.1 to 125 MHz, $C_L = 15$ pF	—	0.8	1.2	ns
		0.1 to 212.5 MHz, $C_L =$ no load	—	0.6	0.9	ns
LVPECL/HCSL Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F		—	—	565	ps
LVDS Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F		—	—	800	ps
LVPECL Output Common Mode	V_{OC}	50Ω to $V_{DD} - 2$ V, single-ended	—	$V_{DD} - 1.4$ V	—	V
LVPECL Output Swing	V_O	50Ω to $V_{DD} - 2$ V, single-ended	0.55	0.8	0.90	V_{PPSE}
LVDS Output Common Mode	V_{OC}	100 Ω line-line, $V_{DD} = 3.3/2.5$ V	1.13	1.23	1.33	V
		100 Ω line-line, $V_{DD} = 1.8$ V	0.83	0.92	1.00	V
LVDS Output Swing	V_O	Single-ended, 100 Ω differential termination	0.25	0.35	0.45	V_{PPSE}
HCSL Output Common Mode	V_{OC}	50Ω to ground	0.35	0.38	0.42	V
HCSL Output Swing	V_O	Single-ended	0.58	0.73	0.85	V_{PPSE}
Duty Cycle	DC	All Output Formats	48	50	52	%

Table 4. Output Clock Jitter and Phase Noise (LVPECL)

$V_{DD} = 2.5$ or 3.3 V $\pm 10\%$, $T_A = -40$ to $+85$ °C; Output Format = LVPECL

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter (RMS)	JPRMS	10k samples ¹	—	—	1.3	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples ¹	—	—	11	ps
Phase Jitter (RMS)	ϕJ	1.875 MHz to 20 MHz integration bandwidth ² (brickwall)	—	0.31	0.5	ps
		12 kHz to 20 MHz integration bandwidth (brickwall) ²	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	ϕN	100 Hz	—	-86	—	dBc/Hz
		1 kHz	—	-109	—	dBc/Hz
		10 kHz	—	-116	—	dBc/Hz
		100 kHz	—	-123	—	dBc/Hz
		1 MHz	—	-136	—	dBc/Hz
Additive RMS Jitter Due to External Power Supply Noise ³	JPSR	10 kHz sinusoidal noise	—	3.0	—	ps
		100 kHz sinusoidal noise	—	3.5	—	ps
		500 kHz sinusoidal noise	—	3.5	—	ps
		1 MHz sinusoidal noise	—	3.5	—	ps
Spurious	SPR	LVPECL output, 156.25 MHz, offset > 10 kHz	—	-75	—	dBc

Notes:

1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.
3. 156.25 MHz. Increase in jitter on output clock due to sinewave noise added to VDD (2.5/3.3 V = 100 mVPP).

Table 5. Output Clock Jitter and Phase Noise (LVDS)

$V_{DD} = 1.8 \text{ V} \pm 5\%$, $2.5 \text{ or } 3.3 \text{ V} \pm 10\%$, $T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$; Output Format = LVDS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples ¹	—	—	2.1	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples ¹	—	—	18	ps
Phase Jitter (RMS)	ϕJ	1.875 MHz to 20 MHz integration bandwidth ² (brickwall)	—	0.25	0.55	ps
		12 kHz to 20 MHz integration bandwidth ² (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	ϕN	100 Hz	—	-86	—	dBc/Hz
		1 kHz	—	-109	—	dBc/Hz
		10 kHz	—	-116	—	dBc/Hz
		100 kHz	—	-123	—	dBc/Hz
		1 MHz	—	-136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset > 10 kHz	—	-75	—	dBc

Notes:

1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.

Table 6. Output Clock Jitter and Phase Noise (HCSL)

$V_{DD} = 1.8\text{ V} \pm 5\%$, 2.5 or 3.3 V $\pm 10\%$, $T_A = -40$ to $+85\text{ }^\circ\text{C}$; Output Format = HCSL

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples*	—	—	1.2	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples*	—	—	11	ps
Phase Jitter (RMS)	ϕ_J	1.875 MHz to 20 MHz integration bandwidth* (brickwall)	—	0.25	0.30	ps
		12 kHz to 20 MHz integration bandwidth* (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	ϕ_N	100 Hz	—	-90	—	dBc/Hz
		1 kHz	—	-112	—	dBc/Hz
		10 kHz	—	-120	—	dBc/Hz
		100 kHz	—	-127	—	dBc/Hz
		1 MHz	—	-140	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset > 10 kHz	—	-75	—	dBc

*Note: Applies to an output frequency of 100 MHz.

Table 7. Output Clock Jitter and Phase Noise (CMOS, Dual CMOS)

$V_{DD} = 1.8\text{ V} \pm 5\%$, 2.5 or 3.3 V $\pm 10\%$, $T_A = -40$ to $+85\text{ }^\circ\text{C}$; Output Format = CMOS, Dual CMOS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Jitter (RMS)	ϕ_J	1.875 MHz to 20 MHz integration bandwidth ² (brickwall)	—	0.25	0.35	ps
		12 kHz to 20 MHz integration bandwidth ² (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	ϕ_N	100 Hz	—	-86	—	dBc/Hz
		1 kHz	—	-108	—	dBc/Hz
		10 kHz	—	-115	—	dBc/Hz
		100 kHz	—	-123	—	dBc/Hz
		1 MHz	—	-136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset > 10 kHz	—	-75	—	dBc

Notes:

1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.

Table 8. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel

Table 9. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
CLCC, Thermal Resistance Junction to Ambient	θ_{JA}	Still air	110	°C/W
2.5x3.2mm, Thermal Resistance Junction to Ambient	θ_{JA}	Still air	164	°C/W

Table 10. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	°C
Storage Temperature	T_S	-55 to +125	°C
Supply Voltage	V_{DD}	-0.5 to +3.8	V
Input Voltage (any input pin)	V_I	-0.5 to $V_{DD} + 0.3$	V
ESD Sensitivity (HBM, per JESD22-A114)	HBM	2	kV
Soldering Temperature (Pb-free profile) ²	T_{PEAK}	260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile) ²	T_P	20–40	sec

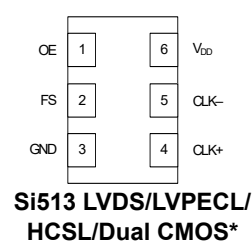
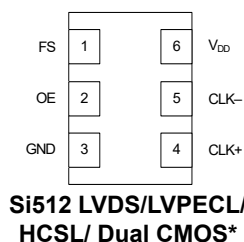
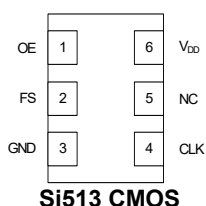
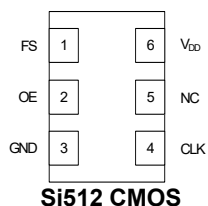
Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020E.

2. Solder Reflow and Rework Requirements for 2.5x3.2 mm Packages

Reflow of Silicon Labs' components should be done in a manner consistent with the IPC/JEDEC J-STD-20E standard. The temperature of the package is not to exceed the classification Temperature provided in the standard. The part should not be within -5°C of the classification or peak reflow temperature (T_{PEAK}) for longer than 30 seconds. Key to maintaining the integrity of the component is providing uniform heating and cooling of the part during reflow and rework. Uniform heating is achieved through having a preheat soak and controlling the temperature ramps in the process. J-STD-20E provides minimum and maximum temperatures and times for the preheat/Soak step that need to be followed, even for rework. The entire assembly area should be heated during rework. Hot air should be flowed from both the bottom of the board and the top of the component. Heating from the top only will cause un-even heating of component and can lead to part integrity issues. Temperature Ramp-up rate are not to exceed 3°C/second. Temperature ramp-down rates from peak to final temperature are not to exceed 6°C/second. Time from 25°C to peak temperature is not to exceed 8 min for Pb-free solders.

3. Pin Descriptions



***Note:** Supports integrated 1:2 CMOS buffer. See section 2.1 “3.1. Dual CMOS Buffer” and section 3 “4. Ordering Information”.

Table 11. Si512 Pin Descriptions (CMOS, OE Pin 2)

Pin	Name	CMOS Function
1	FS	Frequency Selected. 0 = First frequency selected. 1 = Second frequency selected.
2	OE	Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information.
3	GND	Electrical and Case Ground.
4	CLK	Clock Output.
5	NC	No connect. Make no external connection to this pin.
6	V _{DD}	Power Supply Voltage.

Table 12. Si513 Pin Descriptions (CMOS, OE Pin 1)

Pin	Name	CMOS Function
1	OE	Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information.
2	FS	Frequency Selected. 0 = First frequency selected. 1 = Second frequency selected.
3	GND	Electrical and Case Ground.
4	CLK	Clock Output.
5	NC	No connect. Make no external connection to this pin.
6	V _{DD}	Power Supply Voltage.

Table 13. Si512 Pin Descriptions (OE Pin 2)

Pin	Name	LVPECL/LVDS/HCSL/Dual CMOS Function
1	FS	Frequency Selected. 0 = First frequency selected. 1 = Second frequency selected.
2	OE	Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information.
3	GND	Electrical and Case Ground.
4	CLK+	Clock Output.
5	CLK-	Complementary Clock Output.
6	V _{DD}	Power Supply Voltage.

Table 14. Si513 Pin Descriptions (OE Pin 1)

Pin	Name	LVPECL/LVDS/HCSL/Dual CMOS Function
1	OE	Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information.
2	FS	Frequency Selected. 0 = First frequency selected. 1 = Second frequency selected.
3	GND	Electrical and Case Ground.
4	CLK+	Clock Output.
5	CLK-	Complementary Clock Output.
6	V _{DD}	Power Supply Voltage.

3.1. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase output signals. This feature enables replacement of multiple XOs with a single Si512/13 device.

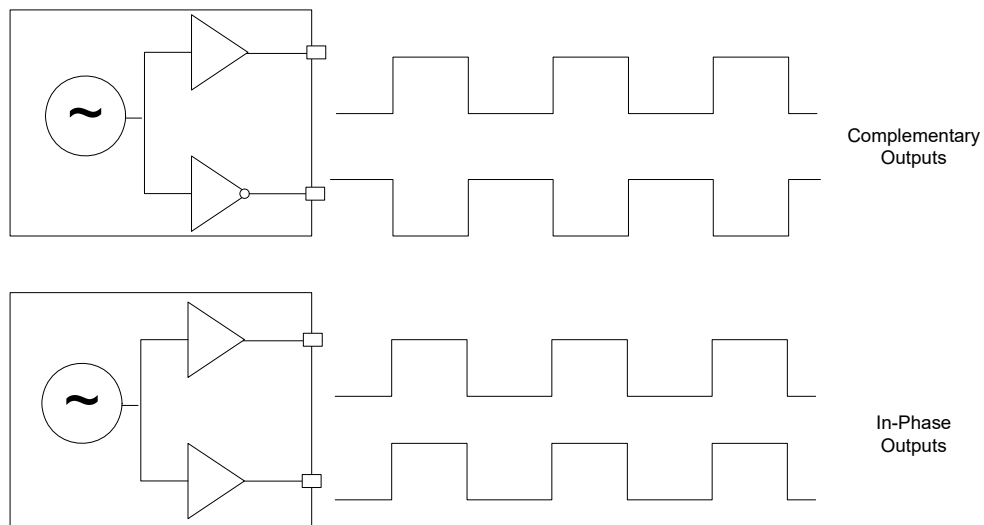


Figure 1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

4. Ordering Information

The Si512/513 supports a wide variety of options including frequency, stability, output format, and V_{DD} . Specific device configurations are programmed into the Si512/513 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to www.silabs.com/oscillators and click "Customize" in the product table. The Si512/513 XO series is supplied in industry-standard, RoHS compliant, lead-free, 2.5 x 3.2 mm, 3.2 x 5.0 mm, and 5 x 7 mm packages. Tape and reel packaging is an ordering option.

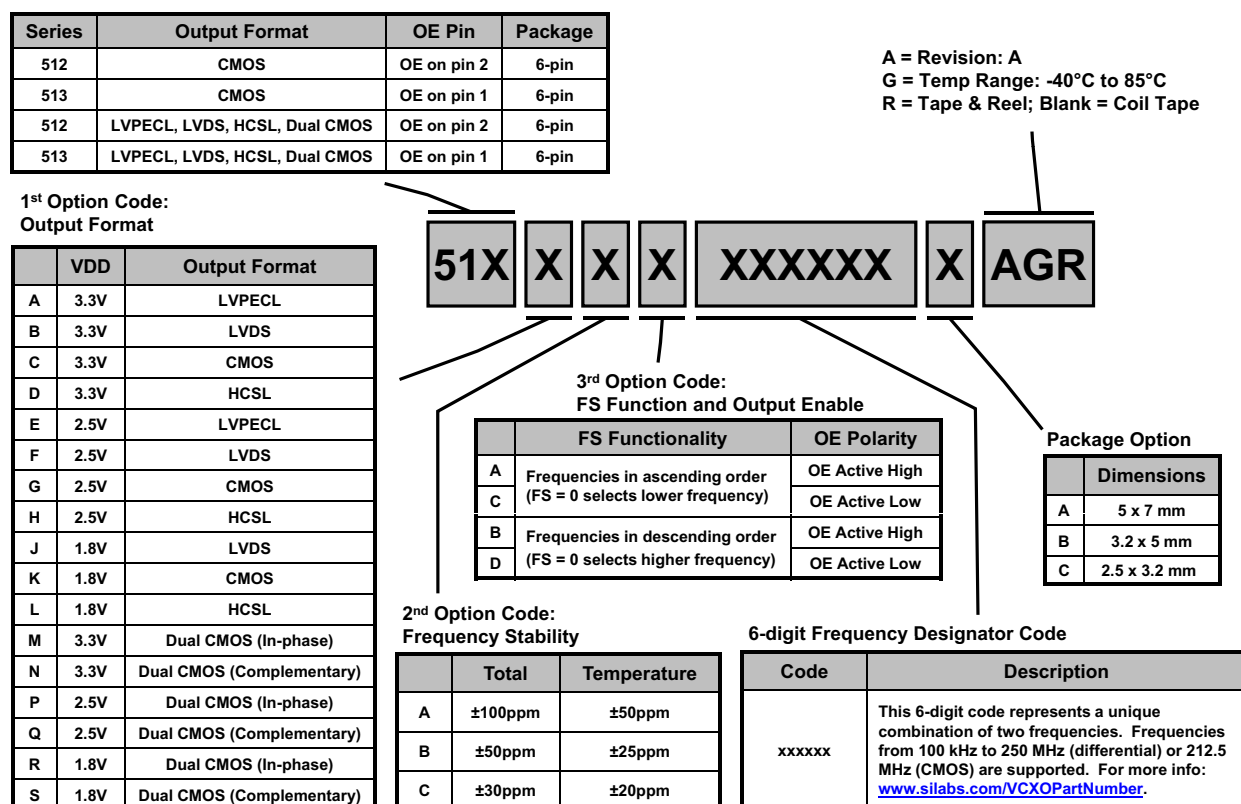


Figure 2. Part Number Convention

Example part number: 512PCA000104BAGR:

The series prefix, 512, indicates the device is a Dual CMOS XO with the OE function on pin 2. The output format code P specifies the outputs are dual in-phase CMOS with a 2.5 V supply. The frequency stability code C indicates a total stability of ± 30 ppm. The frequency select and output enable code A specifies that the two frequencies are listed in ascending order, with the output frequency f_0 (the lower frequency) selected when FS=0, and f_1 (the higher frequency) selected when FS = 1. The device's output enable polarity is active High.

The six-digit code is 000104. As specified by the part number lookup utility at www.silabs.com/VCXOPartNumber, f_0 is 155.52 MHz (the lower frequency) and f_1 is 156.25 MHz (the higher frequency). The package code B refers to the 3.2 x 5 mm footprint with six pins. The last A refers to the product revision, G indicates the temperature range (-40 to +85°C), and R means the device ships in tape and reel format.

Note: CMOS and Dual CMOS maximum frequency is 212.5 MHz.

5. Package Outline Diagram, 5 x 7 mm, 6-pin

Figure 3 illustrates the package details for the 5 x 7 mm Si512/513. Table 15 lists the values for the dimensions shown in the illustration.

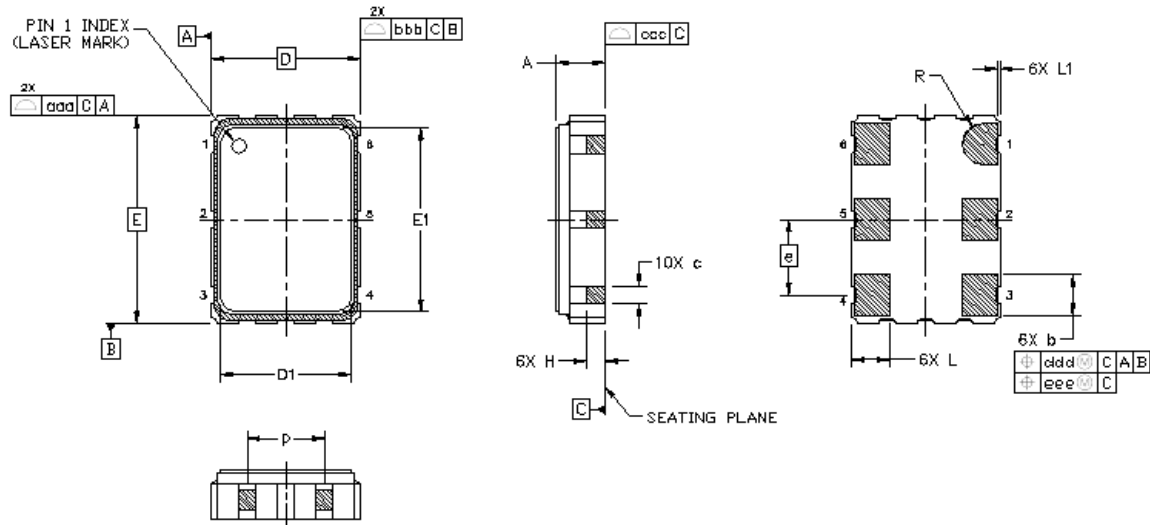


Figure 3. Si512/513 Outline Diagram

Table 15. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D	5.00 BSC.		
D1	4.30	4.40	4.50
e	2.54 BSC.		
E	7.00 BSC.		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R	0.70 REF.		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.05		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

6. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 4 illustrates the 5 x 7 mm PCB land pattern for the Si512/513. Table 16 lists the values for the dimensions shown in the illustration.

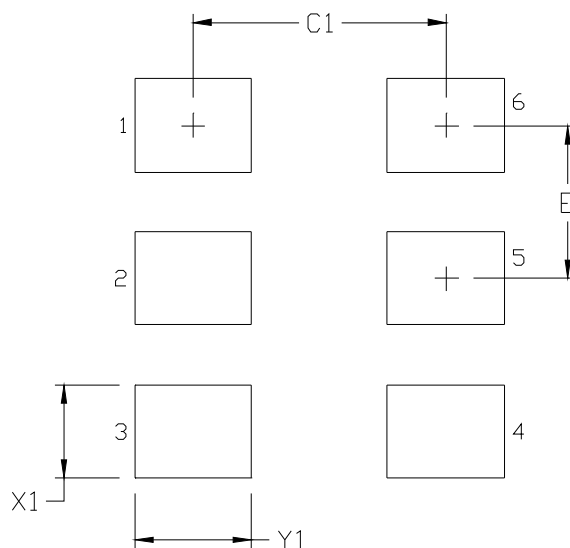


Figure 4. Si512/513 PCB Land Pattern

Table 16. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Package Outline Diagram: 3.2 x 5.0 mm, 6-pin

Figure 5 illustrates the package details for the 3.2 x 5.0 mm Si512/513. Table 17 lists the values for the dimensions shown in the illustration.

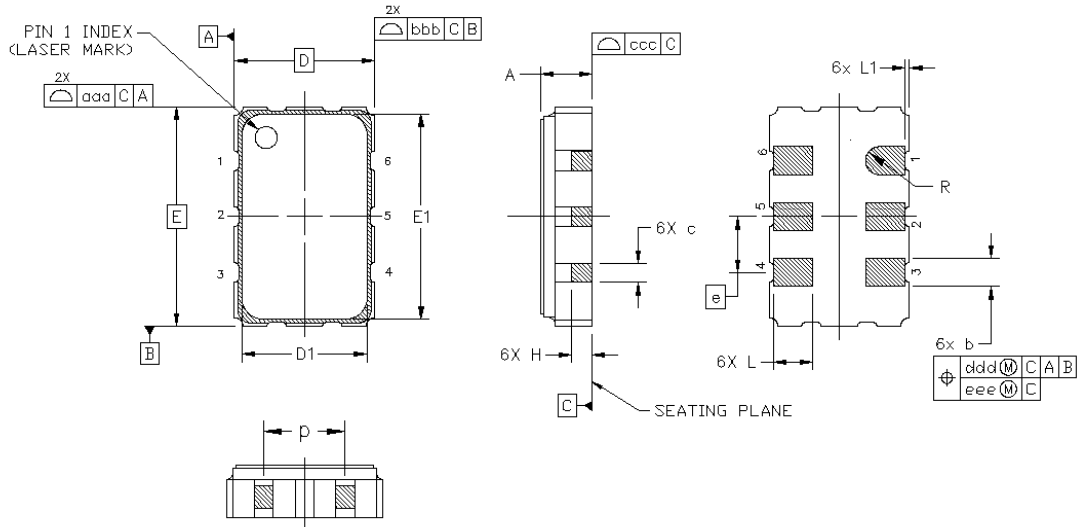


Figure 5. Si512/513 Outline Diagram

Table 17. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.06	1.17	1.33
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D	3.20 BSC		
D1	2.55	2.60	2.65
e	1.27 BSC		
E	5.00 BSC		
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.80	0.90	1.00
L1	0.05	0.10	0.15
p	1.17	1.27	1.37
R	0.32 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.05		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

8. PCB Land Pattern: 3.2 x 5.0 mm

Figure 6 illustrates the 3.2 x 5.0 mm PCB land pattern for the Si512/513. Table 18 lists the values for the dimensions shown in the illustration.

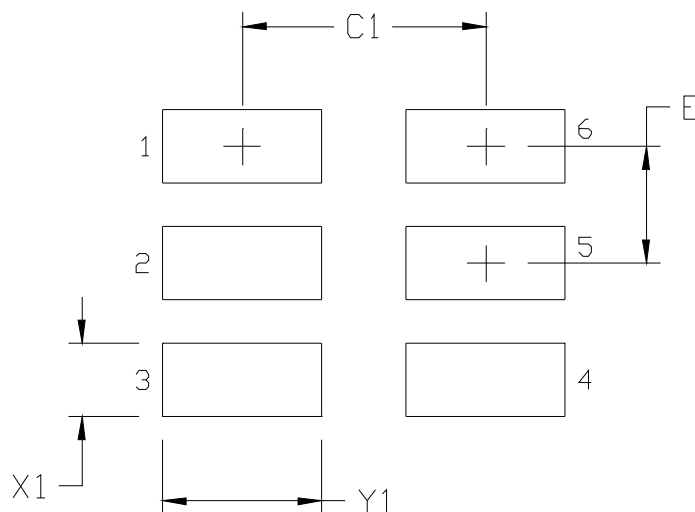


Figure 6. Si512/513 Recommended PCB Land Pattern

Table 18. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

Notes:

General

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Package Outline Diagram: 2.5 x 3.2 mm, 6-pin

Figure 7 illustrates the package details for the 2.5 x 3.2 mm Si512/513. Table 19 lists the values for the dimensions shown in the illustration.

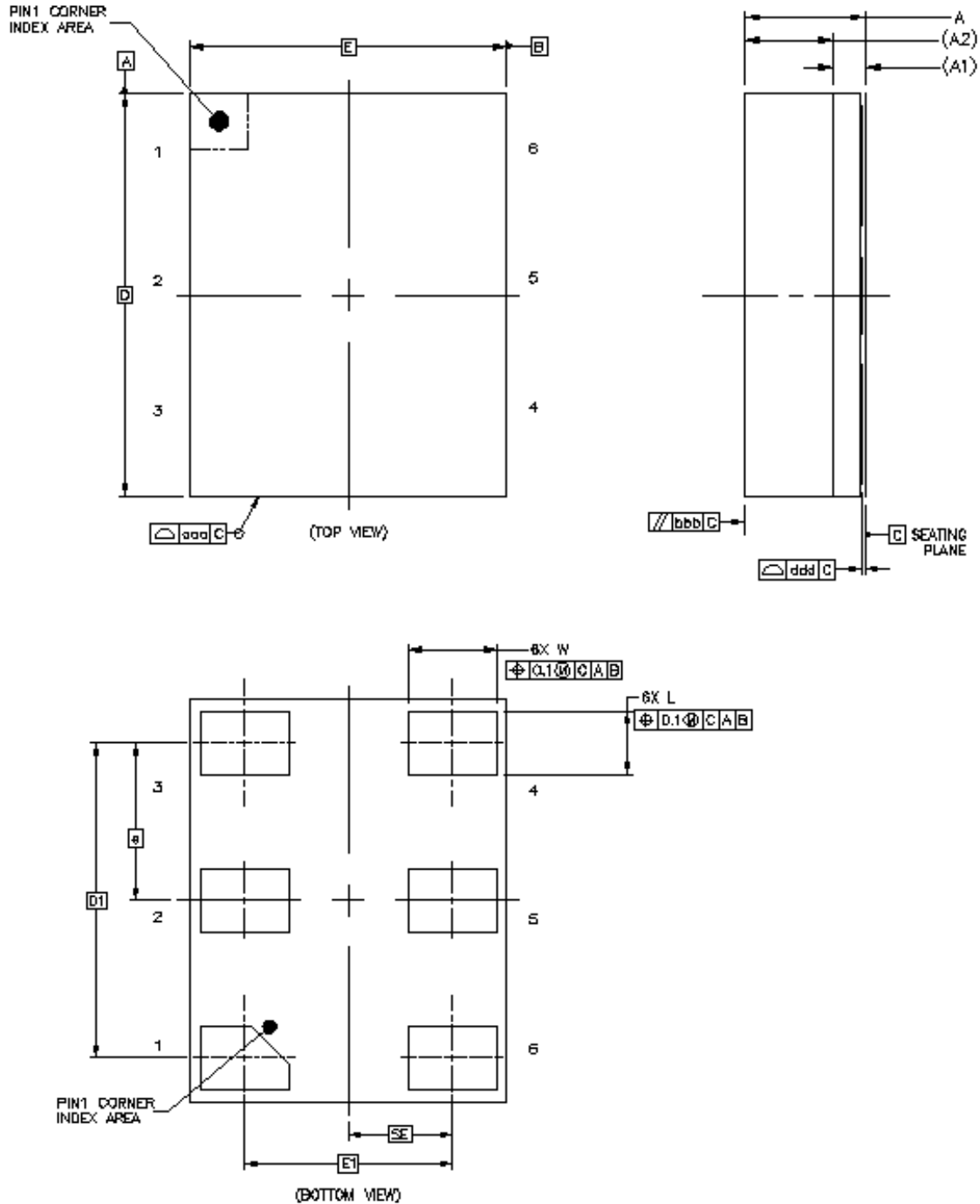


Figure 7. Si512/513 Outline Diagram

Table 19. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	—	—	1.1
A1	0.26 REF		
A2	0.7 REF		
W	0.65	0.7	0.75
D	3.20 BSC		
e	1.25 BSC		
E	2.50 BSC		
M	0.30 BSC		
L	0.45	0.5	0.55
D1	2.5 BSC		
E1	1.65 BSC		
SE	0.825 BSC		
aaa	0.1		
bbb	0.2		
ddd	0.08		
Notes:			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

10. PCB Land Pattern: 2.5 x 3.2 mm, 6-pin

Figure 8 illustrates the 2.5 x 3.2 mm PCB land pattern for the Si512/513. Table 20 lists the values for the dimensions shown in the illustration.

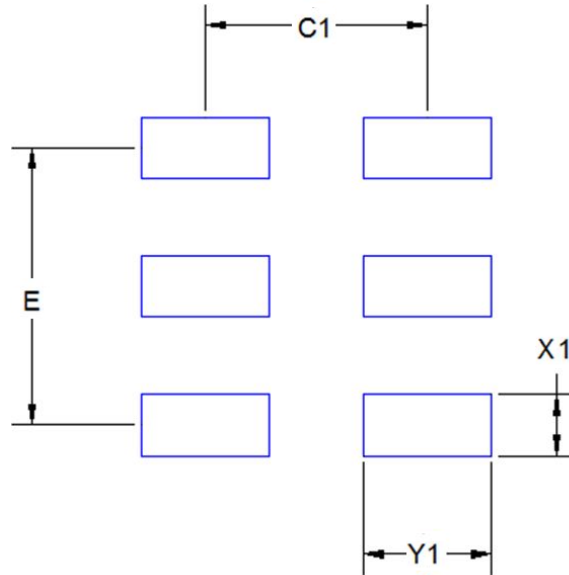


Figure 8. Si512/513 Recommended PCB Land Pattern

Table 20. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	1.9
E	2.50
X1	0.70
Y1	1.05

Notes:

General

- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
- This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

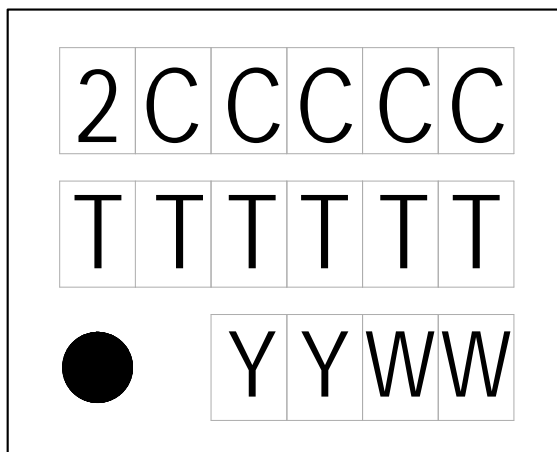
Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Top Marking

Use the part number configuration utility located at: www.silabs.com/VCXOpartnumber to cross-reference the mark code to a specific device configuration.

11.1. Si512/513 Top Marking



11.2. Top Marking Explanation

Mark Method:	Laser	
Line 1 Marking:	2 = Si512 3 = Si513 CCCCC = Mark Code	2CCCCC
Line 2 Marking:	TTTTTT = Assembly Manufacturing Code	TTTTTT
Line 3 Marking:	Pin 1 indicator.	Circle with 0.5 mm diameter; left-justified
	YY = Year. WW = Work week. Characters correspond to the year and work week of package assembly.	YYWW

REVISION HISTORY

Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in Ordering Guide.

Revision 1.1

December, 2017

- Add 2.5 x 3.2 mm package.

Revision 1.0

- Updated Table 1 on page 3.
 - Updates to supply current typical and maximum values for CMOS, LVDS, LVPECL and HCSL.
 - CMOS frequency test condition corrected to 100 MHz.
 - Updates to OE VIH minimum and VIL maximum values.
- Updated Table 2 on page 4.
 - Dual CMOS nominal frequency maximum added.
 - Total stability footnotes clarified for 10 year aging at 40 °C.
 - Disable time maximum values updated.
 - Enable time parameter added.
- Updated Table 3 on page 5.
 - CMOS output rise / fall time typical and maximum values updated.
 - LVPECL/HCSL output rise / fall time maximum value updated.
 - LVPECL output swing maximum value updated.
 - LVDS output common mode typical and maximum values updated.
 - HCSL output swing maximum value updated.
 - Duty cycle minimum and maximum values tightened to 48/52%.
- Updated Table 4 on page 6.
 - Phase jitter test condition and maximum value updated.
 - Phase noise typical values updated.
 - Additive RMS jitter due to external power supply noise typical values updated.
 - Footnote 3 updated limiting the VDD to 2.5/3.3V
- Added Tables 5, 6, 7 for LVDS, HCSL, CMOS, and Dual CMOS operations.
- Moved Absolute Maximum Ratings table.
- Added note to Figure 2 clarifying CMOS and Dual CMOS maximum frequency.
- Updated Figure 5 outline diagram to correct pinout.
- Updated Table 17 on page 16.
- Updated “11. Top Marking” section and moved to page 21.



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