



# Si52254/Si52258 数据表

## 4/8 输出 PCIe Gen1/2/3/4/5 时钟发生器

Si52258/54 是业界性能高、功耗低的汽车级 PCI Express 时钟发生器，适用于 PCIe Gen 1/2/3/4/5 公共时钟和/或 SRIS 应用。Si52258 和 Si52254 分别提供 8 路和 4 路 100 MHz PCIe 差分时钟输出。所有时钟输出均符合 PCIe Gen 1/2/3/4/5 公共时钟和单独参考时钟体系结构规格。

硬件控制引脚可用于启用和禁用输出，以及扩频使能/禁用（以降低 EMI）。

要详细了解 PCI Express、Silicon Labs 的完整 PCIe 产品组合、应用说明和设计工具，包括符合 PCI Express 标准的 Silicon Labs PCIe 时钟抖动工具，请访问 Silicon Labs PCI Express 学习中心。

### 应用：

- 信息娱乐
- ADAS ECU
- 雷达传感器
- LiDar 传感器

### 主要特点

- 8/4 输出，带内部终端
- 符合 PCIe Gen 1/2/3/4/5 标准
- 汽车级 2: -40 至 +105 °C
- 内部 100 Ω 或 85 Ω 线匹配
- 出色的抖动性能
  - 0.05 ps RMS (Gen3/4)
  - 0.025 ps RMS (Gen5)
- 三角扩频，用于降低 EMI，向下扩频 0.25% 或 0.5%
- 独立硬件控制引脚，用于输出使能、使能扩频
- 使能和频率选择
- 25 MHz 晶体输入或时钟输入
- 1.8 - 3.3 V 电源
- 无铅、符合 RoHS-6

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## 1. 功能列表

- 8/4 输出，带内部终端
- 符合 PCIe Gen1/2/3/4/5 标准
- 汽车级 2: -40 至 +105 °C
- 内部 100  $\Omega$  或 85  $\Omega$  线匹配
- 出色的抖动性能
  - 0.05 ps RMS (Gen3/4)
  - 0.025 ps RMS (Gen5)
- 三角扩频，用于降低 EMI，向下扩频 0.25% 或 0.5%
- 独立硬件控制引脚，用于输出使能、使能扩频
- 使能和频率选择
- 25 MHz 晶体输入或时钟输入
- 1.8 - 3.3 V 电源
- 无铅、符合 RoHS-6

## 2. Ordering Guide

Number of Outputs	Part Number	Package Type	Temperature
8	Si52258A-D01AM	40-QFN	Automotive, –40 to 105 °C
	Si52258A-D01AMR	40-QFN – Tape and Reel	Automotive, –40 to 105 °C
4	Si52254A-D01AM	32-QFN	Automotive, –40 to 105 °C
	Si52254A-D01AMR	32-QFN – Tape and Reel	Automotive, –40 to 105 °C

### 3. Functional Description

#### 3.1 Functional Block Diagram

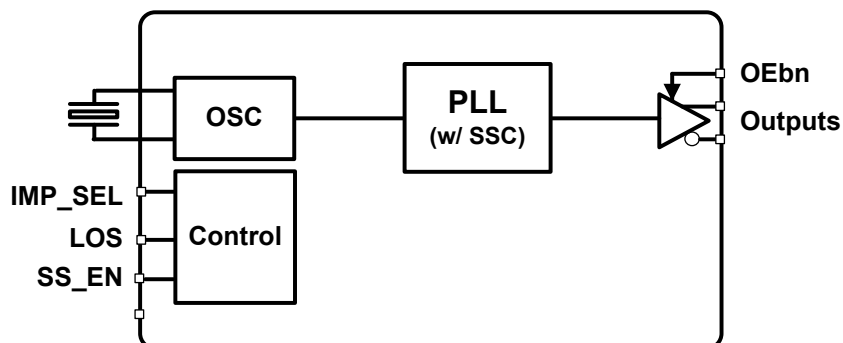


Figure 3.1. Si5225x Block Diagram

#### 3.2 Crystal Recommendations

The Si52258/4 operates from a parallel resonance 25 MHz crystal, or clock input. Crystal operation requires external loading capacitors to match crystal capacitive loading requirements. Si52258/4 XA/XB inputs present 2.5 pF of stray capacitance.

#### 3.3 HCSL Differential Output Terminations

##### Termination for HCSL Outputs

The Si52254/8 HCSL drivers feature integrated termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100  $\Omega$  and 85  $\Omega$  transmission line options, and can be selected using the IMP\_SEL hardware input pin.

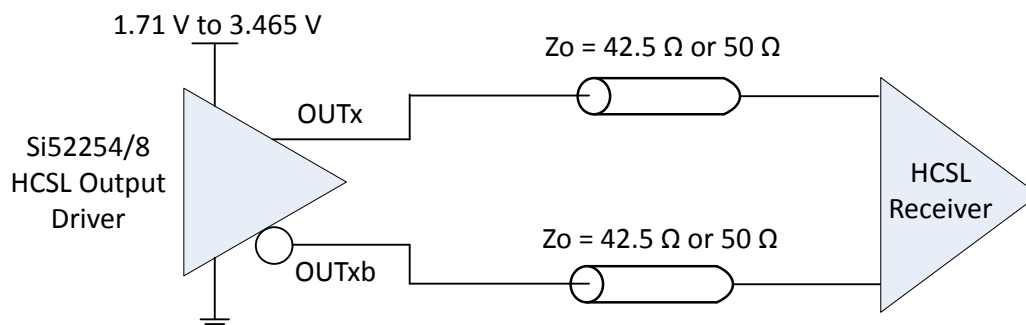


Figure 3.2. HCSL Internal Termination Mode

#### 3.4 Output Enable/Disable

An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high, all designated outputs will be disabled. When held low, the designated outputs will be enabled.

#### 3.5 Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si52254/8 supports spread spectrum modulation. Spread spectrum can be enabled by the hardware input pin.

### 3.6 Loss of Signal (LOS)

The LOS indicator is used to check for the presence of an input reference source (crystal or clock). LOS will assert when the reference source frequency drops below 10 MHz.

The LOS pin must be checked prior to selecting the clock input or should be polled to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic low (LOS = 0) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic high (LOS = 1) state.

#### 4. Power Supply Filtering Recommendations

The Si52258/4 features internal LDOs on each power supply pin, providing excellent power supply noise rejection. As a guideline, each power supply pin should use a parallel combination of a 1  $\mu\text{f}$  and a 0.1  $\mu\text{F}$  bypass capacitor placed as close to the supply pin as possible.

## 5. Electrical Specifications

**Table 5.1. Recommended Operating Conditions**
 $(V_{DD} = V_{DDA} = V_{DD\_DIG} = V_{DD\_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	$T_A$		-40	25	105	$^\circ\text{C}$
Junction Temperature	$T_{JMAX}$		—	—	125	$^\circ\text{C}$
Core Supply Voltage	$V_{DDA}, V_{DD\_DIG}, V_{DD\_xtal}$		1.71	—	3.46	V
Output Driver Supply Voltage	$V_{DDO}$		1.71	—	3.46	V

**Note:**

- All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25  $^\circ\text{C}$  unless otherwise noted.
- All core voltages ( $V_{DD\_DIG}$ ,  $V_{DDA}$ ,  $V_{DD\_XTAL}$ ) must be connected to the same voltage.

**Table 5.2. DC Characteristics**
 $(V_{DD} = V_{DDA} = V_{DD\_DIG} = V_{DD\_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Core Supply Current	$I_{DD}$		—	26	40	mA
Output Buffer Supply Current	$I_{DDOx}$	HCSL Output <sup>1</sup> @ 100 MHz	—	20	22	mA
Total Power Dissipation <sup>2</sup>	$P_d$	40-pin		550	750	mW
		32-pin	—	300	445	mW

**Notes:**

- Differential outputs terminated into a 100  $\Omega$  load at 3.3 V.
- Total power dissipation calculated with all 100 MHz HCSL running at 3.3 V.

**Table 5.3. External Crystal Input Specification**
 $(V_{DD} = V_{DDA} = V_{DD\_DIG} = V_{DD\_XTAL} = 1.8\text{ V to }3.3\text{ V }+5\%/-5\%, V_{DDO} = 1.8\text{ V } \pm 5\%, 2.5\text{ V } \pm 5\%, \text{ or } 3.3\text{ V } \pm 5\%, T_A = -40\text{ to }105\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	$F_{xtal}$			25		MHz
Crystal Drive Level	$d_L$		—	—	250	$\mu\text{W}$
Input Capacitance	$C_{IN}$		—	2.5	—	pF
Input Voltage	$V_{XIN}$		-0.3	—	1.3	V



**Table 5.4. Differential Clock Output Specifications**(V<sub>DD</sub> = V<sub>DDA</sub> = V<sub>DD\_DIG</sub> = V<sub>DD\_XTAL</sub> = 1.8 V to 3.3 V +5%/-5%, V<sub>DDO</sub> = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T<sub>A</sub> = -40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f <sub>OUT</sub>			100			MHz
Duty Cycle	DC			48	—	52	%
Output-Output Skew	T <sub>SK</sub>			—	—	80	ps
Output Voltage Swing	V <sub>SEPP</sub>	HCSL		0.7	0.8	0.9	V <sub>PP</sub>
Common Mode Voltage	V <sub>CM</sub>	HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 8, 10, 14		1	—	4.5	V/ns
HCSL Delta Tr	D <sub>tr</sub>	Notes 10, 13, 14		—	—	155	ps
HCSL Delta Tf	D <sub>tf</sub>	Notes 10, 13, 14		—	—	155	ps
HCSL Vcross Abs	V <sub>xa</sub>	Notes 7, 9, 10, 13		250	—	550	mV
HCSL Delta Vcross	D <sub>vcrs</sub>	Notes 10, 13		—	—	140	mV
HCSL Vovs	V <sub>ovs</sub>	Notes 10, 13		—	—	V <sub>HIGH</sub> +300	mV
HCSL Vuds	V <sub>uds</sub>	Notes 10, 13		—	—	V <sub>LOW</sub> -300	mV
HCSL Vrng	V <sub>rng</sub>	Notes 10, 13		V <sub>HIGH</sub> -200	—	V <sub>LOW</sub> +200	mV
Rise and Fall Times (20% to 80%)	t <sub>R</sub> /t <sub>F</sub>	HCSL		—	—	420	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Notes:</b>						
1. For best jitter performance, keep the midpoint differential input slew rate faster than 0.3 V/ns.						
2. For best jitter performance, keep the midpoint input single ended slew rate faster than 1 V/ns.						
3. Input capacitance on crystal pins targets 23 pf each plus 1 pf external trace capacitance to provide 12 pf series equivalent crystal load capacitance.						
4. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.						
5. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.						
6. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.						
7. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700), Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg).						
8. Measurement taken from Single Ended waveform.						
9. Measurement taken from differential waveform VLow Math function.						
10. Overshoot is defined as the absolute value of the maximum voltage.						
11. Undershoot is defined as the absolute value of the minimum voltage.						
12. The crossing point must meet the absolute and relative crossing point specifications simultaneously.						
13. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system.						
14. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.						

**Table 5.5. Performance Characteristics**

( $V_{DD} = V_{DDA} = V_{DD\_DIG} = V_{DD\_XTAL} = 1.8\text{ V to }3.3\text{ V } +5\%/-5\%$ ,  $V_{DDO} = 1.8\text{ V } \pm 5\%$ ,  $2.5\text{ V } \pm 5\%$ , or  $3.3\text{ V } \pm 5\%$ ,  $T_A = -40\text{ to }105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	$t_{VDD}$	0 V to $V_{DDmin}$	0.1	—	10	ms
Clock Stabilization from Power-up	$t_{STABLE}$	Time for clock outputs to appear after POR	—	15	25	ms
Spread Spectrum PP Frequency Deviation	SSDEV		0.1	—	2.5	%
0.5% Spread Frequency Deviation	SSDEV		0.4	0.45	0.5	%
Spread Spectrum Modulation Rate	SSDEV		30	31.5	33	kHz

**Notes:**

1. Default value is ~31.5 kHz.

**Table 5.6. PCI-Express Clock Outputs (100 MHz HCSL)**(V<sub>DD</sub> = V<sub>DDA</sub> = V<sub>DD\_DIG</sub> = V<sub>DD\_XTAL</sub> = 1.8 V to 3.3 V +5%/-5%, V<sub>DDO</sub> = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T<sub>A</sub> = -40 to 105 °C)

Parameter	Test Condition	SSC On/Off	Typ	Max	Units
PCIe Gen 1.1	Includes PLL BW 1.5–22 MHz, Peaking = 3 dB, Td = 10 ns, Ftrk = 1.5 MHz with BER = 1E-12 <sup>1</sup>	Off	11	19	ps RMS
		On	22	30	ps RMS
PCIe Gen 2.1	Includes PLL BW 5MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, Low Band, F < 1.5 MHz <sup>1</sup>	Off	0.02	0.026	ps RMS
		On	0.12	0.21	ps RMS
	Includes PLL BW 5 MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, High Band, 1.5 MHz < F < Nyquist <sup>1</sup>	Off	0.2	0.31	ps RMS
		On	0.8	1.3	ps RMS
PCIe Gen 3.0 Common Clock	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1 dB, Td = 12 ns, CDR = 10 MHz <sup>1, 2</sup>	Off	0.06	0.1	ps RMS
		On	0.26	0.36	ps RMS
PCIe Gen3.0 SRIS	Includes PLL BW 4 MHz Peaking = 2 dB and 1dB, Td = 12 ns CDR = 10 MHz <sup>1, 2</sup>	On	0.31	0.36	ps RMS
PCIe Gen 4.0 Common Clock	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1dB, Td = 12 ns, CDR = 10 MHz <sup>1, 2</sup>	Off	0.05	0.1	ps RMS
		On	0.26	0.36	ps RMS
PCIe Gen4.0 SRIS	Includes PLL BW 4 MHz Peaking = 2 dB and 1 dB, Td = 12 ns CDR = 10 MHz <sup>1, 2</sup>	On	0.31	0.36	ps RMS
PCIe Gen5.0 Common Clock		Off	0.025	0.04	Ps RMS
		On	0.1	0.15	Ps RMS
PCIe Gen5.0 SRIS		On	0.08	0.1	Ps RMS

**Note:**

1. All output clocks 100 MHz HCSL format. Jitter data taken from Clock Jitter Tool v.1.3.
2. Excludes oscilloscope sampling noise.

Table 5.7. Thermal Characteristics

Parameter	Symbol	Test Condition <sup>1</sup>	Value	Units
<b>Si52258 — 40 QFN</b>				
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Still Air	23.1	°C/W
		Air Flow 1 m/s	17.5	
		Air Flow 2 m/s	16.5	
Thermal Resistance, Junction to Case	$\theta_{JC}$		13.4	
Thermal Resistance, Junction to Board	$\theta_{JB}$		8.7	
	$\Psi_{JB}$	Still Air	8.4	
<b>Si52254 — 32 QFN</b>				
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Still Air	28.4	°C/W
		Air Flow 1 m/s	24	
		Air Flow 2 m/s	23	
Thermal Resistance, Junction to Case	$\theta_{JC}$		15.9	
Thermal Resistance, Junction to Board	$\theta_{JB}$		11.5	
	$\Psi_{JB}$	Still Air	11.2	
<b>Note:</b>				
1. Based on JEDEC standard 4-layer PCB.				

Table 5.8. Absolute Maximum Ratings<sup>1,2,3</sup>

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	$T_{STG}$		-55 to +150	°C
DC Supply Voltage	$V_{DD}$		-0.5 to 3.8	V
	$V_{DDA}$		-0.5 to 3.8	V
	$V_{DD_{xtal}}$		-0.5 to 3.8	V
	$V_{DDO}$		-0.5 to 3.8	V
Input Voltage Range	$V_I$	XIN/XOUT	-0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 k $\Omega$	2.0	kV
Junction Temperature	$T_{JCT}$		-55 to 125	°C
Soldering Temperature	$T_{PEAK}$		260	°C
Soldering Temperature Time at $T_{PEAK}$	$T_P$		20 to 40	sec

**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to [www.silabs.com/support/quality/pages/RoHSInformation.aspx](http://www.silabs.com/support/quality/pages/RoHSInformation.aspx).
3. The device is compliant with JEDEC J-STD-020.

## 6. Pin Descriptions

### 6.1 Si52258A-D01AM Pin Descriptions (40-QFN)

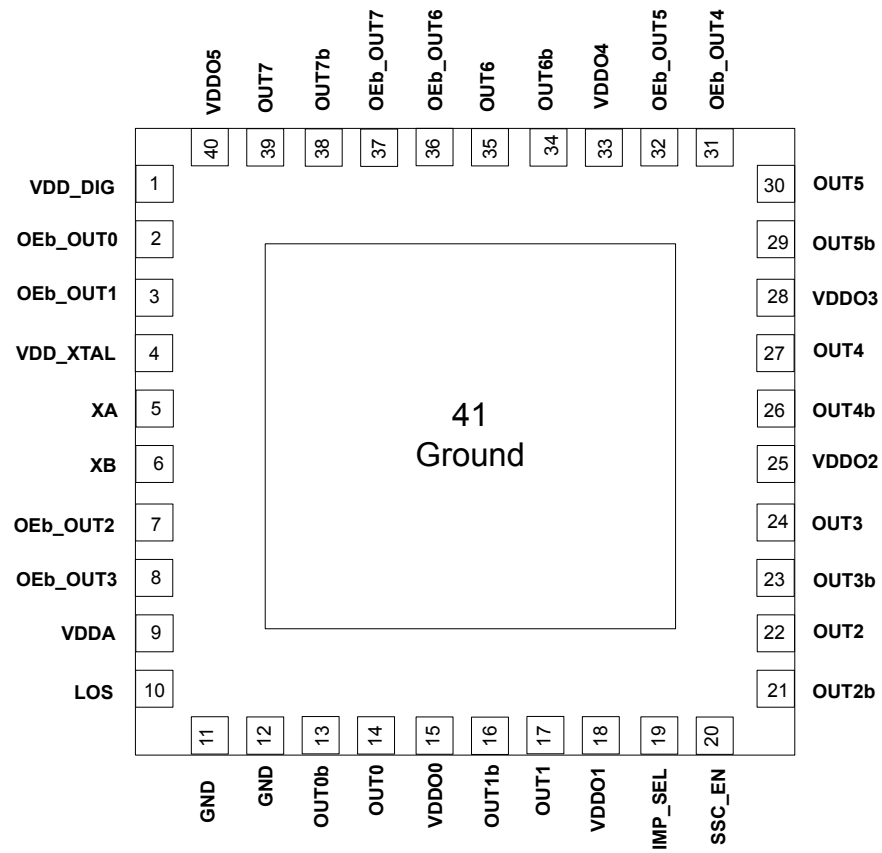


Figure 6.1. 40-QFN

Table 6.1. Si52258A-D01AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL.
2	OEb_OUT0	I	Output enable pin for OUT1. Default low. Low = output enabled High = output disabled
3	OEb_OUT1	I	Output enable pin for OUT1. Default low. Low = output enabled High = output disabled
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	XA	I	Connect to 25 MHz input crystal. Refer to Section 5. <a href="#">Electrical Specifications</a> for recommended crystal specifications.
6	XB	O	
7	OEb_OUT2	I	Output enable pin for OUT2. Default low. Low = output enabled High = output disabled
8	OEb_OUT3	I	Output enable pin for OUT3. Default low. Low = output enabled High = output disabled
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
10	LOS	O	The LOS status pin indicates whether the reference input has dropped below 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected.  0 = reference input has dropped below 10 MHz 1 = reference input is present (>10 MHz)
11	GND	—	Connect this pin to ground.
12	GND	—	Connect this pin to ground.
13	OUT0b	O	<b>Output Clock</b>
14	OUT0	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
15	VDDO0	P	<b>Supply Voltage (1.8–3.3 V) for OUT0</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.

Pin Number	Pin Name	Pin Type	Function
16	OUT1b	O	<b>Output Clock</b>
17	OUT1	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
18	VDDO1	P	<b>Supply Voltage (1.8–3.3 V) for OUT1</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	IMP_SEL	I	Impedance select pin for output drivers. Default low. IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
20	SSC_EN	I	Spread spectrum enable pin. Default low. Low = spread OFF High = spread ON (–0.5%)
21	OUT2b	O	<b>Output Clock</b>
22	OUT2	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
23	OUT3b	O	<b>Output Clock</b>
24	OUT3	O	Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
25	VDDO2	P	<b>Supply Voltage (1.8–3.3 V) for OUT2 and OUT3</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	<b>Output Clock</b>
27	OUT4	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
28	VDDO3	P	<b>Supply Voltage (1.8–3.3 V) for OUT4 and OUT5</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	<b>Output Clock</b>
30	OUT5	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
31	OEb_OUT4	I	Output enable pin for OUT4. Default low. Low = output enabled High = output disabled



Pin Number	Pin Name	Pin Type	Function
32	OEb_OUT5	I	Output enable pin for OUT5. Default low. Low = output enabled High = output disabled
33	VDDO4	P	<b>Supply Voltage (1.8–3.3 V) for OUT6</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	<b>Output Clock</b> 100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
35	OUT6	O	
36	OEb_OUT6	I	Output enable pin for OUT6. Default low. Low = output enabled High = output disabled
37	OEb_OUT7	I	Output enable pin for OUT7. Default low. Low = output enabled High = output disabled
38	OUT7b	O	<b>Output Clock</b> 100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
39	OUT7	O	
40	VDDO5	P	<b>Supply Voltage (1.8–3.3 V) for OUT7</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	GND PAD	P	<b>Ground Pad</b> This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 6.2 Si5224A-D01AM Pin Descriptions (32-QFN)

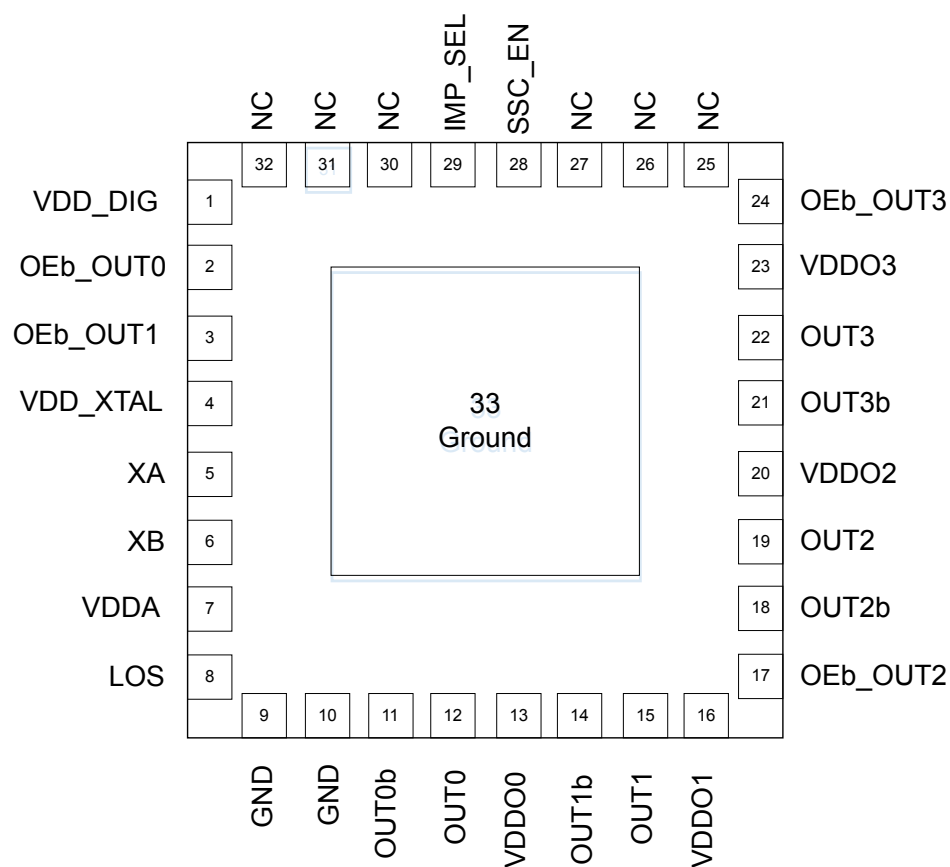


Figure 6.2. 32-QFN

Table 6.2. Si5224A-D01AM Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL.
2	OEb_OUT0	I	Output enable pin for OUT0. Default low. Low = output enabled High = output disabled
3	OEb_OUT1	I	Output enable pin for OUT1. Default low. Low = output enabled High = output disabled
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG."
5	XA	I	Refer to Section 5. <a href="#">Electrical Specifications</a> for recommended crystal specifications.
6	XB	O	

Pin Number	Pin Name	Pin Type	Function
7	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. See the <a href="#">Si5332-AM1/2/3 Family Reference Manual</a> for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
8	LOS	O	The LOS status pin indicates whether the reference input has dropped below 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below 10 MHz 1 = reference input is present (>10 MHz)
9	GND	P	Connect these pins to ground.
10	GND	P	
11	OUT0b	O	<b>Output Clock</b>
12	OUT0	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
13	VDDO0	P	<b>Supply Voltage (1.8–3.3 V) for OUT0</b> See the <a href="#">Si5332-AM1/2/3 Family Reference Manual</a> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	O	<b>Output Clock</b>
15	OUT1	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
16	VDDO1	P	<b>Supply Voltage (1.8–3.3 V) for OUT1</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	OEb_OUT2	I	Output enable pin for OUT2. Default low. Low = output enabled High = output disabled
18	OUT2b	O	<b>Output Clock</b>
19	OUT2	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.
20	VDDO2	P	<b>Supply Voltage (1.8–3.3 V) for OUT2</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
21	OUT3b	O	<b>Output Clock</b>
22	OUT3	O	100 MHz HCSL output. Termination recommendations are provided in <a href="#">3.3 HCSL Differential Output Terminations</a> . Unused outputs should be left unconnected.

Pin Number	Pin Name	Pin Type	Function
23	VDDO3	P	<b>Supply Voltage (1.8–3.3 V) for OUT3</b> Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
24	OEb_OUT3	I	Output enable pin for OUT3. Default low. Low = output enabled High = output disabled
25	NC	—	Do not connect these pins to anything.
26	NC	—	
27	NC	—	
28	SSC_EN	I	Spread spectrum enable pin. Default low. Low = spread OFF High = spread ON (–0.5%)
29	IMP_SEL	I	Impedance select pin for output drivers. Default low. IMP_SEL pin is sampled at power-up only. Low = 100 $\Omega$ High = 85 $\Omega$
30	NC	—	Do not connect these pins to anything.
31	NC	—	
32	NC	—	
33	GND PAD	P	<b>Ground Pad</b> This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 7. Package Outline

### 7.1 Si52258A-D01AM 6x6 mm 40-QFN Package Diagram

The figure below illustrates the package details for the Si52258A-D01AM in 40-QFN. The table below lists the values for the dimensions shown in the illustration.

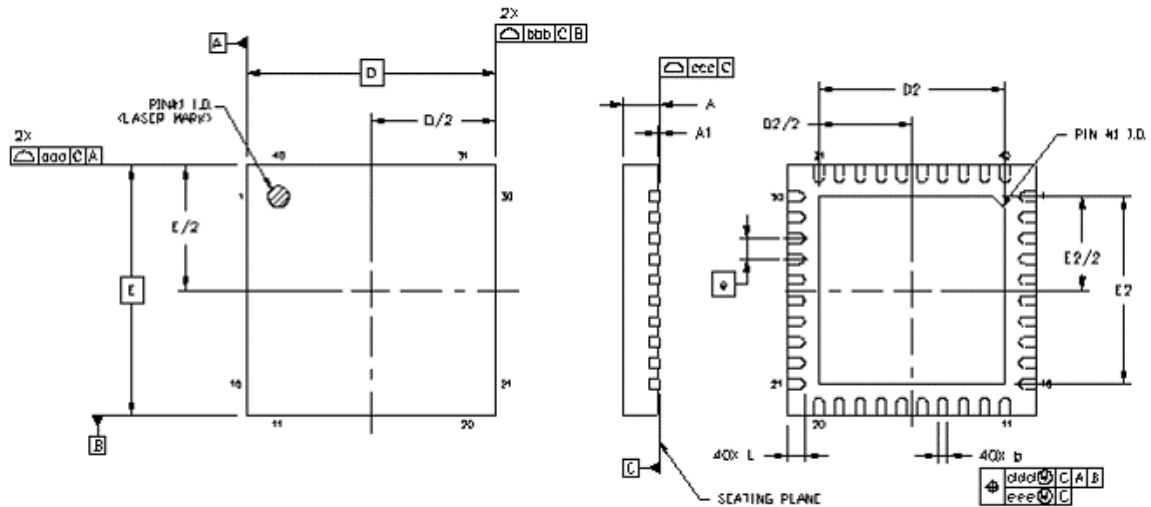


Figure 7.1. 40-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	6.00 BSC		
D2	4.35	4.50	4.65
e	0.50 BSC		
E	6.00 BSC		
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Dimension	Min	Nom	Max
<p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li><li>2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li><li>3. This drawing conforms to the JEDEC Solid State Outline MO-220.</li><li>4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li></ol>			

### 7.2 Si52254A-D01AM 5x5 mm 32-QFN Package Diagram

The figure below illustrates the package details for the Si52254A-D01AM 32-QFN option. The table below lists the values for the dimensions shown in the illustration.



Figure 7.2. 32-Pin Quad Flat No-Lead (QFN)

Table 7.2. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa	0.15		
bbb	0.10		
ccc	0.10		

Dimension	MIN	NOM	MAX
ddd		0.05	
eee		0.08	
fff		0.10	

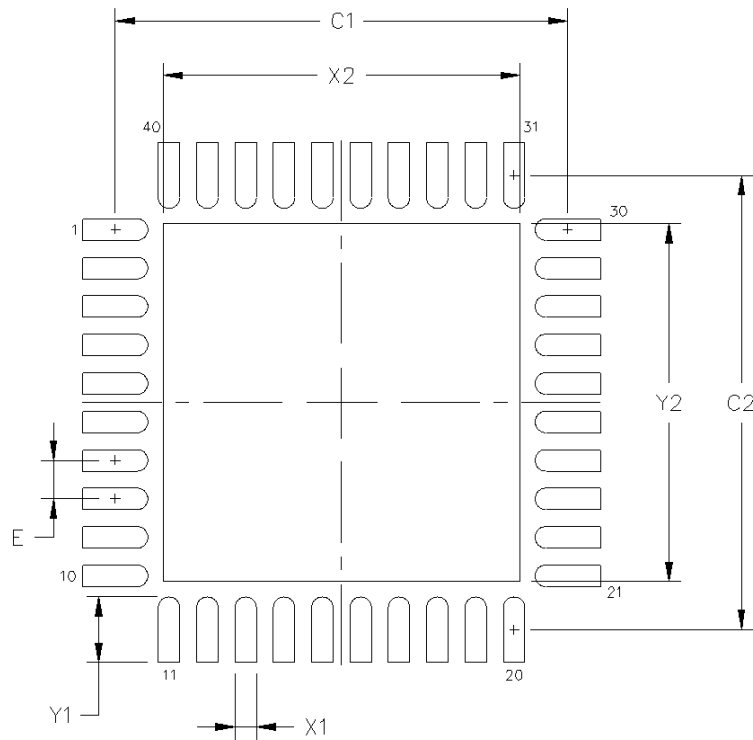
**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



## 8. PCB Land Pattern

### 8.1 Si52258A-D01AM 40-QFN Land Pattern



**Figure 8.1. 40-QFN Land Pattern**

**Table 8.1. PCB Land Pattern Dimensions**

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm
<p><b>Notes:</b></p> <p><b>General</b></p> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li><li>2. This Land Pattern Design is based on the IPC-7351 guidelines.</li></ol> <p><b>Solder Mask Design</b></p> <ol style="list-style-type: none"><li>1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu\text{m}</math> minimum, all the way around the pad.</li></ol> <p><b>Stencil Design</b></p> <ol style="list-style-type: none"><li>1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li><li>2. The stencil thickness should be 0.125 mm (5 mils).</li><li>3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.</li><li>4. A 3<math>\times</math>3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.</li></ol> <p><b>Card Assembly</b></p> <ol style="list-style-type: none"><li>1. A No-Clean, Type-3 solder paste is recommended.</li><li>2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li></ol>	

## 8.2 Si52254A-D01AM 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for Si52254A-D01AM in 32-QFN package. The table below lists the values for the dimensions shown in the illustration.

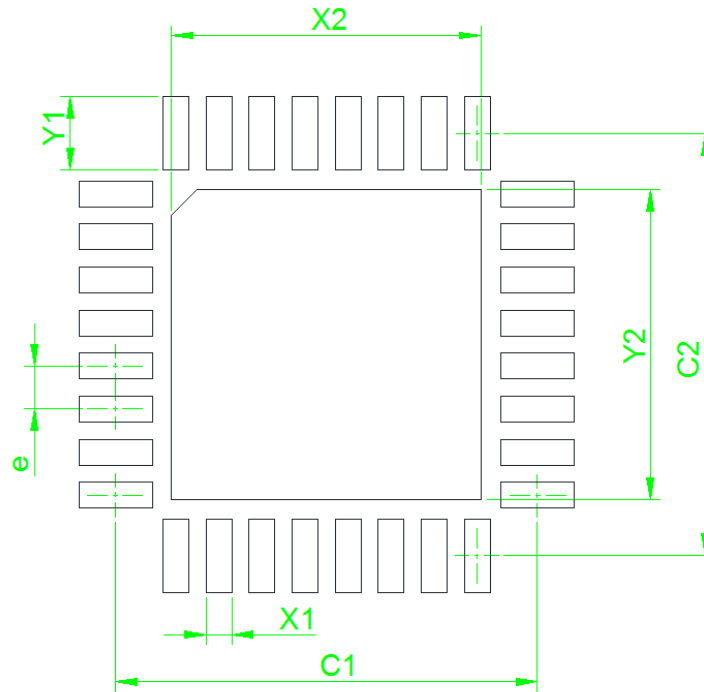


Figure 8.2. 32-QFN Land Pattern

Table 8.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm
<p><b>Notes:</b></p> <p><b>General</b></p> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li><li>2. This Land Pattern Design is based on the IPC-7351 guidelines.</li></ol> <p><b>Solder Mask Design</b></p> <ol style="list-style-type: none"><li>1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu\text{m}</math> minimum, all the way around the pad.</li></ol> <p><b>Stencil Design</b></p> <ol style="list-style-type: none"><li>1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li><li>2. The stencil thickness should be 0.125 mm (5 mils).</li><li>3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.</li><li>4. A 3<math>\times</math>3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.</li></ol> <p><b>Card Assembly</b></p> <ol style="list-style-type: none"><li>1. A No-Clean, Type-3 solder paste is recommended.</li><li>2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li></ol>	

## 9. Top Marking

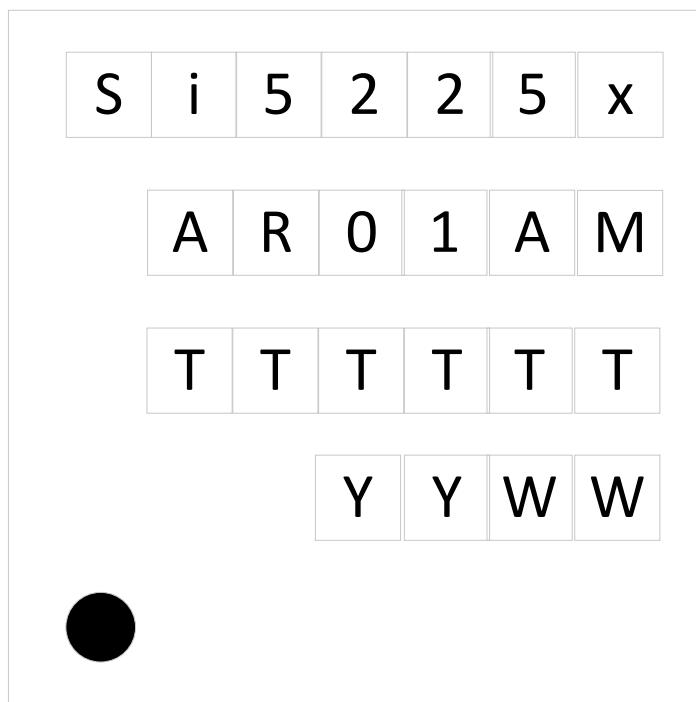


Figure 9.1. Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description
1	Si52258 Si52254	Base part number
2	AD01AM	A = Grade R = Product revision (reference ordering section for latest revision) 01 = Product identification, single input AM = Automotive temperature grade. Package (QFN)
3	TTTTTT	Manufacturing trace code.
4	YYWW	Year (YY) and work week (WW) of package assembly

## 10. Revision History

### Revision 0.7

September, 2019

- Initial release.



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