Si53212/Si53208/Si53204 数据表

12/8/4 路输出 PCI-Express 低抖动、低功耗第 1/2/3/4 代 SRIS 时钟缓冲器

Si53212、Si53208 和 Si53204 是业界性能极高、附加抖动较低的低功耗 PCIe 时钟扇出缓冲器产品系列，可以获得 12、8 或 4 路 100 MHz 的 PCIe 时钟输出。所有差分时钟输出均符合 PCIe Gen1/2/3/4 公共时钟和单独参考时钟规格。该缓冲器产品系列支持扩频，可以用于对输入时钟进行扩频直通。每种设备都具有单独的硬件输出使能控制引脚，可用于启用和禁用差分输出。除了支持 100 MHz 的频率外，设备还支持 10 MHz 到 200 MHz 的输入频率。所有设备都以小型 QFN 封装。小尺寸和低功耗使该产品系列 PCIe 时钟扇出缓冲器成为工业和消费类应用的理想选择。为确保 PCI-Express 合规，Silicon Labs PCIe 时钟抖动工具使测量 PCIe 时钟抖动的过程变得快速而轻松。可从此处免费下载：http://www.silabs.com/pcie-learningcenter。

应用

- 数据中心
- 服务器
- 存储
- PCIe 附加卡
- 通讯
- 工业

主要特点

- 12/8/4 路输出 100 MHz PCIe 第 1/2/3/4 代和支持 SRIS 的时钟扇出缓冲器
- 低功耗推拉式、HCSL 兼容差分输出
- 10 MHz 到 200 MHz 的时钟输入
- 支持扩频，以对输入时钟进行扩频直通，实现 EMI 降低
- 支持 Intel QPI/UPI 标准
- 单电源 1.5 至 1.8 V
- 85 Ω和 100 Ω终端订购选项
- 温度范围：-40 至 85 °C
- 封装选项：
  - 64 引脚 QFN (9 x 9 mm)：12 路输出
  - 48 引脚 QFN (6 x 6 mm)：8 路输出
  - 32 引脚 QFN (5 x 5 mm)：4 路输出
- 小型 QFN 封装
- 无铅、符合 RoHS-6

1. 功能列表

- 12/8/4 路输出 100 MHz PCIe 第 1/2/3/4 代和支持 SRIS 的时钟扇出缓冲器
- 低功耗推拉式、HCSL 兼容差分输出、10 MHz 到 200 MHz 的时钟输入
- 支持扩频，以对输入时钟进行扩频直通，实现 EMI 降低
- 完全支持 Intel QPI/UPI 抖动要求
- 内部 100 Ω 或 85 Ω 输出终端
  - 消除外部终端电阻，以节省电路板空间
- 单电源 1.5 至 1.8 V
- 温度范围：-40° C 至 85° C
- 封装选项：
  - 64 引脚 QFN（9 x 9 mm）：12 路输出
  - 48 引脚 QFN（6 x 6 mm）：8 路输出
  - 32 引脚 QFN（5 x 5 mm）：4 路输出
- 无铅、符合 RoHS-6

2. Ordering Guide

Number of Outputs	Internal Termination	Part Number	Package Type	Temperature
12-output	100 Ω	Si53212-A01AGM	64-QFN	Extended, –40 to 85 °C
		Si53212-A01AGMR	64-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53212-A02AGM	64-QFN	Extended, –40 to 85 °C
		Si53212-A02AGMR	64-QFN, Tape and Reel	Extended, –40 to 85°C
8-output	100 Ω	Si53208-A01AGM	48-QFN	Extended, –40 to 85 °C
		Si53208-A01AGMR	48-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53208-A02AGM	48-QFN	Extended, –40 to 85 °C
		Si53208-A02AGMR	48-QFN, Tape and Reel	Extended, –40 to 85 °C
4-output	100 Ω	Si53204-A01AGM	32-QFN	Extended, –40 to 85 °C
		Si53204-A01AGMR	32-QFN, Tape and Reel	Extended, –40 to 85 °C
	85 Ω	Si53204-A02AGM	32-QFN	Extended, –40 to 85 °C
		Si53204-A02AGMR	32-QFN, Tape and Reel	Extended, –40 to 85 °C

2.1 Technical Support

Table 2.1. Technical Support URLs

Frequently Asked Questions	https://www.silabs.com/community/timing/knowledge-base.entry.html/2018/02/26/si532xx_si53204_si53-LO33 http://www.silabs.com/Si532xx-FAQ
PCIe Clock Jitter Tool	www.silabs.com/products/timing/pci-express-learning-center
PCIe Learning Center	www.silabs.com/products/timing/pci-express-learning-center
Development Kit	https://www.silabs.com/products/development-tools/timing/clock-buffer/si53208-evaluation-kit.html

Table of Contents

3. Functional Block Diagrams

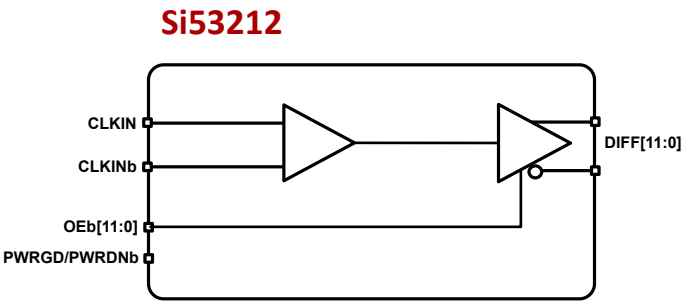


Figure 3.1. Si53212 Block Diagram

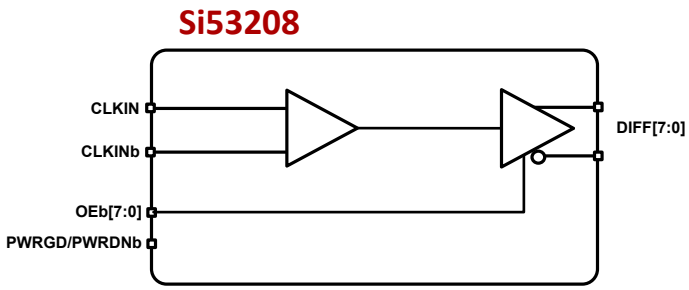


Figure 3.2. Si53208 Block Diagram

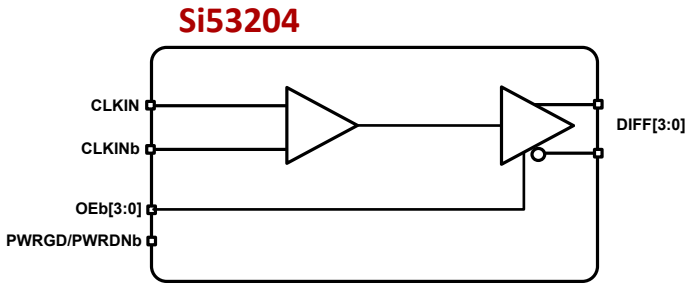


Figure 3.3. Si53204 Block Diagram

4. Electrical Specifications

Table 4.1. DC Electrical Specifications (VDD = 1.5 V ±5%)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.5 V Operating Voltage	VDD core	1.5 V ±5%	1.425	1.5	1.575	V
Output Supply Voltage	VDDIO	Supply voltage for differential Low Power outputs	0.9975	1.05 to 1.5	1.575	V
1.5 V Input High Voltage	VIH	Control input pins	0.75 VDD	—	VDD + 0.3	V
1.5 V Input Mid Voltage	VIM	Tri-level control input pins	0.4 VDD	0.5 VDD	0.6 VDD	V
1.5 V Input Low Voltage	VIL	Control input pins	–0.3	—	0.25 VDD	V
Input current	IIN	Single-ended inputs, VIN = GND, VIN = VDD	–5		5	µA
	IINP	Single-ended inputs, VIN = 0 V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200		200	µA
Input Pin Capacitance	CIN		1.5	—	5	pF
Output Pin Capacitance	COUT		—	—	6	pF
Pin Inductance	LIN		—	—	7	nH
Si53212 Current Consumption (VDD = 1.5 V ±5%)						
Power Down Current	IDD_PD_total		—	1.3	1.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	.75	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	0.5	mA
Dynamic Supply Current	IDD_1.5V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	60	71.5	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	12	13	mA
	IDD_AOP	VDDA, all differential outputs active at 100MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	46	55.5	mA
Si53208 Current Consumption (VDD = 1.5 V ±5%)						
Power Down Current	IDD_PD_total		—	1.3	1.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	.75	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	0.5	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	IDD_1.5V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	42	51.5	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	10	11	mA
	IDD_AOP	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	30	37.5	mA
Si53204 Current Consumption (VDD = 1.5 V ±5%)						
Power Down Current	IDD_PD_total		—	1.3	1.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.4	.75	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	0.5	mA
Dynamic Supply Current	IDD_1.5V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	26	31.5	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	8.5	9.5	mA
	IDD_AOP	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	15.5	19	mA

Table 4.2. DC Electrical Specifications (VDD = 1.8 V ±5%)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1.8 V Operating Voltage	VDD core	1.8 V ±5%	1.71	1.8	1.89	V
Output Supply Voltage	VDDIO	Supply voltage for differential Low Power outputs	0.9975	1.05 to 1.8	1.9	V
1.8 V Input High Voltage	VIH	Control input pins	0.75 VDD	—	VDD + 0.3	V
1.8 V Input Mid Voltage	VIM	Tri-level control input pins	0.4 VDD	0.5 VDD	0.6 VDD	V
1.8 V Input Low Voltage	VIL	Control input pins	–0.3	—	0.25 VDD	V
Input current	IIN	Single-ended inputs, VIN = GND, VIN = VDD	–5	—	5	µA
	IINP	Single-ended inputs, VIN = 0V, inputs with internal pull-up resistors VIN = VDD, inputs with internal pull-down resistors	–200	—	200	µA
Input Pin Capacitance	CIN		1.5	—	5	pF
Output Pin Capacitance	COUT		—	—	6	pF
Pin Inductance	LIN		—	—	7	nH
Si53212 Current Consumption (VDD = 1.8 V ±5%)						
Power Down Current	IDD_PD_total		—	1.4	2.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	.65	mA
Dynamic Supply Current	IDD_1.8V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	61	74	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	12	14.5	mA
	IDD_AOP	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	47	56.5	mA
Si53208 Current Consumption (VDD = 1.8 V ±5%)						
Power Down Current	IDD_PD_total			1.4	2.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	.65	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Dynamic Supply Current	IDD_1.8V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	44	53.5	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz	—	10.5	12.5	mA
	IDD_AOP	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	31	38	mA
Si53204 Current Consumption (VDD = 1.8 V ±5%)						
Power Down Current	IDD_PD_total		—	1.4	2.7	mA
	IDD_PD	VDD, except VDDA and VDD_IO, all outputs off	—	0.5	1.7	mA
	IDD_APD	VDDA, all outputs off	—	0.6	.75	mA
	IDD_IOPD	VDD_IO, all outputs off	—	0.3	.65	mA
Dynamic Supply Current	IDD_1.8V_Total	All outputs enabled. Differential clocks with 5” traces and 2 pF load.	—	27	33	mA
	IDD_OP	VDD, except VDDA and VDD_IO, all differential outputs active at 100 MHz		9	10.5	mA
	IDD_AOP	VDDA, all differential outputs active at 100 MHz	—	2.2	2.6	mA
	IDD_IOOP	VDD_IO, all differential outputs active at 100 MHz	—	16	19.5	mA

Table 4.3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CLKIN Frequency Range			10	—	200	MHz
CLKIN Rising and Falling Slew Rate for Each Clock Output Signal in a Given Differential Pair	TR/TF	Single-ended measurement: VOL = 0.175 to VOH = 0.525 V (Averaged)	0.6	—	4	V/ns
Differential Input High Voltage	VIH		150	—	—	mV
Differential Input Low Voltage	VIL		—	—	-150	mV
Crossing Point Voltage	VOX	Single-ended measurement	250	—	550	mV
Crossing Point Voltage (var)	VOX_DELTA	Single-ended measurement	—	—	140	mV
Differential Ringback Voltage	VRB		–100	—	100	mV
Time before Ringback Voltage	TSTABLE_RB		500	—	—	ps
Absolute maximum input voltage	VMAX		—	—	1150	mV
Absolute minimum input voltage	VMIN		–300	—		mV
Duty Cycle for Each Clock Output Signal in a Given Differential Pair	TDC	Measured at crossing point VOX	45	—	55	%
Rise/Fall Matching	TFRM	Determined as a fraction of 2 x (TR – TF)(TR + TF)	—	—	20	%
Control Input Pins						
Trise	Tr	Rise time of single-ended control inputs	—	—	5	ns
Tfall	Tf	Fall time fo single-ended control inputs	—	—	5	ns
DIFF at 0.7 V						
Output-to-Output Skew	TSKEW	Measured at 0 V differential	—	—	50	ps
Additive Cycle to Cycle Jitter	JADD_CCJ	Measured at 0 V differential	—	14	20	ps
Additive Phase Jitter		12 kHz–20 MHz	—	—	0.21	ps
PCIe Gen 1 Additive Pk-Pk Jitter	JADD_Pk-Pk	PCIe Gen 1	0	10	17	ps
PCIe Gen 2 Additive Phase Jitter	JADD_RMSGEN2	10 kHz < F < 1.5 MHz	0	.125	0.2	ps
		1.5 MHz < F < Nyquist	0	.003	.005	ps
PCIe Gen 3 Additive Phase Jitter	JADD_RMSGEN3	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.04	0.06	ps
PCIe Gen 3 SRIS Addtive Phase Jitter	JADD_RMSGen3_SRIS		—	0.055	0.07	ps
PCIe Gen 3 SRNS Additive Phase Jitter	JADD_RMSGen3_SRNS		—	0.035	0.043	ps
PCIe Gen 4 Additive Phase Jitter	JADD_RMSGen4		—	0.04	0.06	ps

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PCIe Gen 4 SRIS Additive Phase Jitter	JADD_RMSGen4_SRIS		—	0.055	0.07	ps
PCIe Gen 4 SRNS Additive Phase Jitter	JADD_RMSGen4_SRNS		—	0.035	0.043	ps
Slew Rate	TR/TF	Measured differentially from ±150 mV (fast setting)	—	2.4	3.7	V/ns
		Measured differentially from ±150 mV (slow setting)	—	1.9	2.9	V/ns
Slew Rate Matching	Delta TR/TF		—	—	10	%
Voltage High	VHIGH		600	—	850	mV
Voltage Low	VLOW		–150	—	150	mV
Max Voltage	VMAX		—	—	1150	mV
Min Voltage	VMIN		–300	—	—	mV
Enable/Disable and Setup						
Clock Stabilization from Power-up	TSTABLE	Minimum ramp rate 200 V/s	—	1	5	ms
OE_b Latency	TOEBLAT	Differential outputs start after OE_b assertion Differential outputs stop after OE_b deassertion		2	3.5	clocks
Intel QPI Specifications for 100 MHz and 133 MHz						
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	JADD_RMSQPI_SMI	4.8 Gb/s, 133 MHz, 12UI,7.8 M	—	.16	—	ps
		6.4 Gb/s, 133 MHz, 12UI,7.8 M	—	.12	—	ps
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	JADD_RMSQPI_SMI	8 Gb/s, 100 MHz, 12 UI	—	0.9	—	ps
Intel QPI and SMI REFCLK additive jitter[2, 3, 4]	JADD_RMSQPI_SMI	9.6 Gb/s, 100 MHz, 12UI	—	0.7	—	ps
Intel UPI Specifications for 100 MHz						
UPI Additive Phase Jitter (RMS)	J_{RMS_UPI}	Intel UPI 1–10 MHz	—	.67	—	ps

Note:

1. Silicon Labs PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt(output jitter^2 - input jitter^2). Input used is 100 MHz from Si5340.
2. Post processed evaluation through Intel supplied Matlab scripts.
3. Measuring on 100 MHz output using the template file in the PCIe Clock Jitter Tool.
4. Measuring on 100 MHz, 133 MHz outputs using the template file in the PCIe Jitter Tool. For complete PCIe specifications, visit www.pcisig.com.
5. Input clock slew rate of 3.0 V/ns used for jitter measurements.

5. Functional Description

5.1 OEb Pin

The OEb pin is an active low input used to enable and disable the output clock. To enable the output clock, the OEb pin needs to be logic low. By default, the OEb pin is set to logic low. To disable the output clock, the OEb pin is pulled to a logic high. The OEb pin is required to be driven at all times even though it has an internal pull-down resistor.

This pin has an internal 100 kΩ pull-down resistor.

5.2 OEb Assertion

The OEb pin is an active low input used for synchronous stopping and starting the respective output clock while the rest of the device continues to function. The assertion of the OEb function is achieved by pulling the OEb pin high, which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

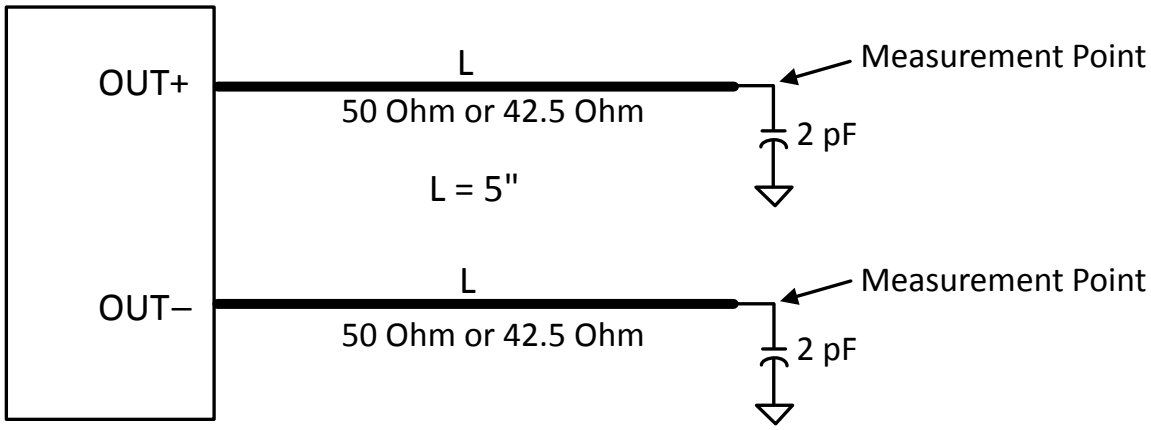
5.3 OEb Deassertion

The OEb function is deasserted by pulling the high. The corresponding output is stopped cleanly and the final output state is driven low.

6. Test and Measurement Setup

The figures below show the test load configuration for differential clock signals.

Figure 6.1. 0.7 V Differential Load Configuration



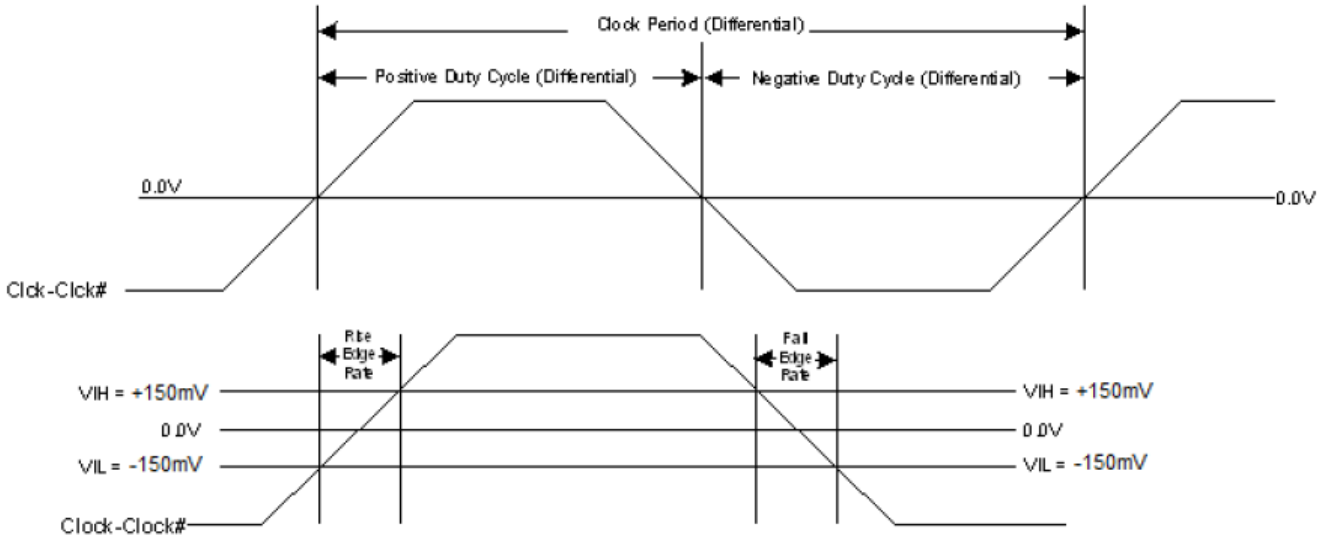


Figure 6.2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

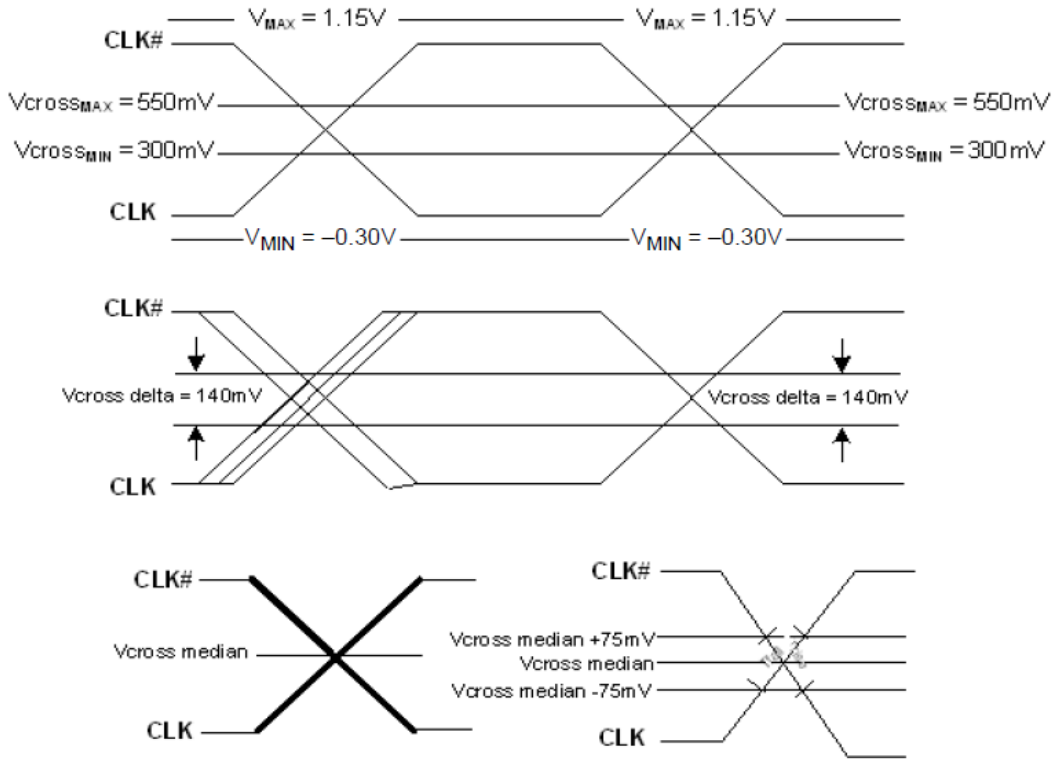


Figure 6.3. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

7. PCIe Clock Jitter Tool

The PCIe Clock Jitter Tool is designed to enable users to quickly and easily take jitter measurements for PCIe Gen1/2/3/4 and SRNS/SRIS. This software removes all the guesswork for PCIe Gen1/2/3/4 and SRNS/SRIS jitter measurements and margins in board designs.

This software tool will provide accurate results in just a few clicks, and is provided in an executable format to support various common input waveform files, such as .csv, .wfm, and .bin. The easy-to-use GUI and helpful tips guide users through each step. Release notes and other documentation are also included in the software package.

Download it for free http://www.silabs.com/pcie-learningcenter.

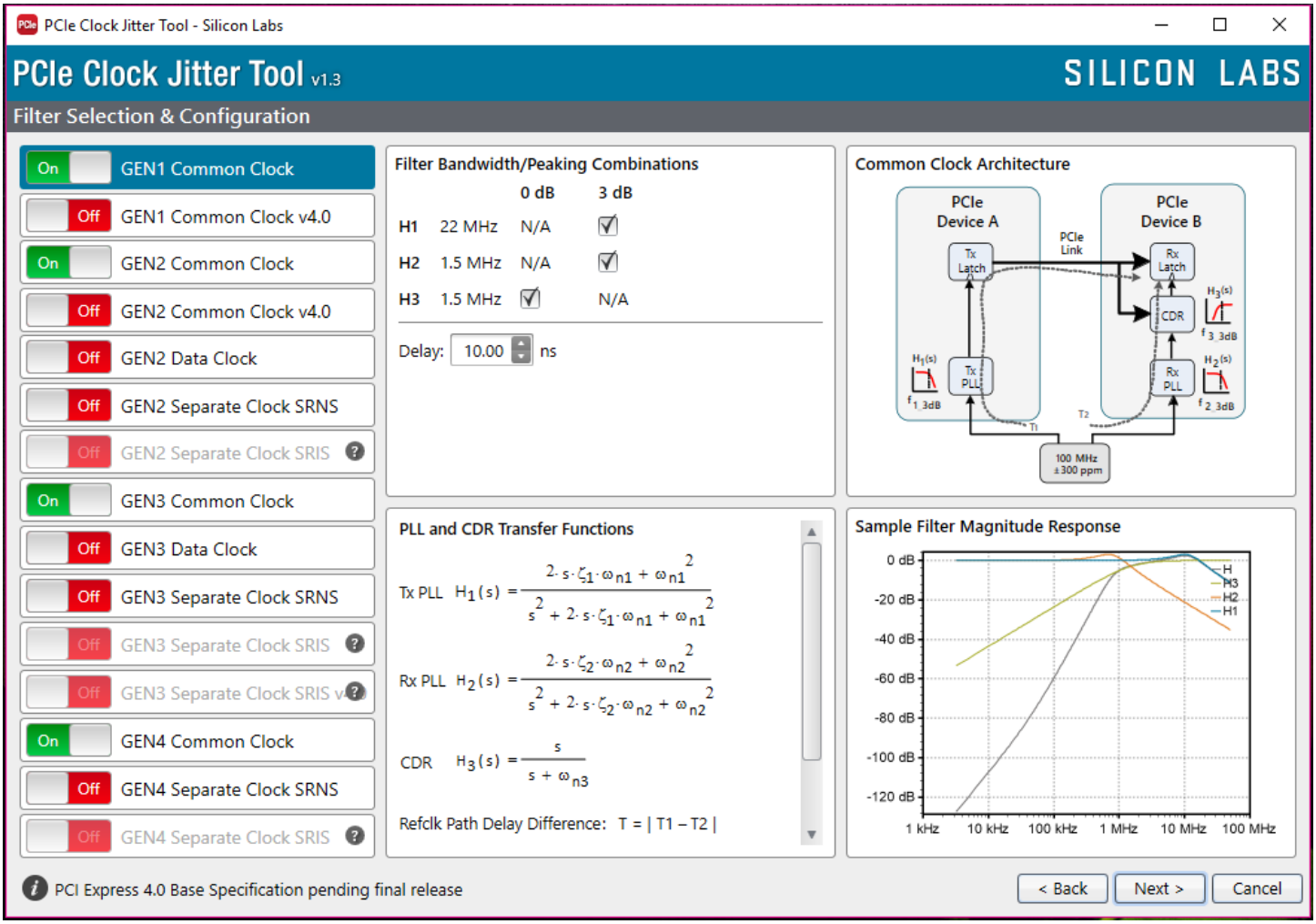


Figure 7.1. PCIe Clock Jittter Tool

8. Pin Descriptions

8.1 Si53212 Pin Descriptions

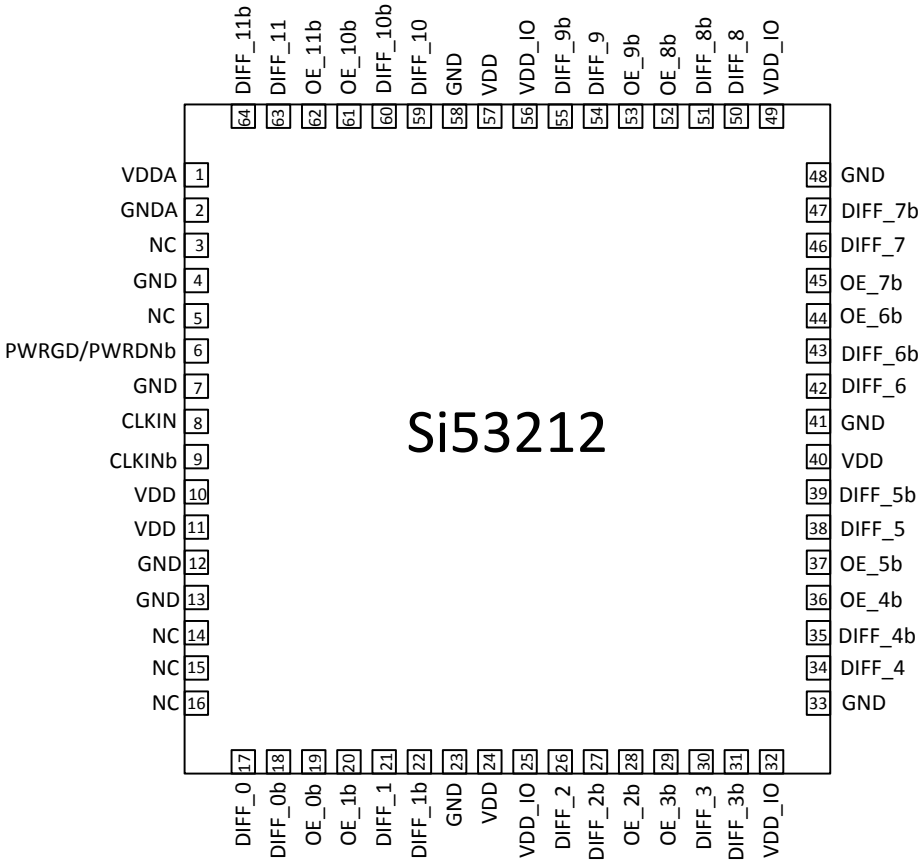


Figure 8.1. 64-Pin QFN

Table 8.1. Si53212 64-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	PWR	Analog Power Supply
2	GNDA	GND	Analog Ground
3	NC	NC	No connect
4	GND	GND	Ground
5	NC	NC	No connect
6	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal pull-up).
7	GND	GND	Ground
8	CLKIN	I	Clock input
9	CLKINb	I	Complementary clock input
10	VDD	PWR	Power supply
11	VDD	PWR	Power supply
12	GND	GND	Ground

Pin #	Name	Type	Description
13	GND	GND	Ground
14	NC	NC	No connect
15	NC	NC	No connect
16	NC	NC	No connect
17	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock
18	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock
19	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
20	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
21	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock
22	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
23	GND	GND	Ground
24	VDD	PWR	Power supply
25	VDD_IO	PWR	Output power supply
26	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock
27	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock
28	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
29	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
30	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock
31	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock
32	VDD_IO	PWR	Output power supply
33	GND	GND	Ground
34	DIFF_4	O, DIF	0.7 V, 100 MHz differential clock
35	DIFF_4b	O, DIF	0.7 V, 100 MHz differential clock
36	OE_4b	I, PD	Output enable for DIFF_4 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
37	OE_5b	I, PD	Output enable for DIFF_5 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
38	DIFF_5	O, DIF	0.7 V, 100 MHz differential clock
39	DIFF_5b	O, DIF	0.7 V, 100 MHz differential clock
40	VDD	PWR	Power supply
41	GND	GND	Ground
42	DIFF_6	O, DIF	0.7 V, 100 MHz differential clock
43	DIFF_6b	O, DIF	0.7 V, 100 MHz differential clock
44	OE_6b	I, PD	Output enable for DIFF_6 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs

Pin #	Name	Type	Description
45	OE_7b	I, PD	Output enable for DIFF_7 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
46	DIFF_7	O, DIF	0.7 V, 100 MHz differential clock
47	DIFF_7b	O, DIF	0.7 V, 100 MHz differential clock
48	GND	GND	Ground
49	VDD_IO	PWR	Output power supply
50	DIFF_8	O, DIF	0.7 V, 100 MHz differential clock
51	DIFF_8b	O, DIF	0.7 V, 100 MHz differential clock
52	OE_8b	I, PD	Output enable for DIFF_8 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
53	OE_9b	I, PD	Output enable for DIFF_9 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
54	DIFF_9	O, DIF	0.7 V, 100 MHz differential clock
55	DIFF_9b	O, DIF	0.7 V, 100 MHz differential clock
56	VDD_IO	PWR	Output power supply
57	VDD	PWR	Power supply
58	GND	GND	Ground
59	DIFF_10	O, DIF	0.7 V, 100 MHz differential clock
60	DIFF_10b	O, DIF	0.7 V, 100 MHz differential clock
61	OE_10b	I, PD	Output enable for DIFF_10 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
62	OE_11b	I, PD	Output enable for DIFF_11 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
63	DIFF_11	O, DIF	0.7 V, 100 MHz differential clock
64	DIFF_11b	O, DIF	0.7 V, 100 MHz differential clock

8.2 Si53208 Pin Descriptions

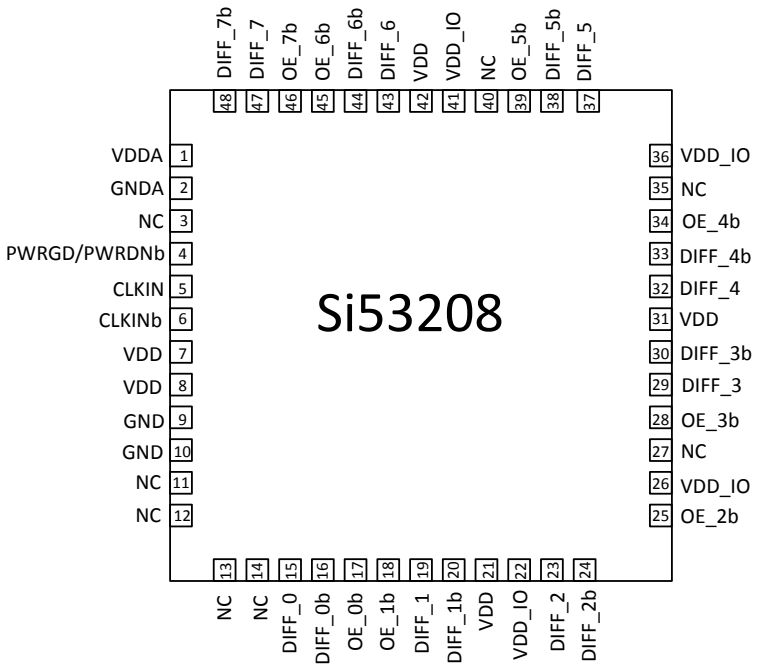


Figure 8.2. 48-pin QFN

Table 8.2. Si53208 48-pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	PWR	Analog Power Supply
2	GNDA	GND	Analog Ground
3	NC	NC	No connect
4	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal pull-up).
5	CLKIN	I	Clock input.
6	CLKINb	I	Complementary clock input
7	VDD	PWR	Power supply
8	VDD	PWR	Power supply
9	GND	GND	Ground
10	GND	GND	Ground
11	NC	NC	No connect
12	NC	NC	No connect
13	NC	NC	No connect
14	NC	NC	No connect
15	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock
16	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock
17	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs

Pin #	Name	Type	Description
18	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
19	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock
20	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
21	VDD	PWR	Power supply
22	VDD_IO	PWR	Output power supply
23	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock
24	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock
25	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
26	VDD_IO	PWR	Output power supply
27	NC	NC	No connect
28	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
29	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock
30	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock
31	VDD	PWR	Power supply
32	DIFF_4	O, DIF	0.7 V, 100 MHz differential clock
33	DIFF_4b	O, DIF	0.7 V, 100 MHz differential clock
34	OE_4b	I, PD	Output enable for DIFF_4 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
35	NC	NC	No connect
36	VDD_IO	PWR	Output power supply
37	DIFF_5	O, DIF	0.7 V, 100 MHz differential clock
38	DIFF_5b	O, DIF	0.7 V, 100 MHz differential clock
39	OE_5b	I, PD	Output enable for DIFF_5 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
40	NC	NC	No connect
41	VDD_IO	PWR	Output power supply
42	VDD	PWR	Power supply
43	DIFF_6	O, DIF	0.7 V, 100 MHz differential clock
44	DIFF_6b	O, DIF	0.7 V, 100 MHz differential clock
45	OE_6b	I, PD	Output enable for DIFF_6 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
46	OE_7b	I, PD	Output enable for DIFF_7 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
47	DIFF_7	O, DIF	0.7 V, 100 MHz differential clock
48	DIFF_7b	O, DIF	0.7 V, 100 MHz differential clock

8.3 Si53204 Pin Descriptions

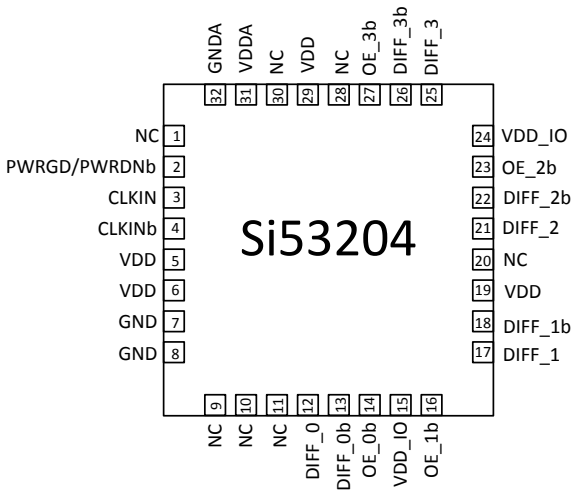


Figure 8.3. 32-pin QFN

Table 8.3. Si53204 32-pin QFN Descriptions

Pin #	Name	Type	Description
1	NC	NC	No connect
2	PWRGD/ PWRDNb	I, PU	Active low input pin asserts power down (PWRDNb) and disables all outputs (This pin has an internal pull-up).
3	CLKIN	I	Clock input.
4	CLKINb	I	Complementary clock input
5	VDD	PWR	Power supply
6	VDD	PWR	Power supply
7	GND	GND	Ground
8	GND	GND	Ground
9	NC	NC	No connect
10	NC	NC	No connect
11	NC	NC	No connect
12	DIFF_0	O, DIF	0.7 V, 100 MHz differential clock
13	DIFF_0b	O, DIF	0.7 V, 100 MHz differential clock
14	OE_0b	I, PD	Output enable for DIFF_0 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
15	VDD_IO	PWR	Output power supply
16	OE_1b	I, PD	Output enable for DIFF_1 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
17	DIFF_1	O, DIF	0.7 V, 100 MHz differential clock
18	DIFF_1b	O, DIF	0.7 V, 100 MHz differential clock
19	VDD	PWR	Power supply
20	NC	NC	No connect

Pin #	Name	Type	Description
21	DIFF_2	O, DIF	0.7 V, 100 MHz differential clock
22	DIFF_2b	O, DIF	0.7 V, 100 MHz differential clock
23	OE_2b	I, PD	Output enable for DIFF_2 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
24	VDD_IO	PWR	Output power supply
25	DIFF_3	O, DIF	0.7 V, 100 MHz differential clock
26	DIFF_3b	O, DIF	0.7 V, 100 MHz differential clock
27	OE_3b	I, PD	Output enable for DIFF_3 pair (This pin has an internal pull-down). 0 = Enable outputs; 1 = Disable outputs
28	NC	NC	No connect
29	VDD	PWR	Power supply
30	NC	NC	No connect
31	VDDA	PWR	Analog Power Supply
32	GNDA	GND	Analog Ground

9. Packaging

9.1 Si53212 Package

The figure below illustrates the package details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

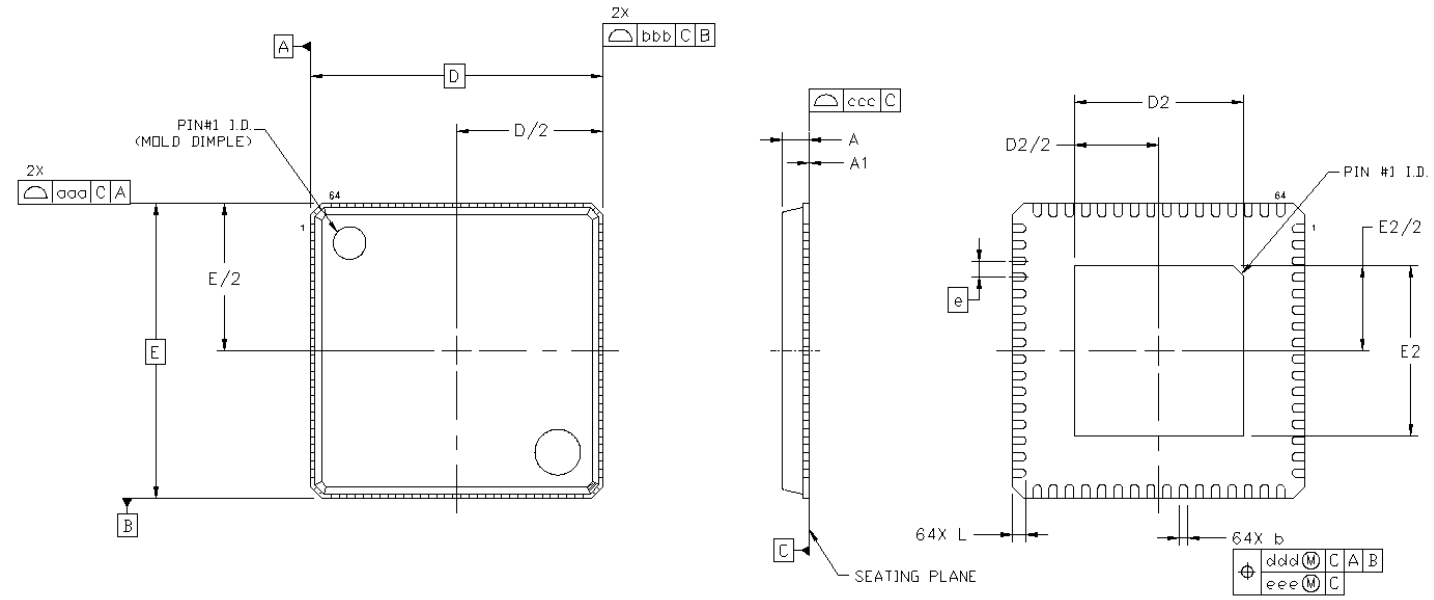


Figure 9.1. 64L 9 x 9 mm QFN Package Diagram

Table 9.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020D specification for Small Body Components.

9.2 Si53212 Land Pattern

The following figure illustrates the land pattern details for the Si53212 in a 64-Lead 9 x 9 mm QFN package. The table lists the values for the dimensions shown in the illustration.

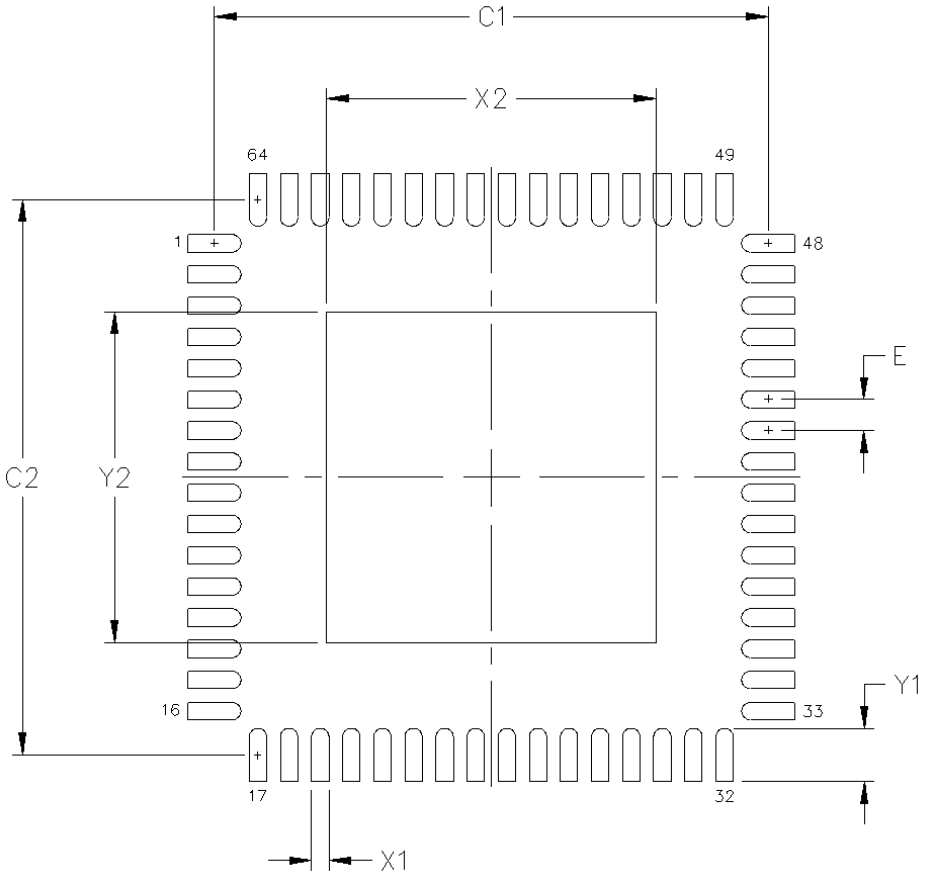


Figure 9.2. 64L 9 x 9 mm QFN Land Pattern

Table 9.2. PCB Land Pattern Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Dimension	mm

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.25 mm square openings on a 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 Si53208 Package

The figure below illustrates the package details for the Si53208 in a 48-Lead 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

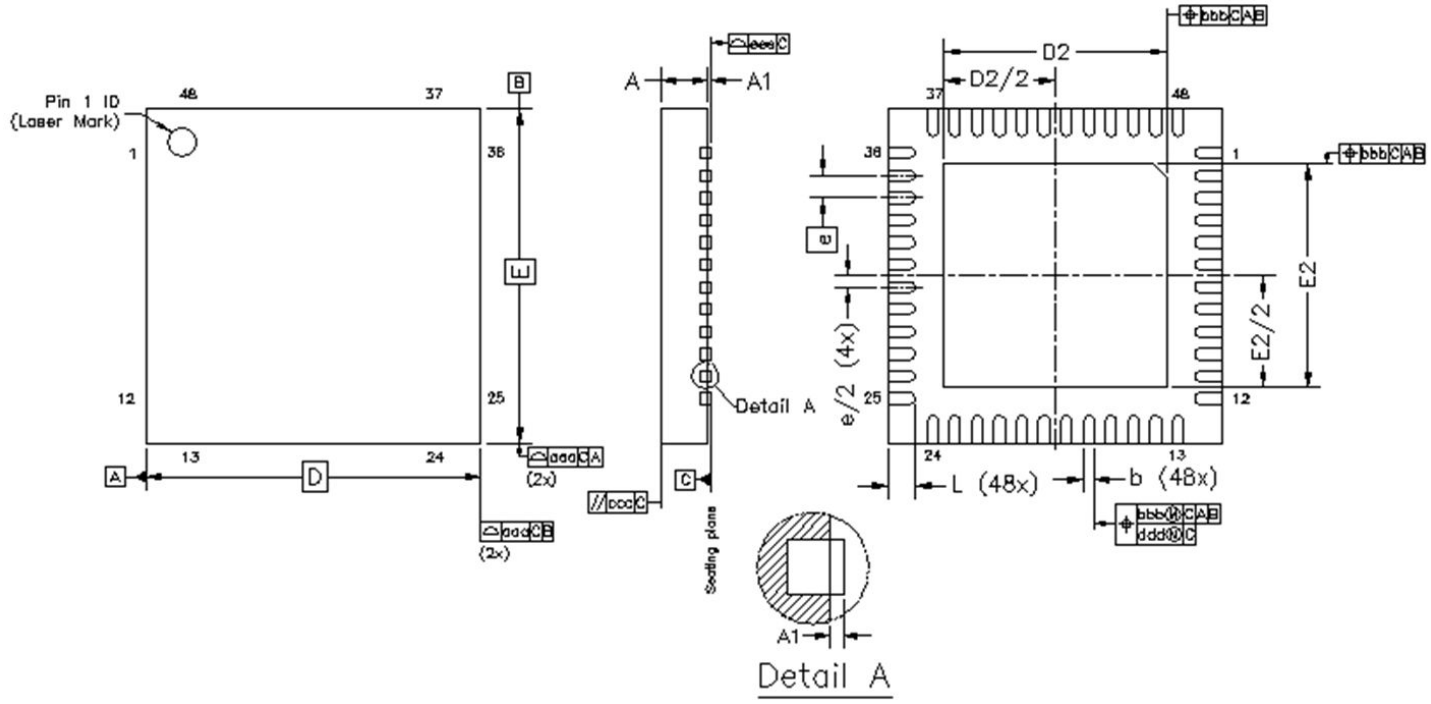


Figure 9.3. 48L 6 x 6 mm QFN Package Diagram

Table 9.3. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		6.00 BSC	
D2	3.5	3.6	3.7
e		0.40 BSC	
E		6.00 BSC	
E2	3.5	3.6	3.7
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

9.4 Si53208 Land Pattern

The figure below illustrates the land pattern details for the Si53208 in a 48-Lead, 6 x 6 mm QFN package. The table lists the values for the dimensions shown in the illustration.

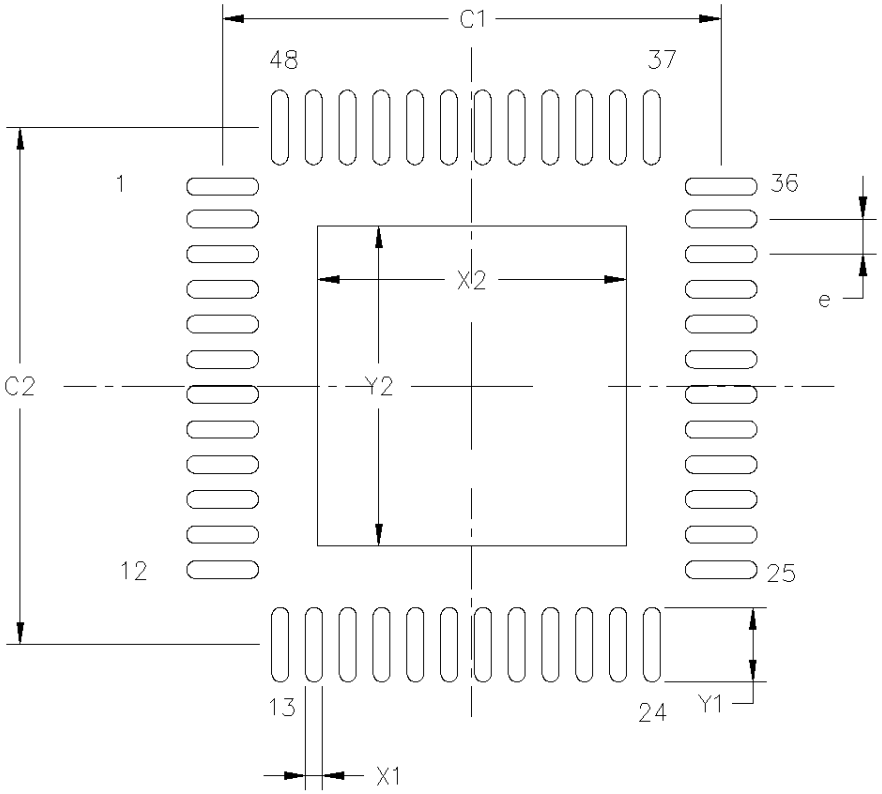


Figure 9.4. 48L 6 x 6 mm QFN Land Pattern

Table 9.4. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
X1	0.20
X2	3.60
Y1	0.85
Y2	3.60
e	0.40 BSC

Dimension	mm

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 3x3 array of 0.90 mm square openings on 1.15mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.5 Si53204 Package

The figure below illustrates the package details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

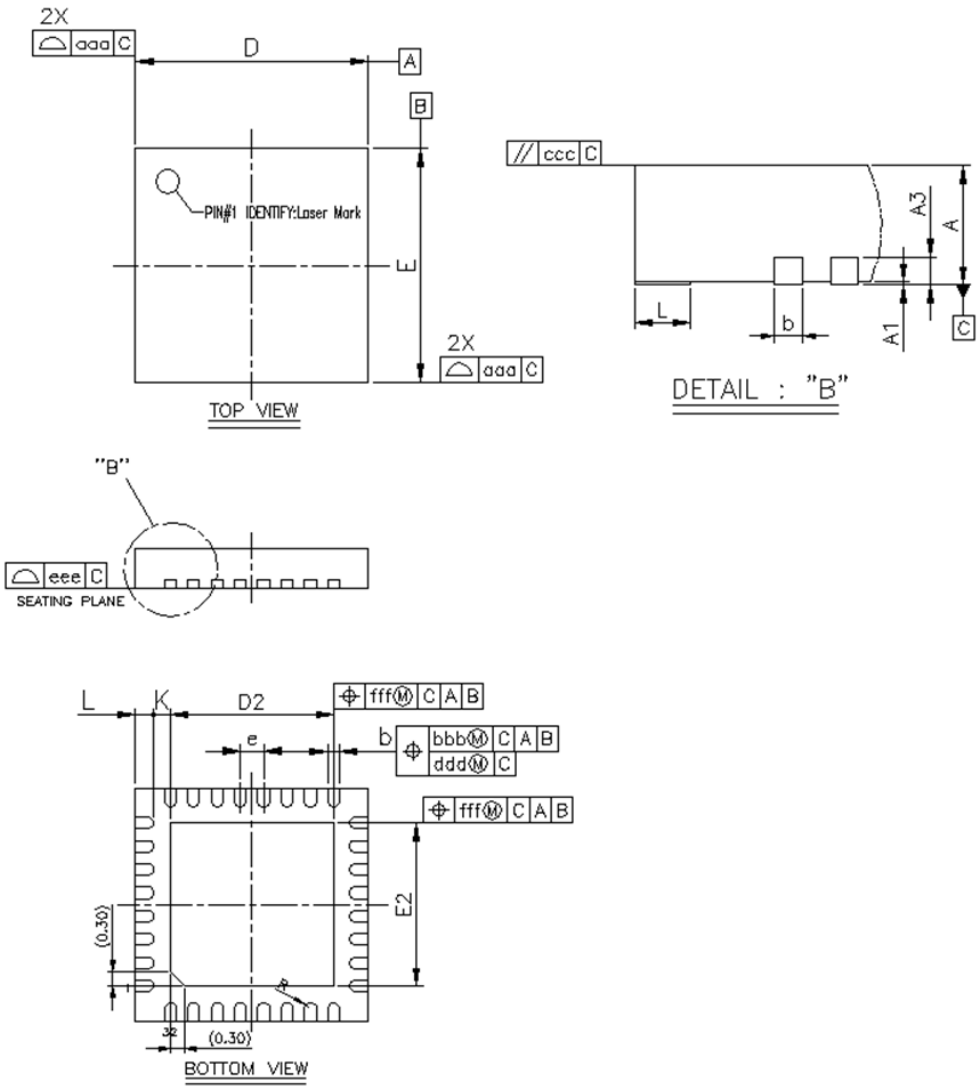


Figure 9.5. 32L 5 x 5 mm QFN Package Diagram

Table 9.5. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
K	0.20	—	—
L	0.30	0.40	0.50
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per JEDEC/IPC J-STD-020 specification for Small Body Components.

9.6 Si53204 Land Pattern

The figure below illustrates the land pattern details for the Si53204 in a 32-Lead, 5 x 5 mm QFN package. The table lists the values for the dimensions shown in the illustration.

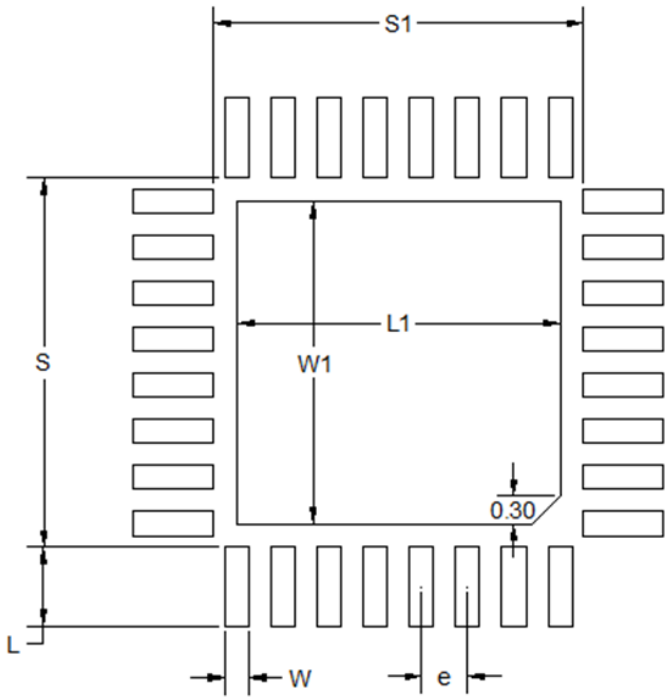


Figure 9.6. 32L 5 x 5 mm QFN Land Pattern

Table 9.6. PCB Land Pattern Dimensions

Dimension	mm
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Dimension	mm

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3x3 array of 0.85 mm square openings on 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.7 Si53212 Top Markings

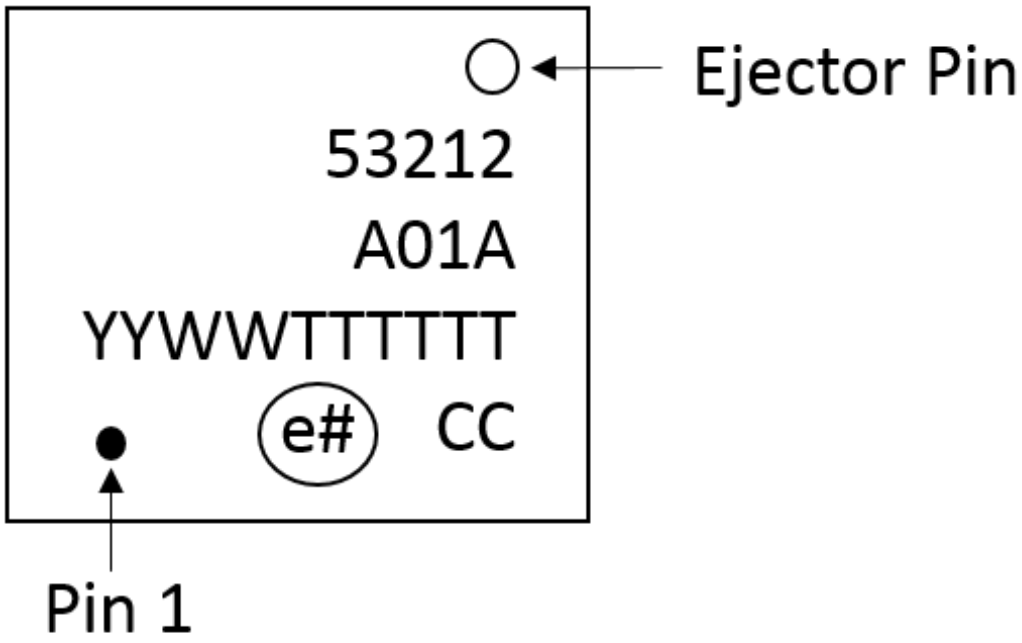


Figure 9.7. Si53212 Top Marking

Table 9.7. Si53212 Top Marking Explanation

Line	Characters	Description
1	53212	Device part number
2	A01A	Device part number
3	YYWWTTTTTT	YY = Assembly year WW = Work week TTTTTT = Manufacturing trace code

4	e# CC	e# = Lead-finish symbol. # is a number
		CC = Country of origin (ISO abbreviation)

9.8 Si53208 Top Markings

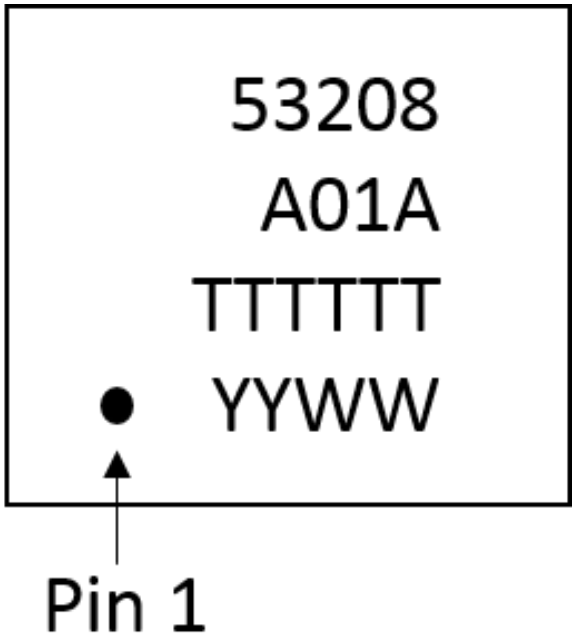


Figure 9.8. Si53208 Top Marking

Table 9.8. Si53208 Top Marking Explanation

Line	Characters	Description
1	53208	Device part number
2	A01A	Device part number
3	TTTTTT	Manufacturing trace code
4	YYWW	YY = Assembly year WW = Work week

9.9 Si53204 Top Markings

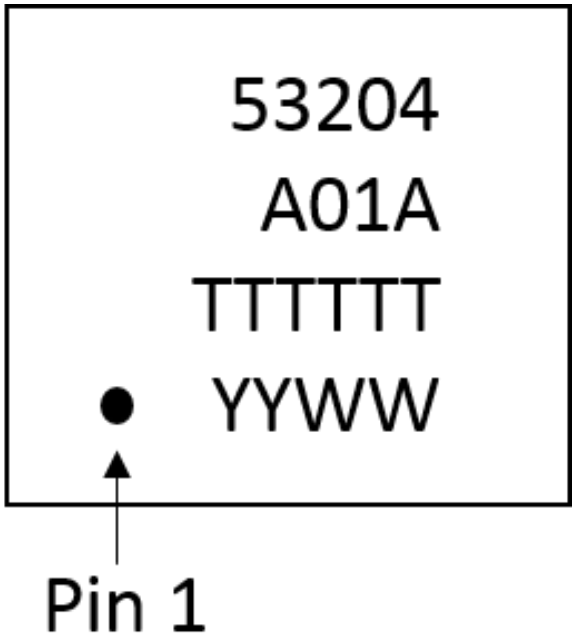


Figure 9.9. Si53204 Top Marking

Table 9.9. Si53204 Top Marking Explanation

Line	Characters	Description
1	53204	Device part number
2	A01A	Device part number
3	TTTTTT	Manufacturing trace code
4	YYWW	YY = Assembly year WW = Work week

10. Revision History

Revision 0.7

March, 2018

- Initial release.

ClockBuilder Pro

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