Si5332 車載用データシート

AEC-Q100 認定、6/8 出力、任意周波数クロック・ジェネレータ

Silicon Labs 独自の柔軟な周波数合成テクノロジー、MultiSynth™ に基づいた車載用 Si5332 は、優れたジッター性能 (190 fs rms) を実現しながら、任意の組み合わせの出力周波数を生成します。デバイスの非常に柔軟なアーキテクチャにより、0 ppm の周波数合成エラーを実現しながら、1 つのデバイスで最大 8 個の差動クロック出力の幅広い整数および非整数関係周波数を生成することができます。デバイスは、独立した電圧にそれぞれ接続できる複数の出力バンクを提供するため、供給電圧が混在するアプリケーションに使用できます。さらに、各クロック出力の信号フォーマットはユーザによる構成が可能です。周波数、フォーマット、供給電圧の柔軟性を備えた Si5332 を使用することで、複数のクロック IC と発振器を 1 つのデバイスに置き換えることができます。

Si5332 は、ClockBuilder Pro™ ソフトウェアを使用して素早く簡単に構成できます。ClockBuilder Pro は、固有の構成ごとにカスタム部品番号を割り当てます。カスタム部品番号を使って注文されたデバイスは、出荷時に無料で工場でプログラムされるため、各アプリケーションに応じてクロックを簡単にカスタマイズできます。Si5332 の I^2C インターフェイスを使用すれば、電源投入時にデバイスをユーザー構成したり、ClockBuilder Pro フィールド・プログラマを使用した新しい設定で内部構成 NVM をプログラムできます。

アプリケーション：

- インフォテインメント
- ADAS ECU
- レーダー・センサー
- LiDar センサー

主な機能

- 任意周波数 6/8 出力、プログラム可能なクロック・ジェネレータ
- AEC-Q100 認定
- AEC-Q006 認定
- 車載グレード 2：-40 ～ +105 °C
- 出力クロックとユーザ構成可能なハードウェア入力ピンの異なる組み合わせをサポートする 3 種類のパッケージ・サイズ
  - 32 ピン QFN、最大 6 出力
  - 40 ピン QFN、最大 8 出力
- MultiSynth テクノロジーにより、最大 250 MHz までの出力の任意の周波数合成が可能
- 高度な構成が可能な出力パス、クロスポイント・マルチプレクサを搭載
  - 最大 3 つの独立した非整数合成出力パス
  - 最大 5 つの独立した整数分周器
- 入力周波数帯域：
  - 外部水晶：16 ～ 50 MHz
  - 差動クロック：10 ～ 250 MHz
  - LVCMOS クロック：10 ～ 170 MHz
- 出力周波数帯域：
  - 差動：5 ～ 333.33 MHz
  - LVCMOS：5 ～ 170 MHz
- PCIe Gen1/2/3/4/5 準拠
- 出力毎のユーザ構成可能なクロック出力信号フォーマット：LVDS、LVPECL、HCSL、LVCMOS
- マルチ・プロファイル構成をサポート
- ダウンおよびセンター・スプレッド・スペクトラム
- RoHS-6 準拠
- Si5332-AM1/2/3 ファミリ・リファレンス・マニュアル

Table of Contents

1. Features List . . . 4

2. Ordering Guide . . . 5

3. Functional Description . . . 6

3.1 Functional Block Diagrams . . . 7

3.2 Modes of Operation . . . 8

3.2.1 Initialization . . . 8

3.3 Frequency Configuration . . . 8

3.4 Inputs . . . 9

3.4.1 External Reference Input (XA/XB) . . . 9

3.4.2 Input Clocks . . . 9

3.4.3 Input Selection . . . 9

3.5 Outputs . . . 10

3.5.1 Output Signal Format . . . 10

3.5.2 Differential Output Terminations . . . 11

3.5.3 LVCMOS Output Terminations . . . 15

3.5.4 LVCMOS Output Signal Swing . . . 15

3.5.5 LVCMOS Output Polarity . . . 15

3.5.6 Output Enable/Disable . . . 15

3.5.7 Differential Output Configurable Skew Settings . . . 15

3.5.8 Synchronous Output Disable Feature . . . 15

3.6 Spread Spectrum . . . 16

3.7 Universal Hardware Pins . . . 16

3.8 Custom Factory Pre-programmed Parts . . . 18

3.9 I^2C Serial Interface . . . 18

3.10 In-Circuit Programming . . . 18

3.11 Minimizing Power Consumption . . . 18

4. Register Map . . . 19

5. Electrical Specifications . . . 20

6. Pin Descriptions . . . 33

6.1 Pin Descriptions (40-QFN) . . . 33

6.2 Pin Descriptions (32-QFN) . . . 38

7. Package Outline . . . 42

7.1 Si5332 6x6mm 40-QFN Package Diagram . . . 42

7.2 Si5332 5x5mm 32-QFN Package Diagram . . . 44

8. PCB Land Pattern . . . 46

8.1 6x6mm 40-QFN Land Pattern . . . 46

8.2 5x5mm 32-QFN Land Pattern . . . 48

9. Top Marking 50

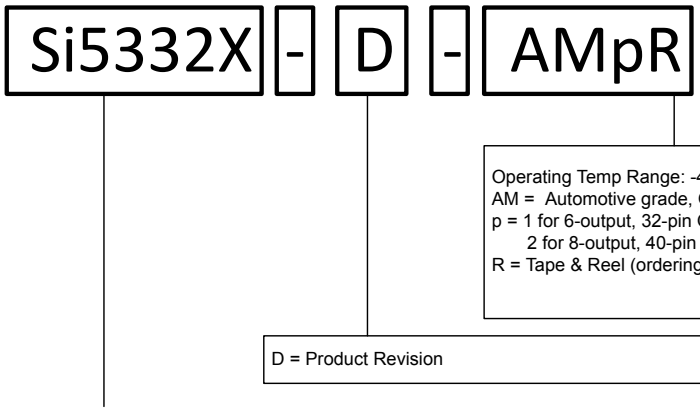
10. Document Change List 51

第 1 章 機能リスト

- 任意周波数 6/8 出力、プログラム可能なクロック・ジェネレータ
- 出力クロックとユーザ構成可能なハードウェア入力ピンの異なる組み合わせをサポートする 3 種類のパッケージ・サイズ
  - 32 ピン QFN、最大 6 出力
  - 40 ピン QFN、最大 8 出力
- MultiSynth™ テクノロジーにより、最大 250 MHz までの出力の任意の周波数合成が可能
- 最大 333.33 MHz の整数出力周波数
- 高度な構成が可能な出力パス、クロスポイント・マルチプレクサを搭載
  - 2 つの独立した非整数合成出力パス
  - 最大 5 つの独立した整数分周器
- 入力周波数帯域：
  - 外部水晶：16 ～ 50 MHz
  - 差動クロック：10 ～ 250 MHz
  - LVCMOS クロック：10 ～ 170 MHz
- 出力周波数帯域：
  - 差動：5 ～ 333.33 MHz
  - LVCMOS：5 ～ 170 MHz
- 出力毎のユーザ構成可能なクロック出力信号フォーマット：LVDS、LVPECL、HCSL、LVCMOS
- 190 fs RMS 位相ジッタ
- PCIe Gen1/2/3/4/5、共通クロック、SRIS 準拠
- 1.8 V、2.5 V、3.3 V コア VDD
- 調整可能な出力間遅延
- マルチ・プロファイル構成をサポート：
  - 同じカスタム部品番号で最大 16 の入力/出力構成を保存
- グリッチのない独立したオンザフライ出力周波数変更
- 非常に低い消費電力
- 各出力バンクの独立した出力電源ピン：
  - 1.8 V、2.5 V、または 3.3 V 差動
  - 1.5 V、1.8 V、2.5 V、3.3 V LVCMOS
- プログラム可能なスプレッド・スペクトラム
  - ダウンおよびセンター・スプレッド（30 ～ 33 kHz で -0.1% ～ 2.5%、0.01% ステップ）
- 電源フィルタリング内蔵
- シリアル・インターフェイス：I^2C
- ClockBuilder Pro ソフトウェア・ユーティリティにより、デバイスの構成とカスタム部品番号の割り合てを簡素化
- AEC-Q100 認定
- AEC-Q006 認定
- 車載グレード 2 温度範囲：-40 ～ +105 °C
- RoHS-6 準拠

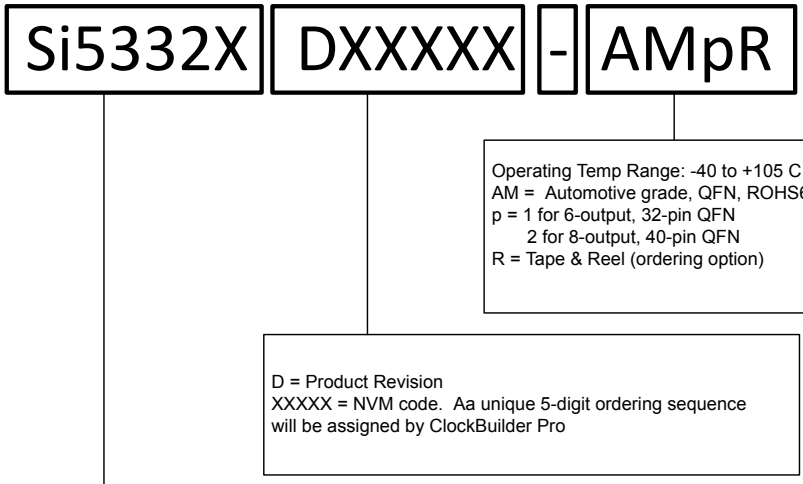
2. Ordering Guide

In-system programmable devices



Ordering Part Number	Frequency Synthesis Mode	Input Type	Output Clock Frequency Range	Operating Temperature Range
Si5332A	Integer and Fractional mode	External crystal or Clock	5MHz - 333.33MHz	-40 to +105C
Si5332B	Integer and Fractional mode		5MHz - 200MHz	
Si5332C	Integer mode only		5MHz - 333.33MHz	
Si5332D	Integer mode only		5MHz - 200MHz	

Pre-programmed devices using a ClockBuilder Pro configuration file



Ordering Part Number	Frequency Synthesis Mode	Input Type	Output Clock Frequency Range	Operating Temperature Range
Si5332A	Integer and Fractional mode	External crystal or Clock	5MHz - 333.33MHz	-40 to +105C
Si5332B	Integer and Fractional mode		5MHz - 200MHz	
Si5332C	Integer mode only		5MHz - 333.33MHz	
Si5332D	Integer mode only		5MHz - 200MHz	

Figure 2.1. Orderable Part Number Guide

3. Functional Description

The Si5332 is an automotive grade 2 high-performance, low-jitter clock generator capable of synthesizing up to eight user-programmable clock frequencies up to 333.33 MHz. The device supports free-run operation using an external crystal or it can lock to an external clock signal. The output drivers support up to eight differential clocks or sixteen LVCMOS clocks, or a combination of both. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, and LVCMOS. VDDO pins are provided for versatility, which can be set to 3.3 V, 2.5 V, 1.8 V or 1.5 V (CMOS only) to power the multi-format output drivers. The core voltage supply (VDD) accepts 3.3 V, 2.5 V, or 1.8 V and is independent from the output supplies (VDDOxs). Using its two-stage synthesis architecture and patented high-resolution low-jitter MultiSynth technology, the Si5332 can generate an entire clock tree from a single device.

The Si5332 combines a wideband PLL with next generation MultiSynth technology to offer the industry's highest output count high performance programmable clock generator with attainable jitter performance below 200 fs RMS. The PLL locks to either an external 16-50 MHz crystal or to an external clock (CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#) for generating synchronous clocks. In free-run mode, the oscillator frequency is multiplied by the PLL and then divided down either by an integer divider or MultiSynth for fractional synthesis.

The Si5332 features user-defined universal hardware pins which can be configured in the ClockBuilder Pro software utility. Universal hardware pins can be used for input functions such as OE, spread spectrum enable, input clock selection, output frequency selection, or I^2C address select, or RESET. Users can also assign a universal hardware pin as an LOS output.

The device provides the option of storing a user-defined clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up. To enable in-system programming, a power up mode is available through OTP, which powers up the chip in an OTP defined default mode but with no outputs enabled. This allows a host processor to first write a user defined subset of the registers and then restart the power-up sequence to activate the newly programmed configuration without re-downloading the OTP.

3.1 Functional Block Diagrams

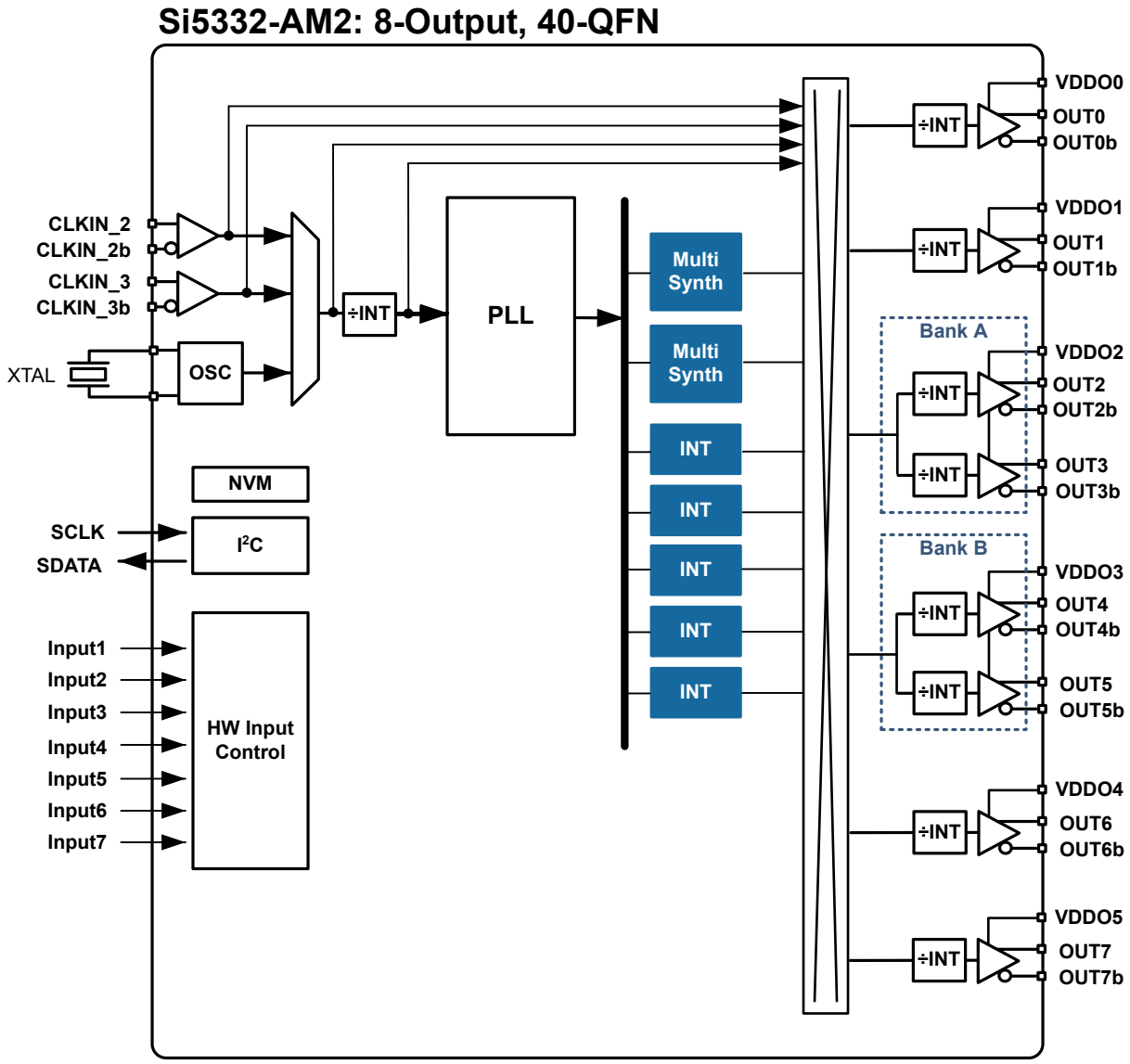


Figure 3.1. Block Diagram for 8-Output Si5332 in 40-QFN

The Si5332-AM2 40-QFN features:

- Up to eight differential clock outputs, with six VDDO pins.
- Seven user-configurable HW input pins, defined using ClockBuilder Pro.

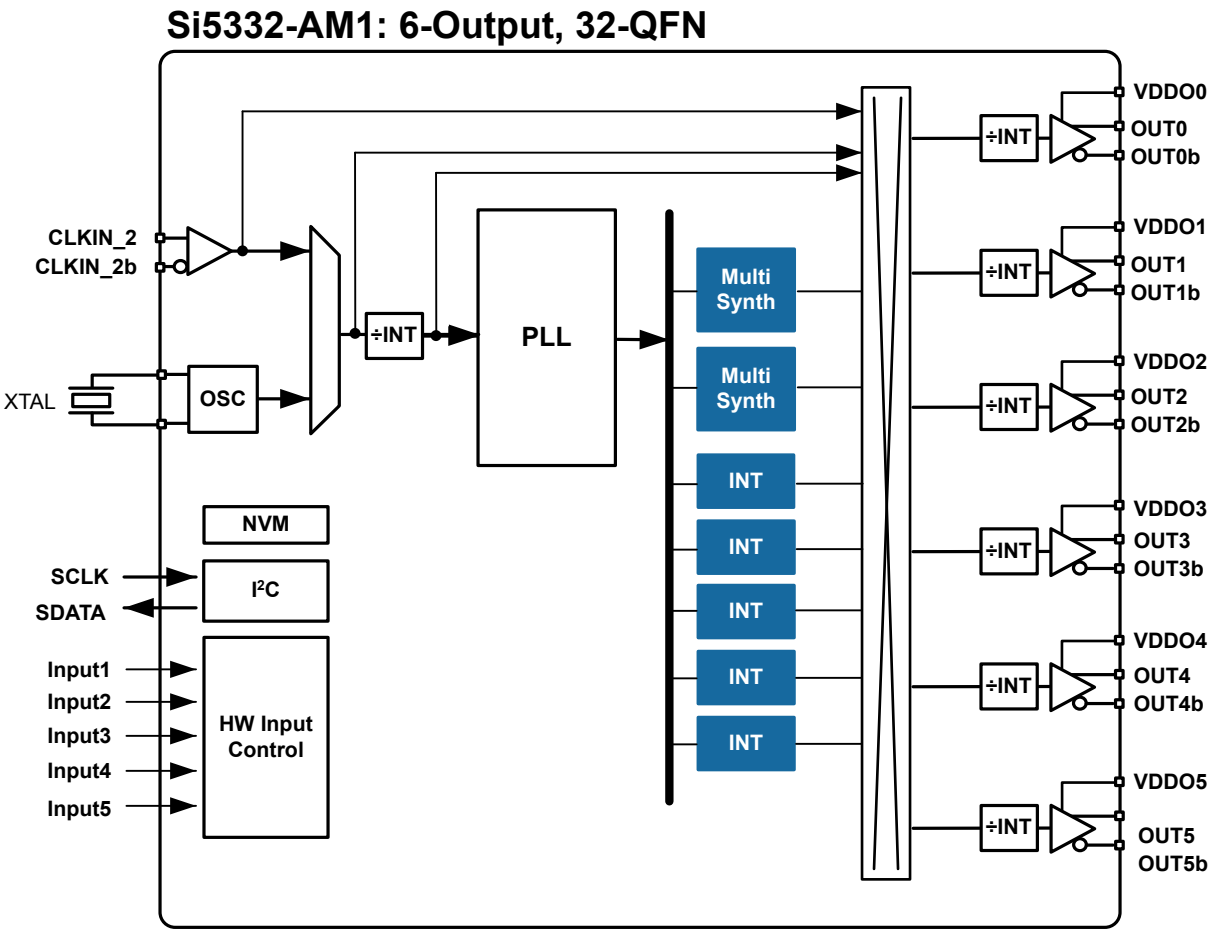


Figure 3.2. Block Diagram for 6-Output Si5332 in 32-QFN

The Si5332-AM1 32-QFN features:

- Up to six differential clock outputs with individual VDDO.
- Five user-configurable HW input pins, defined using ClockBuilder Pro.

3.2 Modes of Operation

The Si5332 supports both free-run and synchronous modes of operation. The default mode selection is set in ClockBuilder Pro. Alternatively, two universal hardware input pins can be defined as CLKIN_SEL[1:0] to select between a crystal or clock input. There is also the option to select the input source via the serial interface by writing to the input select register.

3.2.1 Initialization

When power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. The clock outputs will be squelched until the device initialization is done.

3.3 Frequency Configuration

The phase-locked loop is fully integrated and does not require external loop filter components. Its function is to phase lock to the selected input and provide a common synchronous reference to the high-performance MultiSynth fractional or integer dividers.

A cross point mux connects any of the MultiSynth divided frequencies or INT divided frequencies to individual output drivers or banks of output drivers. Additional output integer dividers provide further frequency division by an even integer from 1 to 63. The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (Mn/Md), the MultiSynth fractional dividers (Nn/Nd), and the output integer dividers (R). Silicon Labs' Clockbuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan

3.4 Inputs

The Si5332 requires an external 16–50 MHz crystal at its XIN/XOUT pins to operate in free-run mode, or an external input clock (CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#) for synchronous operation. An external crystal is not required in synchronous mode.

3.4.1 External Reference Input (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) on Si5332A/B/C/D to produce a low jitter reference for the PLL when operating in the free-run mode. The Si5332-AM1/2/3 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to Table 5.4 External Crystal Input Specification on page 23 for crystal specifications.

For free-running operation, the internal oscillator can operate from a low-frequency fundamental mode crystal (XTAL) with a resonant frequency of 16 to 50 MHz. A crystal can easily be connected to pins XA and XB without external components, as shown in the figure below. Internal loading capacitance (CL) values from 2.5 pf to 21.5 pf can be selected via register settings. Alternatively, an external CL can be used along with the internal CL.

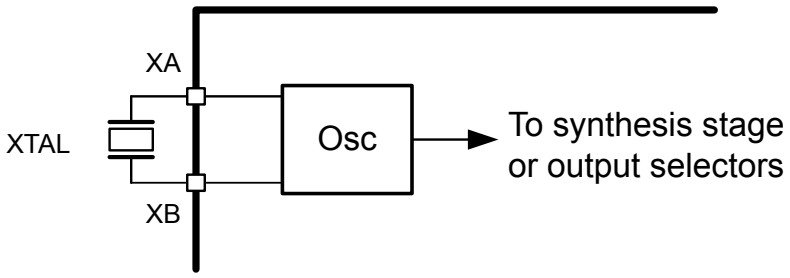


Figure 3.3. External Reference Input (XA/XB)

3.4.2 Input Clocks

An input clock is available to synchronize the PLL when operating in synchronous mode. This input can be configured as LVPECL, LVDS or HCSL differential, or LVCMOS. The recommended input termination schemes are shown in the Si5332-AM1/2/3 Family Reference Manual. Differential signals must be AC coupled. Unused inputs can be disabled by register configuration.

3.4.3 Input Selection

The active clock input is selected by register control, or by defining two universal input pins as CLKIN_SEL[1:0] in ClockBuilder Pro. A register bit determines input selection as pin or register selectable. If there is no clock signal on the selected input at power-up, the device will not generate output clocks.

In a typical application, the Si5332 reference input is configured immediately after power-up and initialization. If the device is switched to another input more than ±1000 ppm offset from the initial input, the device must be recalibrated manually to the new frequency, temporarily turning off the clock outputs. After the VCO is recalibrated, the device will resume producing clock outputs. If the selected inputs are within ±1000 ppm, any phase error difference will propagate through the device at a rate determined by the PLL bandwidth. Hitless switching and phase build-out are not supported by the Si5332.

3.5 Outputs

The Si5332 supports up to 12 differential output drivers. Each output can be independently configured as a differential pair or as dual LVCMOS outputs. The 8-output and 12-output devices feature banks of outputs, with each bank sharing a common VDDO.

Table 3.1. Clock Outputs

Device/Package	Maximum Outputs
Si5332-AM1 (32-QFN)	6 Differential, 12 LVCMOS
Si5332-AM2 (40-QFN)	8 Differential, 16 LVCMOS

The output stage is different for each of the three versions of Si5332.

- The 6-output device features individual VDDO pins for each clock output. Each clock output can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point mux.
- The 8-output device includes four clock outputs with dedicated VDDO pins, each of which can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point mux. The remaining four clock outputs are divided into Bank A and Bank B. Each Bank of outputs can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point mux. The outputs within each of the two Banks share a common VDDO pin.

Utilizing the reference clock enables a fan-out buffer function from an input clock source to any bank of outputs.

Individual integer output dividers (R) allow the generation of additional synchronous frequencies. These integer dividers are configurable as divide by 1 (default) through 63.

3.5.1 Output Signal Format

The differential output swing and common mode voltage are compatible with a wide variety of signal formats including HCSL, LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS drivers, enabling the device to support both differential and single-ended clock outputs. Output formats can be defined in ClockBuilder Pro or via the serial interface.

3.5.2 Differential Output Terminations

LVDS Driver Termination

For a general LVDS interface, the recommended value for the differential termination impedance (Z_T) is between 90 Ω and 132 Ω. The actual value should be selected to match the differential impedance (Z0) of the transmission line. A typical point-to-point LVDS design uses a 100 Ω parallel resistor at the receiver and a 100 Ω differential transmission-line environment. To avoid any transmission-line reflection issues, surface mount the components and place them as close to the receiver as possible. The standard LVDS termination schematic as shown in Figure 3.4 Standard LVDS Termination on page 11 can be used with either type of output structure. Figure 3.5 Optional LVDS Termination on page 11, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 0.01 to 0.1 µF. If using a non-standard termination, please contact Silicon Labs to confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

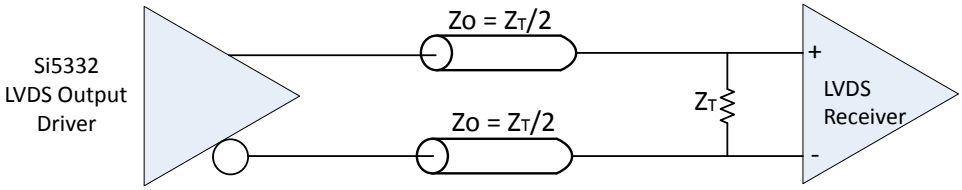


Figure 3.4. Standard LVDS Termination

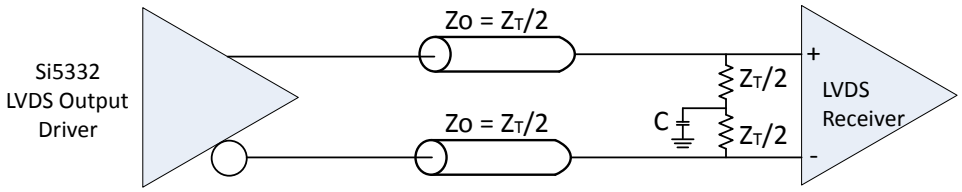


Figure 3.5. Optional LVDS Termination

Termination for 3.3 V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Use matched impedance techniques to maximize operating frequency and minimize signal distortion. Figure 3.6 3.3 V LVPECL Output Termination, Option 1 on page 12 and Figure 3.7 3.3 V LVPECL Output Termination, Option 2 on page 12 show two different layouts. Other suitable clock layouts may exist, but it is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

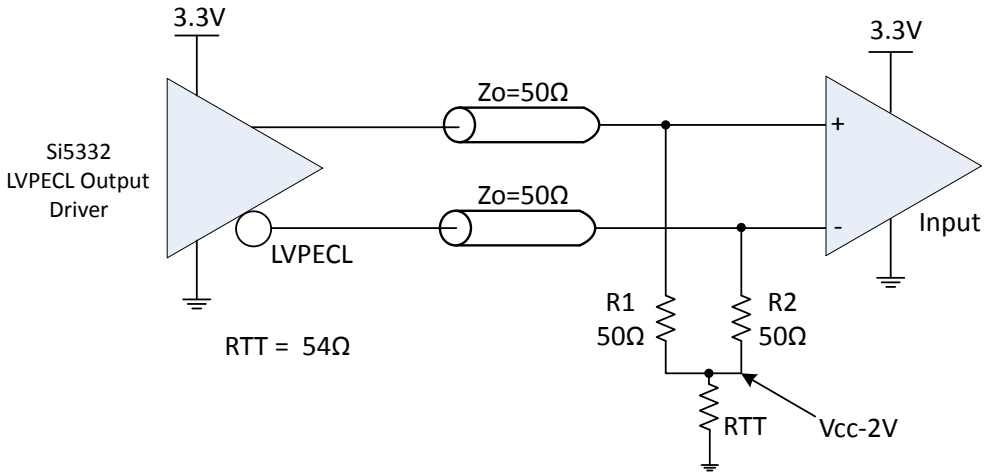


Figure 3.6. 3.3 V LVPECL Output Termination, Option 1

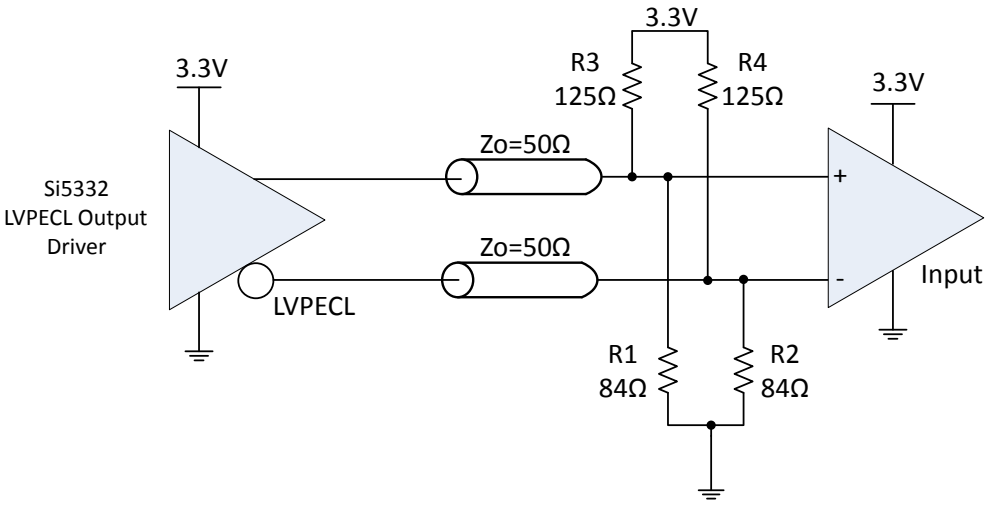


Figure 3.7. 3.3 V LVPECL Output Termination, Option 2

Termination for 2.5 V LVPECL Outputs

Figure 3.8 2.5 V LVPECL Termination Example, Option 1 on page 13 and Figure 3.9 2.5 V LVPECL Termination Example, Option 2 on page 13 show examples of termination for the 2.5 V LVPECL driver option. These terminations are equivalent to terminating 50 Ω to VDDO – 2 V. For VDDO = 2.5 V, the VDDO – 2 V is very close to ground level. The R3 in Figure 3.9 2.5 V LVPECL Termination Example, Option 2 on page 13 can be optionally eliminated using the termination shown in Figure 3.8 2.5 V LVPECL Termination Example, Option 1 on page 13.

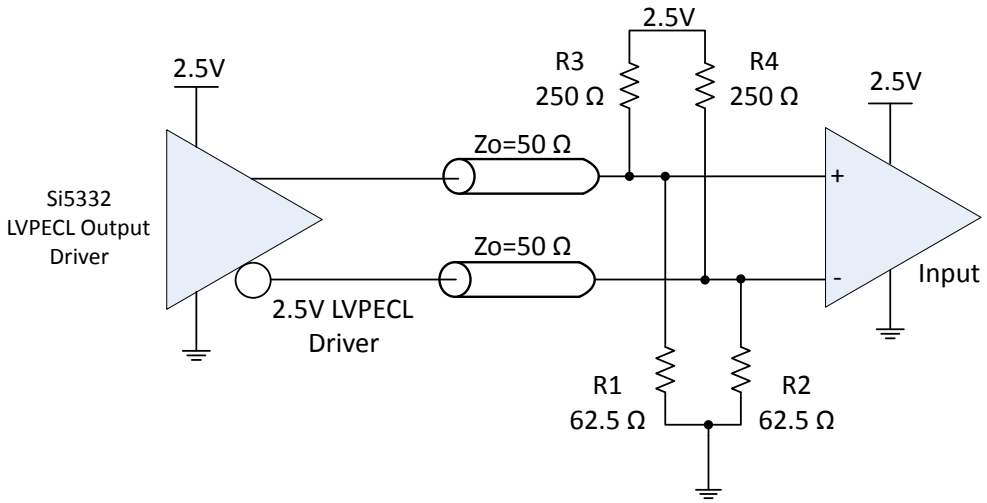


Figure 3.8. 2.5 V LVPECL Termination Example, Option 1

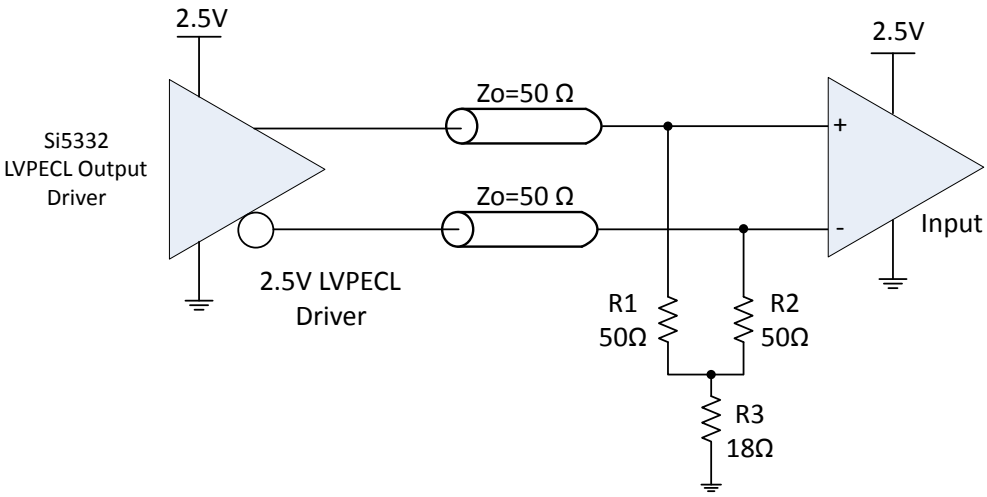


Figure 3.9. 2.5 V LVPECL Termination Example, Option 2

Termination for HCSL Outputs

The Si5332 HCSL driver option integrates termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100 Ω and 85 Ω transmission line options. This configuration option may be specified using ClockBuilder Pro or via the device I^2C interface.

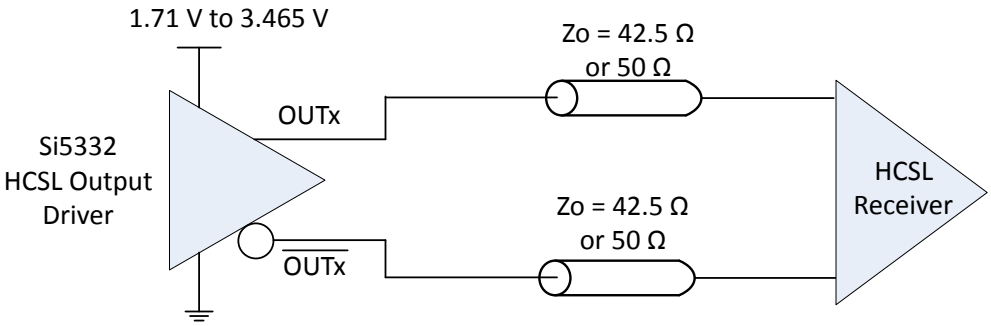


Figure 3.10. HCSL Internal Termination Mode

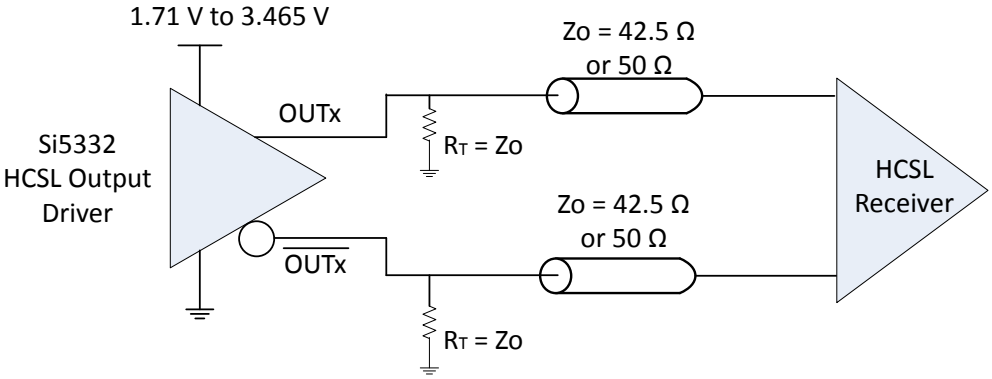


Figure 3.11. HCSL External Termination Mode

3.5.3 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.

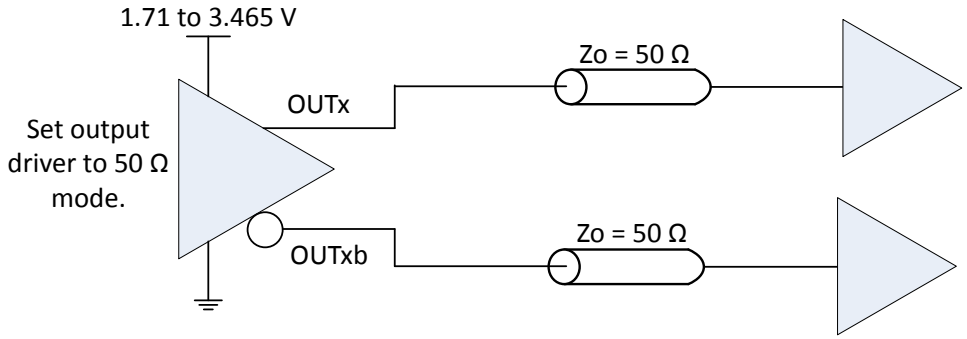


Figure 3.12. LVCMOS Output Termination Example, Option 1

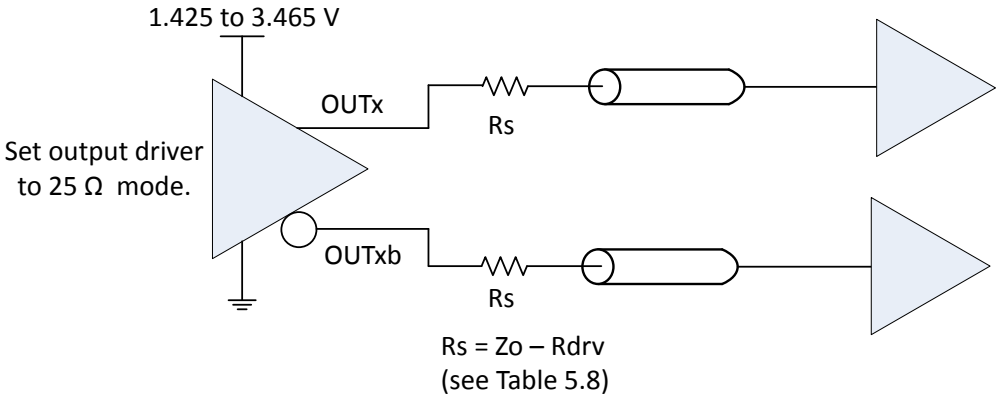


Figure 3.13. LVCMOS Output Termination Example, Option 2

3.5.4 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

3.5.5 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTxb pin is generated in phase with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

3.5.6 Output Enable/Disable

The universal hardware input pins can be programmed to operate as output enable (OEb), controlling one or more outputs. Pin assignment is done using ClockBuilder Pro. An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high all designated outputs will be disabled. When held low, the designated outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

3.5.7 Differential Output Configurable Skew Settings

Skew on the differential outputs can be independently configured. The skew is adjustable in 35 ps steps across a range of 245 ps.

3.5.8 Synchronous Output Disable Feature

Output clocks are always enabled and disabled synchronously. The output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output.

3.6 Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5332 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The Si5332 implements spread spectrum using its patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude. Spread spectrum can be enabled through I^2C, or by configuring one of the universal hardware input pins using ClockBuilder Pro.

The Si5332 features both center and down spread spectrum modulation capability, from 0.1% to 2.5%. Each MultiSynth is capable of generating an independent spread spectrum clock. The feature is enabled using a user-defined universal hardware input pin or via the device I^2C interface. Spread spectrum can only be applied to output clock derived from a MultiSynth fractional divider, up to 250 MHz. Since the spread spectrum clock generation is performed in the MultiSynth fractional dividers, the spread spectrum waveform is highly consistent across process, voltage and temperature. The Si5332 features two independent MultiSynth dividers, enabling the device to provide two independent spread profiles simultaneously to the clock output banks.

Spread spectrum is commonly used for 100 MHz PCI Express clock outputs. To comply with the spread spectrum specifications for PCI Express, set the spreading frequency to a maximum of 33 kHz and –0.5% down spread. A universal hardware input pin can be configured to toggle spread spectrum on/off.

3.7 Universal Hardware Pins

Universal hardware pins are user-configurable control pins that can have one or more of the functions listed below assigned to them using ClockBuilder Pro.

Universal hardware pins can be utilized for the following functions:

Table 3.2. Universal Hardware Pins

Description	Function
SSEN_EN0	Spread spectrum enable on MultiSynth0 (N0).
SSEN_EN1	Spread spectrum enable on MultiSynth0 (N1).
FS_INTx	Used to switch an integer output divider frequency from frequency A to frequency B.
FS_MSx	Used to switch a MultiSynth output divider output from frequency and/or change spread spectrum profile.
OE	Output enable for one or more outputs.
I^2C address select	Sets the LSB of the I^2C address to either 0 or 1.
CLKIN_SEL[1:0]	Selects between crystal or clock inputs.
LOS	Detects if reference input frequency drops below 10 MHz.
Multi-Profile	Consolidates multiple configuration files into a single device.

Spread Spectrum Enable Pins (SSEN[1:0])

SSEN_EN[1:0] pins are active pins that enable/disable spread spectrum on all outputs that correspond to MutliSynth0 or MultiSynth1, respectively. The change in frequency or spread spectrum will be instantaneous and may not be glitch free.

Table 3.3. SSEN_EN Pin Selection Table

SSEN_ENx	
0	Spread Spectrum disabled on MultiSynthx
1	Spread Spectrum enabled on MultiSynthx

Output Frequency Select Pins

There are five integer dividers, one corresponding to each of the five output banks. Using ClockBuilder Pro, a universal hardware input pin can be assigned for each integer divider, providing capability to select between two different pre-programmed divide values. Divider values of every integer from 8 to 255 are available in ClockBuilder Pro for each integer divider.

Table 3.4. FS_INT Pin Selection Table

FS_INTX	Output Frequency from INTx
0	Frequency A, as defined in ClockBuilder Pro
1	Frequency B, as defined in ClockBuilder Pro

Output Enable

A universal hardware input pin can be defined to control output enable of a differential output, a bank of differential outputs, or as a global output enable pin controlling all outputs. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 µs for the output to have a clean clock.

Output enabled/disabled for LVCMOS are done in pairs. Each differential buffer True and Compliment output can generate an LVCMOS clock and the OE pin associated with the True and Compliment output buffer will control the respective LVCMOS pair.

For example: If DIFF0 is configured to be SE1 and DIFF0# is configured to be SE2 and OE1 is the associated OE pin, de-asserting the OE1 pin will disable both SE1 and SE2 outputs. The disable and enable of the outputs to a known state is glitch free.

I^2C Address Pin

This pin sets the LSB of the 7-bit I^2C address. For example, if the I^2C address is 6Ah, setting this pin high will set the I^2C address to 6Bh.

CLKIN_SEL[0:1] Pins

These pins are used to set the input source clock between the input clock channels (Crystal, CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#). Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

Multi-Profile

Si5332 has the ability to store multiple unique configurations in the same custom part number by enabling multi-profile support in ClockBuilder Pro after selecting the desired Si5332 device. The ClockBuilder Pro wizard guides users to enter the input/output/feature set needed for each individual profile configuration, then compiles them together and assigns the necessary number of universal hardware pins based on the number of profiles entered. The actual number of profiles supported in a particular design is limited by overall design complexity and NVM size. ClockBuilder Pro automatically determines the NVM size required for your multi-profile design and will warn if the maximum limit is exceeded.

LOS (Loss of Signal)

LOS is a feature that can be implemented during configuration file development using ClockBuilder Pro on a customized device. LOS is not available on the generic volatile I^2C programmable devices. The LOS indicator is used to check for the presence of an input reference source(crystal or clock). Users can choose either active high or active low logic when the LOS pin is defined. LOS will assert when the reference source frequency drops below the minimum input frequency specifications noted in the Table 5.3 Clock Input Specifications on page 22.

For Active High:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin assumes a logic high (LOS = 1) state. When a reference source is present at the associated input clock pin, the LOS pin assumes a logic low (LOS = 0) state.

For Active Low:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin assumes a logic low (LOS = 0) state. When a reference source is present at the associated input clock pin, the LOS pin assumes a logic high (LOS = 1) state.

3.8 Custom Factory Pre-programmed Parts

Custom pre-programmed parts can be ordered corresponding to a specific configuration file generated using the ClockBuilder Pro software utility. Silicon Labs writes the configuration file into the device prior to shipping. Use the ClockBuilder Pro custom part number wizard (http://www.silabs.com/clockbuilderpro) to quickly and easily generate a custom part number for your ClockBuilder Pro configuration file. A factory pre-programmed part will generate clocks at power-up.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship within two weeks.

3.9 I²C Serial Interface

The Si5332 is compatible with rev6 of the I²C specification, including Standard, Fast, and Fast+ modes.

Configuration and operation of the Si5332 can be controlled by reading and writing registers using the I²C . Communication with a 1.8 V, 2.5 V, or 3.3 V host is supported consistent with SDA, SCLK pin usage as described in the device Pin Description tables. See the Si5332-AM1/2/3 Family Reference Manual for details.

3.10 In-Circuit Programming

The Si5332 is in-system configurable using the I²C interface by the following two methods:

- *In-ciruit configuration of device registers after power-up.* With this method, changes to volatile register memory can be done as required to produce the desired outputs. This does not alter internal NVM; therefore, register memory changes are lost at power-down. Refer to the Si5332-AM1/2/3 Family Reference Manual available on our web site for details.
- *In-circuit re-configuration of internal NVM.* Writing to internal NVM requires the use of the CBPro Field Programmer (CBPROG-DONGLE) and CBPro software. See UG286: ClockBuilderPro Field Programmer Kit User's Guide available on our web site for more information. (One important note: The Si5332 core VDDs [VDD_DIG, VDDA, and VDD_XTAL] must be powered by 3.3 V during in-circuit NVM programming.)
- VDD core voltages (VDD_DIG, VDDA, VDD_XTAL) must be 3.3 V for in-circuit programming. Using VDD core voltage lower than 3.3 V (i.e., 2.5 V or 1.8 V) will not support reliable in-circuit NVM programming.

3.11 Minimizing Power Consumption

The Si5332 clock generator products are designed to provide a high level of flexibility and programmability, while achieving very low jitter performance. To ensure the 125 °C maximum junction temperature limit (T_{JMAX}) is not exceeded, overall power consumption of the device must be limited to the maximum specifications noted in Table 5.2 DC Characteristics on page 21.

ClockBuilder Pro provides power consumption and T_J estimates to help with power estimation and budgeting as a configuration file is being developed. If the maximum power consumption limit is exceeded, ClockBuilder Pro will provide a warning to the user. Silicon Labs recommends the following guidelines:

To minimize power consumption:

- Use 1.8 V VDD and/or VDDO instead of 2.5 V or 3.3 V whenever possible.
- For differential clock outputs, use LVDS output drivers instead of LVPECL or HCSL.
- For HCSL clock outputs:
  - Select 100 Ω impedance driver instead of 85 Ω
  - Select external termination instead of internal termination
- For single-ended clock outputs
  - Use the lowest frequency option available for your design. Lower frequencies consumes lower output driver current.
  - Use the lowest capacitive loading available for your design. Lower capacitive loading consumes lower output driver current.
  - When two outputs of the same frequency are needed, select a dual-complementary CMOS output driver instead of two independent single-CMOS output drivers.

Silicon Labs always recommends that users develop a configuration file in ClockBuilder Pro and assign a customized part number. Users who elect to use the "blank" ordering option and program the device in-system must first check the desired configuration in ClockBuilder Pro to ensure the maximum power consumption limits are not exceeded. That is the only way to ensure the maximum power consumption limits are not exceeded, and therefore, meets a 125 °C maximum junction temperature.

4. Register Map

Refer to the Si5332-AM1/2/3 Family Reference Manual for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	25	105	°C
Junction Temperature	TJ_{MAX}		—	—	125	°C
Core Supply Voltage	V_{DDA}, V_{DD_DIG}, V_{DD_xtal}		1.71	—	3.46	V
Output Driver Supply Voltage	V_{DDO}		1.42[3]	—	3.46	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
2. All core voltages (VDD_DIG, VDDA, VDD_XTAL) must be connected to the same voltage.
3. LVCMOS outputs only.

Table 5.2. DC Characteristics

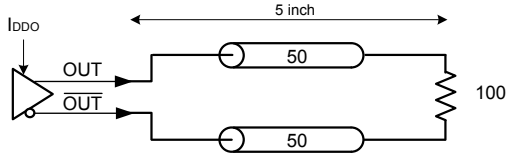
(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}			—	45	70	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[3] @ 156.25 MHz		—	33	35	mA
		HCSL Output[3] @ 100 MHz		—	20	22	mA
		LVDS Output[3] @ 156.25 MHz		—	11	13	mA
		3.3 V VDDO LVCMOS[4] output @ 170 MHz		—	16	19	mA
		2.5 V VDDO LVCMOS[4] output @ 170 MHz		—	9	11	mA
		1.8 VDDO LVCMOS[4] output @ 170 MHz		—	7.5	8.5	mA
Total Power Dissipation	P_d	40-pin	Note 1, 5		320	875	mW
		32-pin	Notes 2, 5	—	270	720	mW

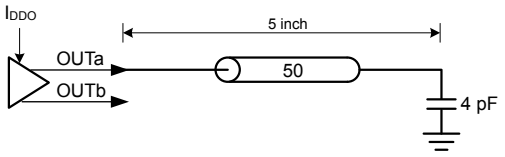
Notes:

1. Si5332 40-pin test configuration: V_{DDD} = V_{DDA} = V_{DD} = 1.8 V, 4 × 2.5 V LVDS outputs enabled @ 156.25 MHz, 2 × 1.8 V HCSL outputs enabled @ 100 MHz, 2x 3.3 V LVCMOS outputs enabled @ 25 MHz. . Excludes power in termination resistors.
2. Si5332 32-pin test configuration: V_{DDD} = V_{DDA} = V_{DDI} = 1.8 V, 2 × 2.5 V LVDS outputs enabled @ 156.25 MHz, 2 × 1.8 V HCSL outputs enabled @ 100 MHz. 2x 3.3 V LVCMOS outputs enabled @ 25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into a 100 Ω load.
4. LVCMOS outputs measured into a 5 inch 50 Ω PCB trace with 4 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. ClockBuilderPro includes a power consumption indicator. Users should always enter the desired configuration into ClockBuilder-Pro to ensure the maximum power dissipation limits are not exceeded.
6. If configurations exceed the Max Total Power Dissipation specifications, the maximum ambient temperature limit of 105 °C and maximum junction temperature limits of 125 °C are void.

Table 5.3. Clock Input Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC-coupled Differential Input Clock on CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#)						
Frequency	F_{IN}	Differential	10	—	250	MHz
Voltage Swing	V_{PP_DIFF}[3]	Differential AC-coupled < 333.33 MHz	0.5	—	1.8	V_{PP_diff}
Slew Rate	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		2	3.5	6	pF
Input Clock (AC-coupled LVCMOS Input Clock on CLKIN_2 or CLKIN_3)						
Frequency	F_{IN}		10	—	170	MHz
Input High Voltage	V_{IH}		0.8 × V_{DD}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.2 × V_{DD}	V
Slew Rate[1,2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		2	3.5	6	pF
Input Clock (AC-coupled Input Clock on CLKIN1)						
Frequency	F_{IN}		10	—	170	MHz
Voltage Swing				—	1	V_{PP}
Input Low Voltage	V_{IL}		—	—	0.2 x V_{DD}	V
Slew Rate[1, 2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		2	3.5	6	pF

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20}$ = ((0.8 - 0.2) * $V_{IN\_Vpp\_se}$) / SR.
3. V_{PP_DIFF} = 2 x $V_{PP\_SINGLE\text{-}ENDED}$

Table 5.4. External Crystal Input Specification

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{xtal}			16-50		MHz
Load Capacitance	C_L	16 - 30 MHz	6	12	20	pF
		31 - 50 MHz			10	pF
Shunt Capacitance	C_O	16 - 30 MHz	—	—	7	pF
		31 - 50 MHz	—	—	2	pF
ESR		16 - 30 MHz	—	—	50	Ω
		31 - 50 MHz	—	—	50	Ω
Max Crystal Drive Level	d_L		—	—	250	µW
Input Capacitance [1]	C_{IN}	Internal cap disabled	—	2.5	—	pF
		Internal cap enabled (per pad)[2]	5	—	43	pF
Input Voltage	V_{XIN}		-0.3	—	1.3	V

Notes:

1. Internal capacitance on the xtal input pads is programmable or can be disabled. Refer to section 3.4.1 External Reference Input (XA/XB) for more detailed information.
2. Refer to Si5332-AM1/2/3 Family Reference Manual for more information.

Table 5.5. Control Pins

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5332 Control Input Pins (Inputx)						
Input Voltage	V_{IL}		-0.1	—	0.3 × VDD[1]	V
	V_{IH}		0.7 × VDD[1]	—	1.1 × V_{DD}	V
Input Capacitance	C_{IN}		—	—	4	pF
Pull-up/down Resistance	R_{IN}		—	50	—	kΩ

Note:

1. V_{DD} indicates all core voltages V_{DD_DIG}, V_{DDA}, and V_{DD_XTAL} which are required to all be using same nominal voltage.

Table 5.6. Differential Clock Output Specifications

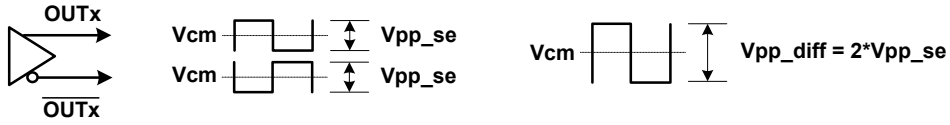
(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Frequency	f_{OUT}	Integer synthesis mode		5	—	333.33[20]	MHz
		Fractional synthesis mode		5	—	250	MHz
Duty Cycle	DC			48	—	52	%
Output-Output Skew	T_{SK}	Within the same bank		—	—	30	ps
		Across banks		—	—	80	ps
Output Voltage Swing	V_{SEPP}	LVPECL		0.6	0.75	0.85	V_{PP}
		LVDS	1.8/2.5/3.3 V	0.3	0.375	0.45	V_{PP}
		HCSL		0.7	0.8	0.9	V_{PP}
Common Mode Voltage	V_{CM}	LVPECL		—	VDDO-1.4	—	V
		LVDS	2.5/3.3 V	1.125	1.2	1.275	V
		LVDS	1.8 V	0.75	0.8	0.85	V
		HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 12,14,18		1	—	4.5	V/ns
HCSL Delta Tr	D_{tr}	Notes 14,17, 18		—	—	155	ps
HCSL Delta Tf	D_{tf}	Notes 14, 17, 18		—	—	155	ps
HCSL Vcross Abs	V_{xa}	Notes 11, 13, 14, 17		250	—	550	mV
HCSL Delta Vcross	D_{vcrs}	Notes 14,17		—	—	140	mV
HCSL Vovs	V_{ovs}	Notes 14,17		—	—	V_{HIGH}+300	mV
HCSL Vuds	V_{uds}	Notes 15, 17		—	—	V_{LOW}-300	mV
HCSL Vrng	V_{rng}	Notes 14,17		V_{HIGH}-200	—	V_{LOW}+200	mV
Rise and Fall Times (20% to 80%)	t_R/t_F	LVDS (fast mode)	3.3 V or 2.5 V	150	200	350	ps
		LVDS (slow mode)	3.3 V or 2.5 V	350	530	620	ps
			1.8 V	150	225	350	ps
Rise and Fall Times (20% to 80%)	t_R/t_F	LVPECL		150	—	320	ps
		HCSL		—	—	420	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units

Notes:

1. For best jitter performance, keep the midpoint differential input slew rate faster than 0.3 V/ns.
2. Not in PLL bypass mode.
3. For best jitter performance, keep the midpoint input single ended slew rate faster than 1 V/ns.
4. On chip termination resistance can be programmed on (100 Ω) or off (high impedance).
5. Not including R divider.
6. Input capacitance on crystal pins targets 23 pf each plus 1 pf external trace capacitance to provide 12 pf series equivalent crystal load capacitance.
7. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
8. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
9. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
10. Test configuration is Rs = 33.2 Ω, Rp = 49.9, 2 pF.
11. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700), Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg).
12. Measurement taken from Single Ended waveform.
13. Measurement taken from differential waveform VLow Math function.
14. Overshoot is defined as the absolute value of the maximum voltage.
15. Undershoot is defined as the absolute value of the minimum voltage.
16. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
17. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system.
18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.



19. LVDS swing levels for 50 Ω transmission lines.
20. Max frequency is 333 + 1/3 MHz.

Table 5.7. LVCMOS Clock Output Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.5 V ±5%, 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	fout	1.8-3.3 V CMOS	5	—	170	MHz
		1.5 V CMOS	5	—	133.33	MHz
Rise/Fall Time, 3.3 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace, CL = 4 pf	—	0.5	0.8	ns
Rise/Fall Time, 2.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.6	0.95	ns
Rise/Fall Time, 1.8 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.75	1.3	ns
Rise/Fall Time, 1.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.9	1.3	ns
CMOS Output Resistance (Single Strength)		3.3 V	—	46	—	Ω
		2.5 V	—	48	—	Ω
		1.8 V	—	53	—	Ω
		1.5 V	—	58	—	Ω
CMOS Output Resistance (Double Strength)		3.3 V	—	23	—	Ω
		2.5 V	—	24	—	Ω
		1.8 V	—	27	—	Ω
		1.5 V	—	29	—	Ω
CMOS Output Voltage	V_{OH}	–4 mA load	VDDO-0.3	—	—	V
	V_{OL}	4 mA load	—	—	0.3	V
Duty Cycle	DC	XO and PLL mode	45	—	55	%

Table 5.8. Performance Characteristics

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Initialization Time	$t_{initialization}$	Time for I^2C to become operational after core supply exceeds V_{DDmin}	—	—	15	ms
Clock Stabilization from Power-up	t_{STABLE}	Time for clock outputs to appear after POR	—	15	25	ms
Input to Output Propagation Delay	t_{PROP}	Buffer mode (PLL Bypass)	—	2.5	4.1	ns
Spread Spectrum PP Frequency Deviation	SSDEV	MultiSynth Output < 250 MHz	0.1	—	2.5	%
0.5% Spread Frequency Deviation	SSDEV	MultiSynth Output < 250 MHz	0.4	0.45	0.5	%
Spread Spectrum Modulation Rate		MultiSynth Output < 250 MHz	30	31.5	33	kHz

Notes:

1. Outputs at same frequencies and using the same driver format.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and 250 MHz.
3. Update rate via I^2C is also limited by the time it takes to perform a write operation.
4. Default value is ~31.5 kHz.

Table 5.9. Jitter Performance Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Typ	Max	Units
Jitter Generation, Locked to External 25 MHz Clock	J_{GEN}	INT Mode 12 kHz – 20 MHz [1,2]	210	280	fs RMS
		FRAC/DCO Mode 12 kHz – 20 MHz [3,5]	250		fs RMS
	J_{PER}	Derived from integrated phase noise at a BER of 1e-12	3.3		ps Pk-Pk
	J_{CC}		3.1		ps Pk
	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode. [2,3] Measured in the time domain. Performance is limited by the noise floor of the equipment.	12		ps Pk-Pk
	J_{CC}		11		ps Pk
Jitter Generation, Locked to External 25 MHz Crystal	J_{GEN}	INT Mode 12 kHz – 20 MHz [1,2]	190	240	fs RMS
		FRAC/DCO Mode 12 kHz – 20 MHz [3,5]	250		fs RMS
	J_{PER}	Derived from integrated phase noise at a BER of 1e-12	3.5		ps Pk-Pk
	J_{CC}		3.1		ps Pk
	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode. [2,3] Measured in the time domain. Performance is limited by the noise floor of the equipment.	12		ps Pk-Pk
	J_{CC}		11		ps Pk
Power Supply Noise Rejection[6]	PSNR	25 kHz	–100	—	dB
		50 kHz	–97	—	
		100 kHz	–72	—	
		500 kHz	–83	—	
		1 MHz	-91	—	

Notes:

1. INT jitter generation test conditions f_{OUT} = 156.25 MHz LVPECL.
2. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
3. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.
4. All jitter data in this table is based upon all output formats being differential. When LVCMOS outputs are used, there is the potential that the output jitter may increase due to the nature of LVCMOS outputs. If your configuration implements any LVCMOS output and any output is required to have jitter less than 3 ps RMS, contact Silicon Labs for support to validate your configuration and ensure the best jitter performance.
5. FRAC jitter generation test conditions f_{OUT} = 150 MHz LVPECL.
6. Measured at 156.25 MHz carrier frequency. Carrier power of -1.5 dBm. 100 mVpp sine wave noise added and noise spur amplitude measured.

Table 5.10. PCI-Express Clock Outputs (100 MHz HCSL)

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Test Condition	SSC On/Off	Typ	Max	Units
PCIe Gen 1.1	Includes PLL BW 1.5–22 MHz, Peaking = 3dB, Td = 10 ns, Ftrk=1.5 MHz with BER = 1E-12 [2]	Off	11	19	ps RMS
		On	22	30	ps RMS
PCIe Gen 2.1	Includes PLL BW 5MHz & 8–16 MHz, Jitter Peaking = 0.01-1 dB & 3 dB, Td=12ns, Low Band, F < 1.5 MHz	Off	0.02	0.026	ps RMS
		On	0.12	0.21	ps RMS
	Includes PLL BW 5 MHz & 8–16 MHz, Jitter Peaking = 0.01-1dB & 3dB, Td=12ns, High Band, 1.5 MHz < F < Nyquist[2]	Off	0.2	0.31	ps RMS
		On	0.8	1.3	ps RMS
PCIe Gen 3.0 Common Clock	Includes PLL BW 2–4 MHz & 5 MHz, Peaking = 0.01-2dB & 1dB, Td=12 ns, CDR = 10 MHz [2, 3]	Off	0.06	0.1	ps RMS
		On	0.26	0.36	ps RMS
PCIe Gen3.0 SRIS	Includes PLL BW 4 MHz Peaking = 2dB & 1dB, Td=12 ns CDR = 10 MHz [2, 3]	On	0.31	0.36	ps RMS
PCIe Gen 4.0 Common Clock	Includes PLL BW 2–4 MHz & 5 MHz, Peaking = 0.01-2dB & 1dB, Td=12 ns, CDR = 10 MHz [2, 3]	Off	0.05	0.1	ps RMS
		On	0.26	0.36	ps RMS
PCIe Gen4.0 SRIS	Includes PLL BW 4 MHz Peaking = 2dB & 1dB, Td=12 ns CDR = 10 MHz [2, 3]	On	0.31	0.36	ps RMS
PCIe Gen5.0 Common Clock		Off	0.025	0.04	Ps RMS
		On	0.1	0.15	Ps RMS
PCIe Gen5.0 SRIS		On	0.08	0.1	Ps RMS

Notes:

1. All jitter data in this table is based upon all output formats being differential. When LVCMOS outputs are used, there is the potential that the output jitter may increase due to the nature of LVCMOS outputs. If your configuration implements any LVCMOS output and any output is required to have jitter less than 3 ps RMS, contact Silicon Labs for support to validate your configuration and ensure the best jitter performance.
2. All output clocks 100 MHz HCSL format. Jitter data taken from Clock Jitter Tool v.1.3.
3. Excludes oscilloscope sampling noise.

Table 5.11. Fanout Mode Additive Jitter Performance Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Typ	Max	Units
Additive Phase Jitter		156.25 MHz, 12 kHz-20 MHz[1], LVDS (slow mode)	130 (LVDS slow)	170	fs RMS
		156.25 MHz, 12kHz-20MHz, LVDS (fast mode)	120	150	fs RMS
		156.25 MHz, 12 kHz-20 MHz, LVPECL[1]	110	140	fs RMS
		156.25 MHz, 12 kHz-20 MHz, HCSL[1]	120	150	fs RMS
PCIe Gen3/4 Additive Phase Jitter	JADD_GEN3 JADD_GEN4	Includes PLL BW 2–4 MHz, CDR = 10 MHz	54	69	fs RMS
PCIe Gen5 Additive Phase Jitter	JADD_GEN5	Includes PLL BW 500 kHz - 1.8 MHz, CDR = 20 MHz	21	27	fs RMS

Note:

1. Measured with differential input on CLKIN_2, bypassing the PLL to any output.
2. Silicon Labs PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt(output jitter^2 - input jitter^2). Input used is 100 MHz from Si5340.
3. Measurements on 100 MHz output use the template file in the PCIe Clock Jitter Tool.
4. For complete PCIe specifications, visit www.pcisig.com.
5. Input clock slew rate of 3.0 V/ns used for jitter measurements.

Table 5.12. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Units
Si5332 — 40 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	23.1	°C/W
		Air Flow 1 m/s	17.5	
		Air Flow 2 m/s	16.5	
Thermal Resistance, Junction to Case	θ_{JC}	Still Air	13.4	
Thermal Resistance, Junction to Board	θ_{JB}	Still Air	8.7	
	Ψ_{JB}	Still Air	8.4	
Thermal Resistance, Junction to Top Center	Ψ_{JT}	Still Air	0.3	
Si5332 — 32 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	28.4	°C/W
		Air Flow 1 m/s	24	
		Air Flow 2 m/s	23	
Thermal Resistance, Junction to Case	θ_{JC}	Still Air	15.9	
Thermal Resistance, Junction to Board	θ_{JB}	Still Air	11.5	
	Ψ_{JB}	Still Air	11.2	
Thermal Resistance, Junction to Top Center	Ψ_{JT}	Still Air	0.4	

Note:
1. Based on a JEDEC standard 4-layer PCB.

Table 5.13. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	VDD_{xtal}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_I	XIN/XOUT	–0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Soldering Temperature	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK}	T_P		20 to 40	sec

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
3. The device is compliant with JEDEC J-STD-020.

6. Pin Descriptions

6.1 Pin Descriptions (40-QFN)

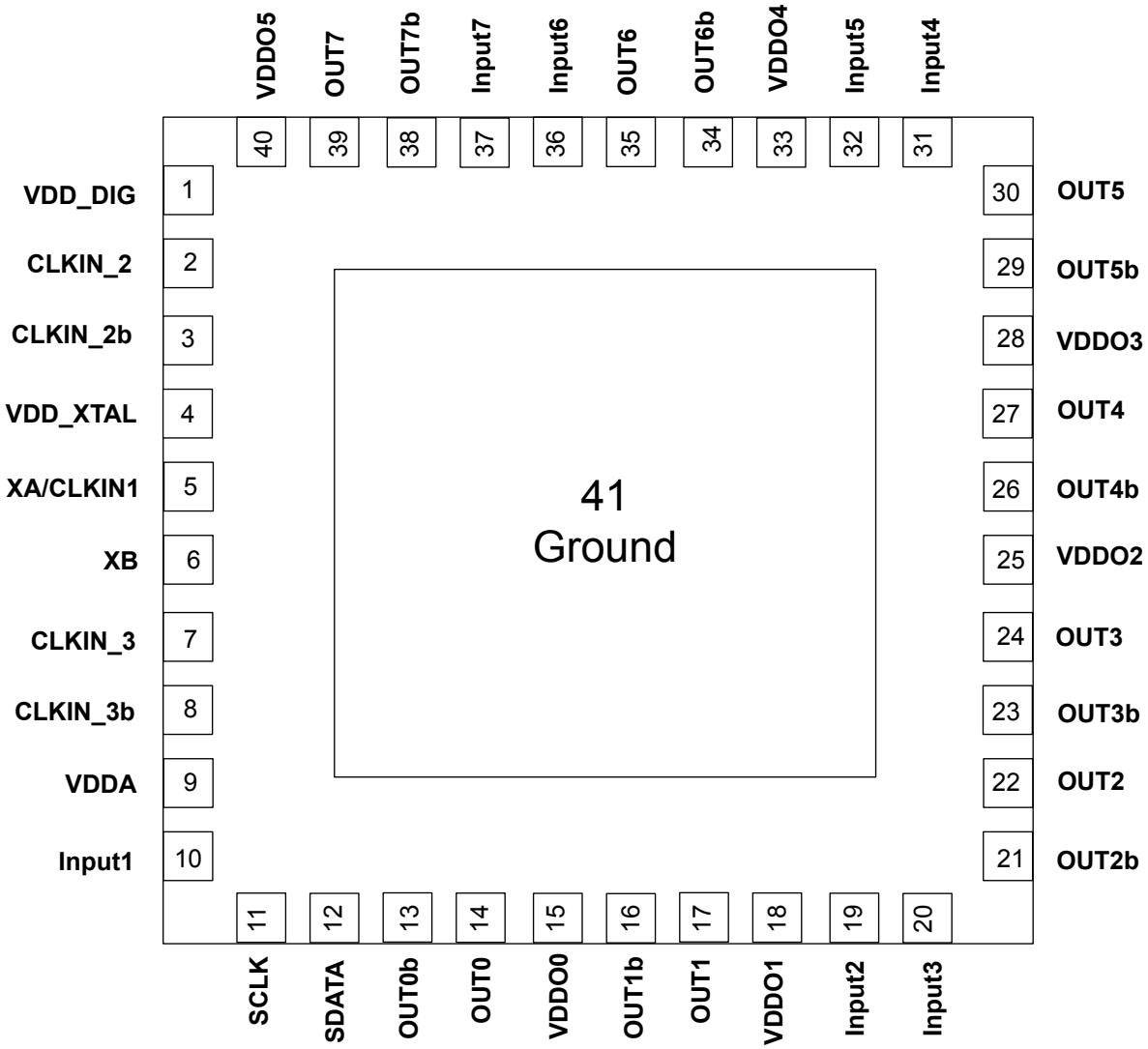


Figure 6.1. 40-QFN

Table 6.1. Si5332 Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL.
2	CLKIN_2	I	These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_2b	I	
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	XA/CLKIN1	I	**Si5332A/B/C/D:** These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Refer to Section 5. Electrical Specifications for recommended crystal specifications.
6	XB	O	
7	CLKIN_3	I	These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_3 and CLKIN_3b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
8	CLKIN_3b	I	
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
10	INPUT1	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
11	SCLK	I	**Serial Clock Input** This pin functions as the serial clock input for I^2C. SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG.
12	SDATA	I/O	**Serial Data Interface** This is the bidirectional data pin for the I^2C mode. SDA is a digital, open-drain, bi-directional pin internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG.
13	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
14	OUT0	O	

Pin Number	Pin Name	Pin Type	Function
15	VDDO0	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	INPUT2	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
20	INPUT3	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
22	OUT2	O	
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT2 and OUT3** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
27	OUT4	O	

Pin Number	Pin Name	Pin Type	Function
28	VDDO3	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT4 and OUT5** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
30	OUT5	O	
31	INPUT4	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
32	INPUT5	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
33	VDDO4	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
35	OUT6	O	
36	INPUT6	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
37	INPUT7	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
38	OUT7b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
39	OUT7	O	
40	VDDO5	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT7** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.

Pin Number	Pin Name	Pin Type	Function
41	GND PAD	P	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.2 Pin Descriptions (32-QFN)

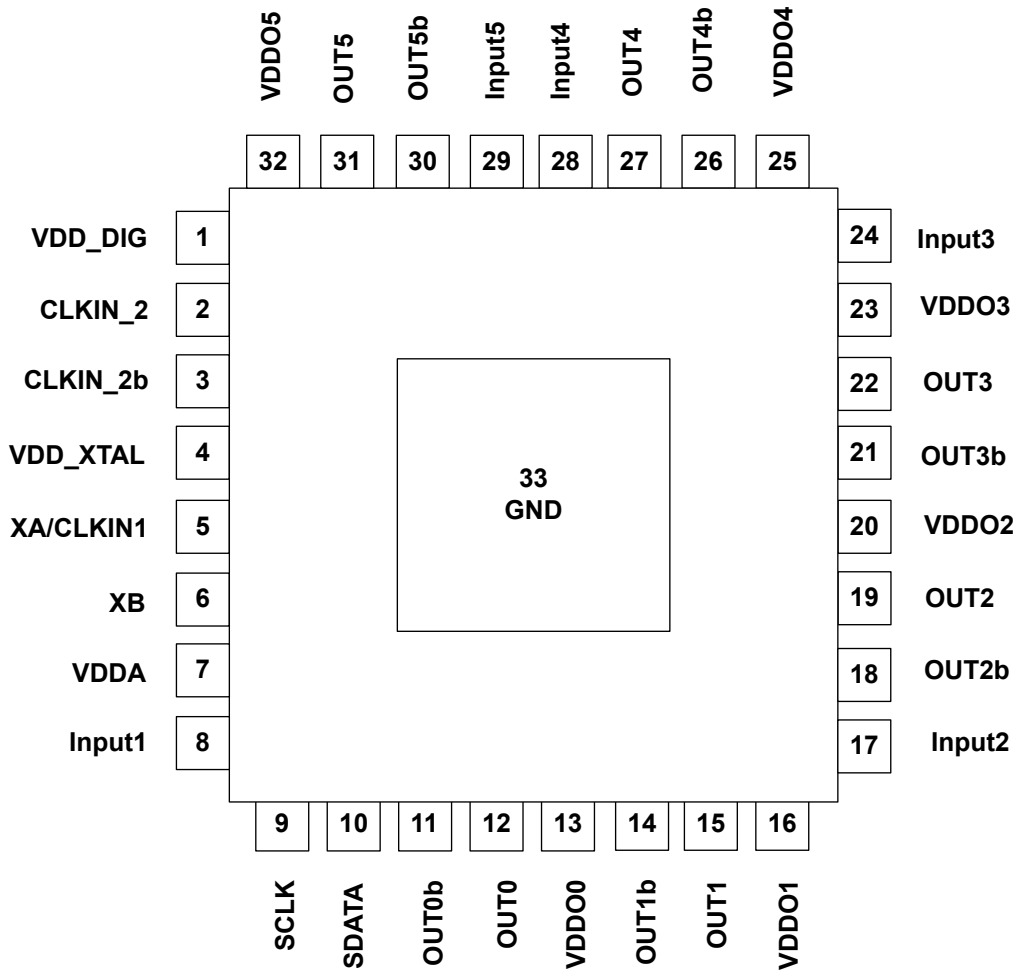


Figure 6.2. 32-QFN

Table 6.2. Si5332 Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL.
2	CLKIN_2	I	These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Un-used".
3	CLKIN_2b	I	
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	XA/CLKIN1	I	**Si5332A/B/C/D** These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Refer to Section 5. Electrical Specifications for recommended crystal specifications.
6	XB	O	

Pin Number	Pin Name	Pin Type	Function
7	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
8	INPUT1	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
9	SCLK	I	**Serial Clock Input** This pin functions as the serial clock input for I^2C. SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG.
10	SDATA	I/O	**Serial Data Interface** This is the bidirectional data pin for the I^2C mode. SDA is a digital, open-drain, bi-directional pin internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG.
11	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
12	OUT0	O	
13	VDDO0	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
15	OUT1	O	
16	VDDO1	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	INPUT2	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.

Pin Number	Pin Name	Pin Type	Function
18	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
19	OUT2	O	
20	VDDO2	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT2** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
21	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
22	OUT3	O	
23	VDDO3	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT3** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
24	INPUT3	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
25	VDDO4	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT4** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
27	OUT4	O	
28	INPUT4	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.
29	INPUT5	I/O	Universal HW pin. This hardware pin is user-definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Pins for a list of definitions that hardware input pins can be used for.

Pin Number	Pin Name	Pin Type	Function
30	OUT5b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
31	OUT5	O	
32	VDDO5	P	**Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT5** See the Si5332-AM1/2/3 Family Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
33	GND PAD	P	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

7. Package Outline

7.1 Si5332 6x6mm 40-QFN Package Diagram

The figure below illustrates the package details for the Si5332A/B/C/D in 40-QFN. The table below lists the values for the dimensions shown in the illustration.

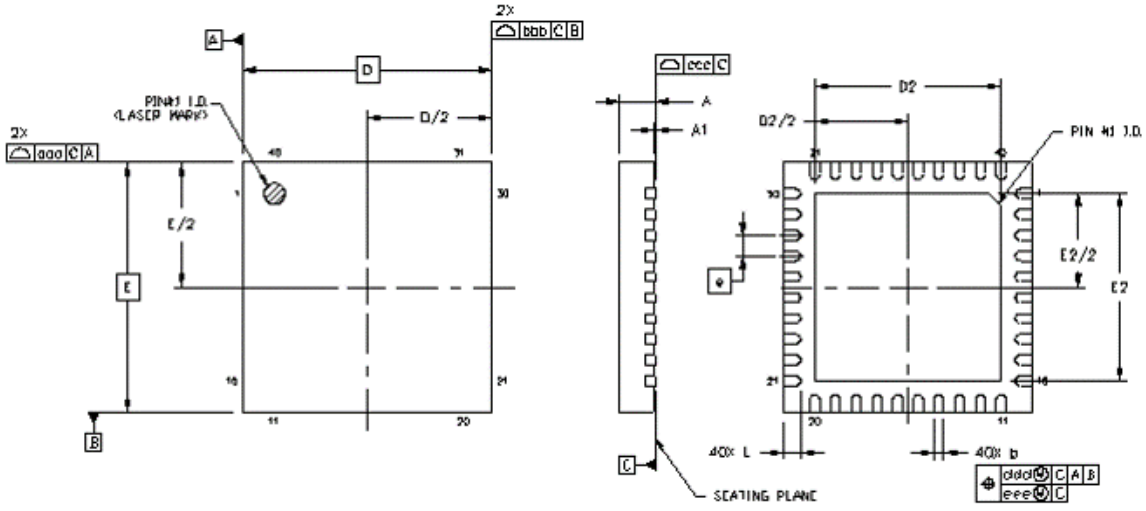


Figure 7.1. 40-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee			0.05

Dimension	Min	Nom	Max

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 Si5332 5x5mm 32-QFN Package Diagram

The figure below illustrates the package details for the Si5332A/B/C/D 32-QFN option. The table below lists the values for the dimensions shown in the illustration.

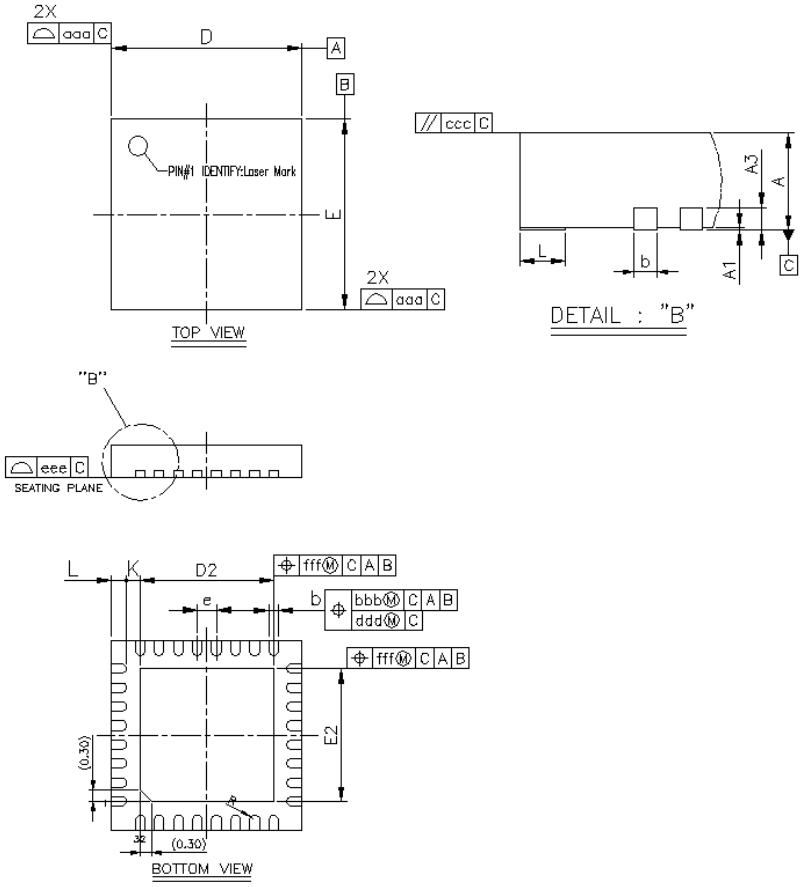


Figure 7.2. 32-Pin Quad Flat No-Lead (QFN)

Table 7.2. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	

Dimension	MIN	NOM	MAX
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1 6x6mm 40-QFN Land Pattern

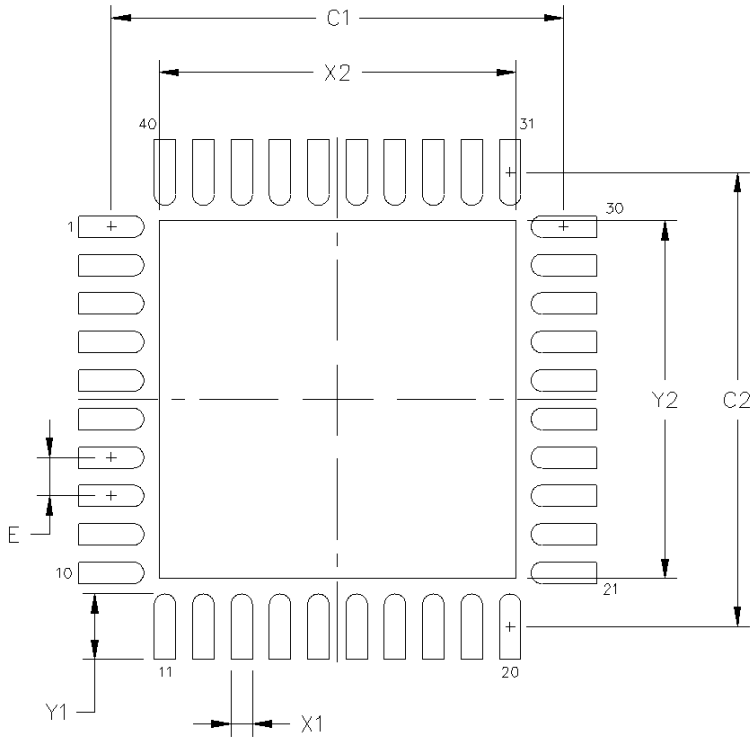


Figure 8.1. 40-QFN Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. The stencil aperture to land pad size recommendation is 70% paste coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 5x5mm 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for Si5332 in 32-QFN package. The table below lists the values for the dimensions shown in the illustration.

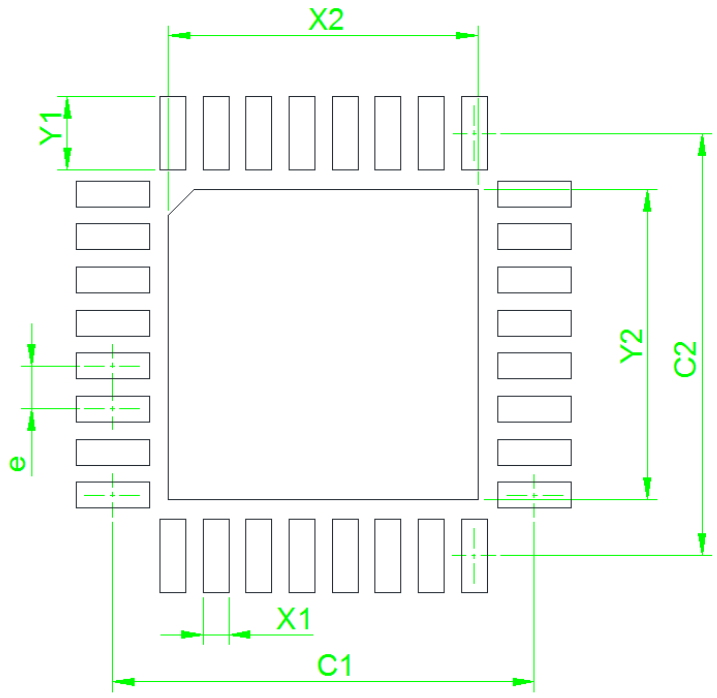


Figure 8.2. 32-QFN Land Pattern

Table 8.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. The stencil aperture to land pad size recommendation is 70% paste coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

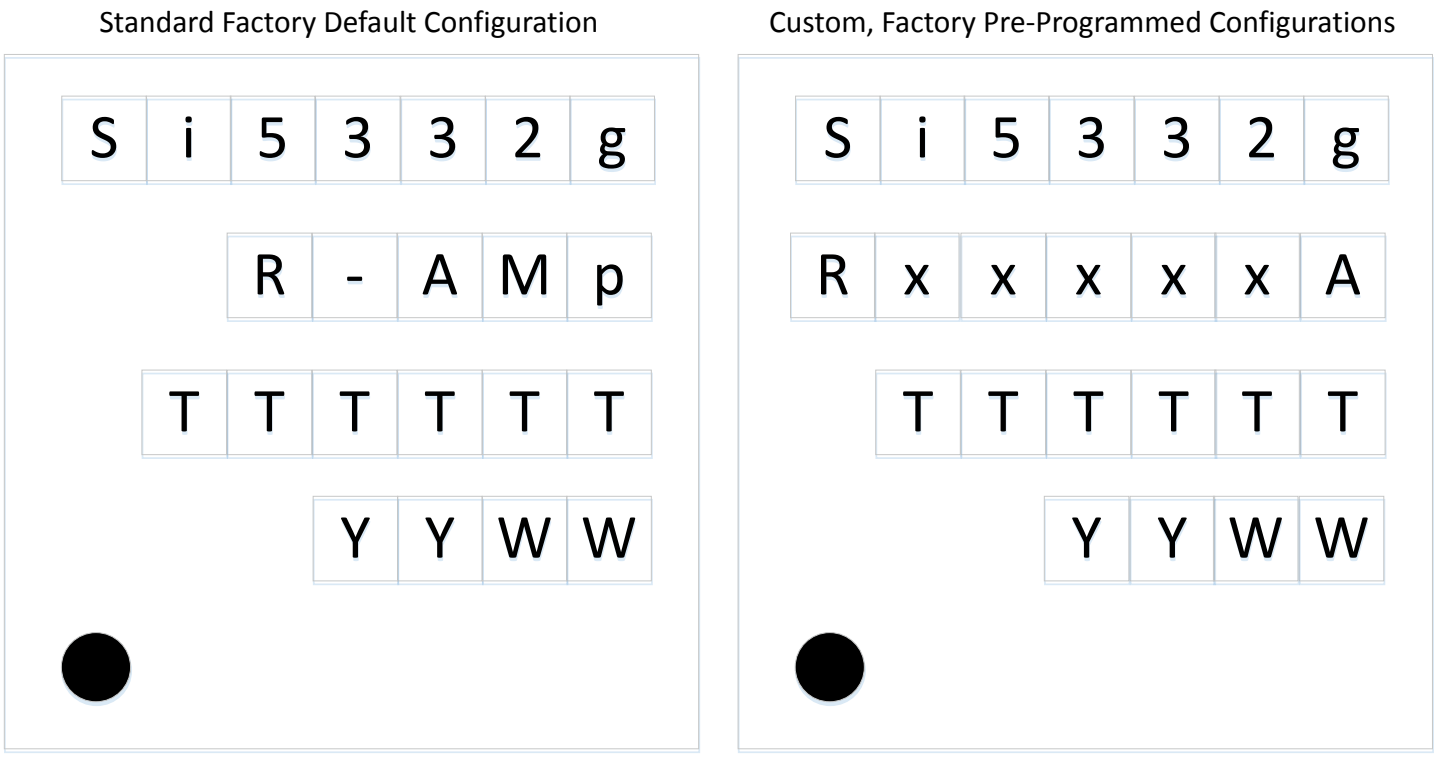


Figure 9.1. Si5332 Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description
1	Si5332g	Si5332 = Base part number
		g = Device Grade (A, B, C, D)
2	R-AMp	R = Product revision (see Ordering Guide for current revision)
		- = Dash character
		AM = Automotive grade temperature range (-40 °C to +105 °C) and Package (QFN)
		p = Package Size • 1 = 6-output, 32-pin QFN • 2 = 8-output, 40-pin QFN
	RxxxxxA	R = product revision
		xxxxx = Customer specific NVM sequence number. NVM code assigned for custom, factory pre-programmed devices using ClockBuilder Pro. See Ordering Guide for more information.
3	TTTTTT	Manufacturing trace code
4	YYWW	Year (YY) and work week (WW) of package assembly

10. Document Change List

Revision 1.0

July, 2020

- Added AEC-Q100 qualified.
- Updated Stencil Design notes in 8. PCB Land Pattern.

Revision 0.7

September, 2019

- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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