Si53358/4/2 データシート

8/4/2-出力クロック・バッファ

汎用/ピン選択可能な形式の Si53358/54/52 デバイスは、業界で最高の性能と最も低い電力を特長とした車載用ファンアウト・バッファです。Si53358、Si53354、および Si53352 は、それぞれ 8、4、および 2 つの差動クロック出力を生成します。これらのデバイスは、標準の 120 fs 付加位相ジッタ特性を備え、10 ～ 250 MHz の周波数帯域で動作します。内蔵の LDO によって 高 PSNR 性能を実現し、外部部品の必要性を低減することで、ノイズの多い環境で低ジッタ・クロック分配を簡素化します。

Si5335x ファミリは、ピン選択可能な入力/出力形式のバージョンと完全にカスタマイズ可能なバージョンの両方でご提供しています。完全にカスタマイズ可能なバージョンでは、ClockBuilder Pro を使用して入力/出力形式と入力ハードウェア・ピンを定義して、正確なシステム要件に一致させることができます。ClockBuilder Pro を使用すると、出力ごとに個別に信号形式を定義し、2:1 の入力多重通信回路を有効化して、入力/出力電圧変換を定義できます。これらの機能に加えて、入力クロックの LOS モニタを有効にすることができます。

アプリケーション：

- インフォテインメント
- ADAS ECU
- レーダー・センサー
- LiDar センサー

主な機能

- 8/4/2 出力
- 入力喪失クロック用ロス・オブ・シグナル（LOS）モニタ
- 車載グレード 2：-40 ～ +105 °C
- 10 ～ 250 MHz 周波数帯域
- ClockBuilder Pro を使用した完全にカスタマイズ可能な構成
- 優れた付加ジッタ性能
  - 120 fs RMS、156.25 MHz
- 出力イネーブルのための個別のハードウェア制御ピン
- MUX によるオプションのデュアル入力機能
- 1.8 ～ 3.3 V 電源
- 鉛フリー対応、RoHS-6 準拠

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- 8/4/2 出力
- 入力喪失クロック用ロス・オブ・シグナル（LOS）モニタ
- 車載グレード 2：-40 ～ +105 °C
- 10 ～ 250 MHz 周波数帯域
- ClockBuilder Pro を使用した完全にカスタマイズ可能な構成
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  - 120 fs RMS、156.25 MHz
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- 1.8 ～ 3.3 V 電源
- 鉛フリー対応、RoHS-6 準拠

2. Ordering Guide

Input/Output Format Configuration	Number of Inputs	Number of Outputs	Part Number	Package Type	Temperature
Pin-Selectable	1	2	Si53352A-D01AM	32-pin QFN	-40 °C to +105 °C, Automotive Grade 2
	1	4	Si53354A-D01AM	40-pin QFN	
	2	8	Si53358A-D01AM	40-pin QFN	
User-Defined (ClockBuilder Pro)	1	2	Si53352BDxxxxx-AM	32-pin QFN	
	1	4	Si53354BDxxxxx-AM	40-pin QFN	
	2	8	Si53358BDxxxxx-AM	40-pin QFN	

Note:

1. For user-defined devices, the “xxxxx” suffix is generated by ClockBuilder Pro after a configuration file is created.
2. For tape and reel, add "R" to the end of the orderable part number.

3. Functional Description

3.1 Functional Block Diagrams

3.1.1 Si53352A-D01AM Functional Block Diagram

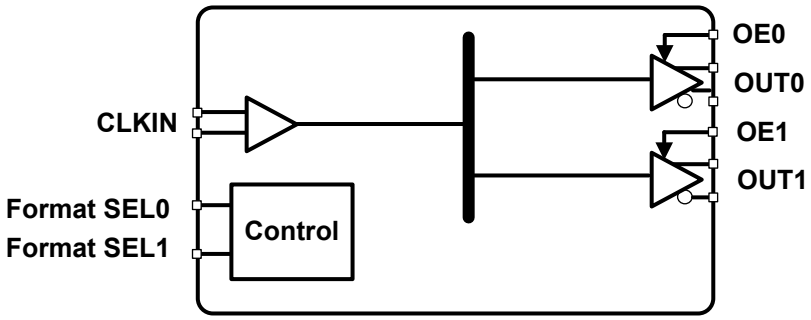


Figure 3.1. Si53352A-D01AM Functional Block Diagram

3.1.2 Si53354A-D01AM Functional Block Diagram

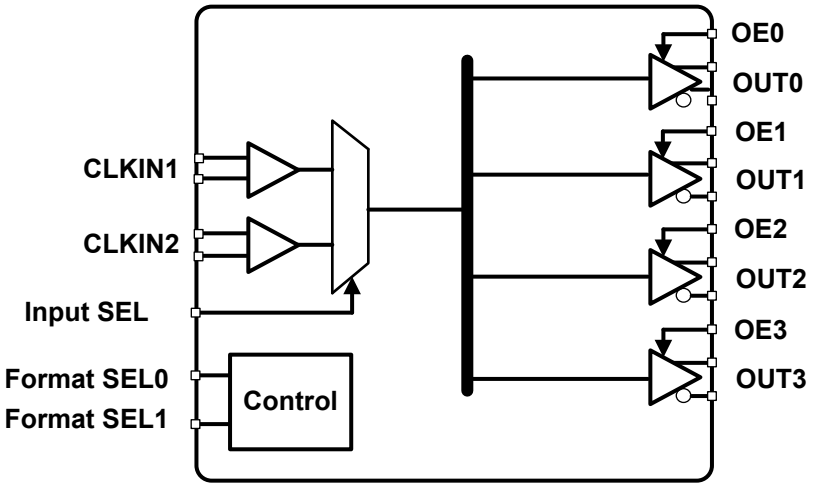


Figure 3.2. Si53354A-D01AM Functional Block Diagram

3.1.3 Si53358A-D01AM Functional Block Diagram

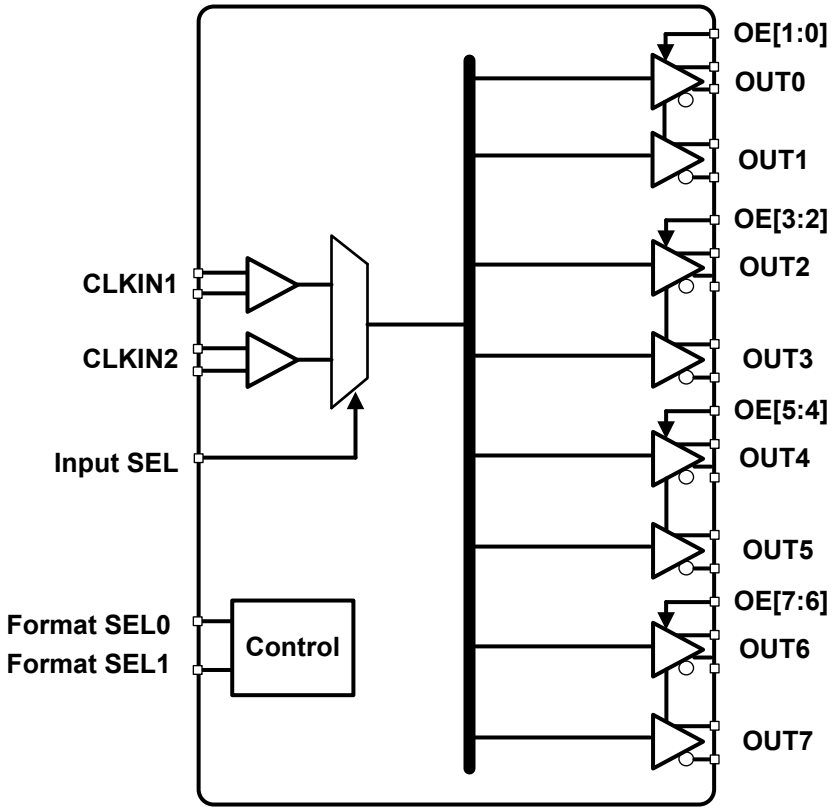


Figure 3.3. Si53358A-D01AM Functional Block Diagram

3.1.4 Si53352BDxxxxx-AM Functional Block Diagram

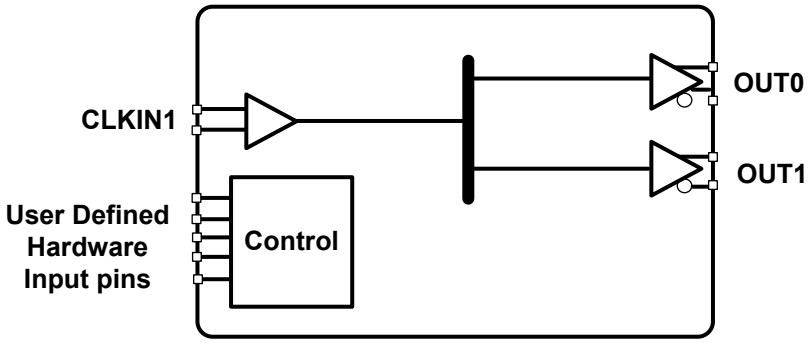


Figure 3.4. Si533252BDxxxxx-AM Functional Block Diagram

3.1.5 Si53354BDxxxxx-AM Functional Block Diagram

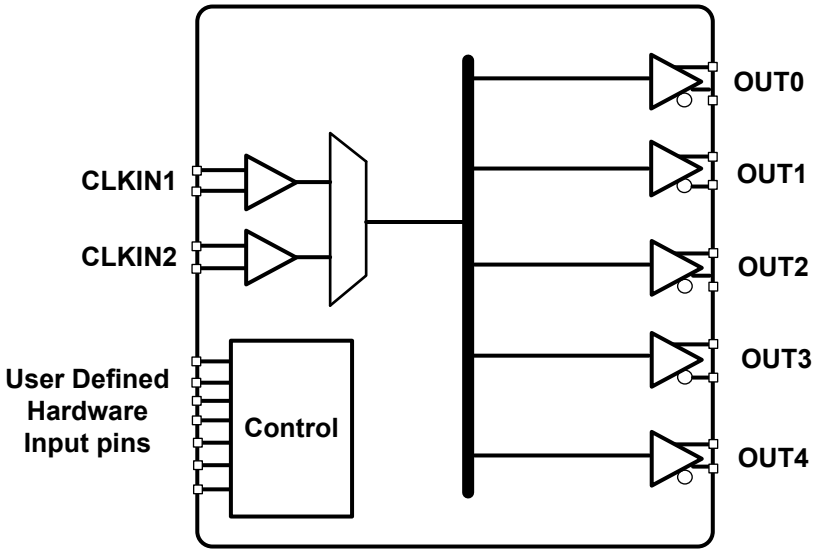


Figure 3.5. Si53354BDxxxxx-AM Functional Block Diagram

3.1.6 Si53358BDxxxxx-AM Functional Block Diagram

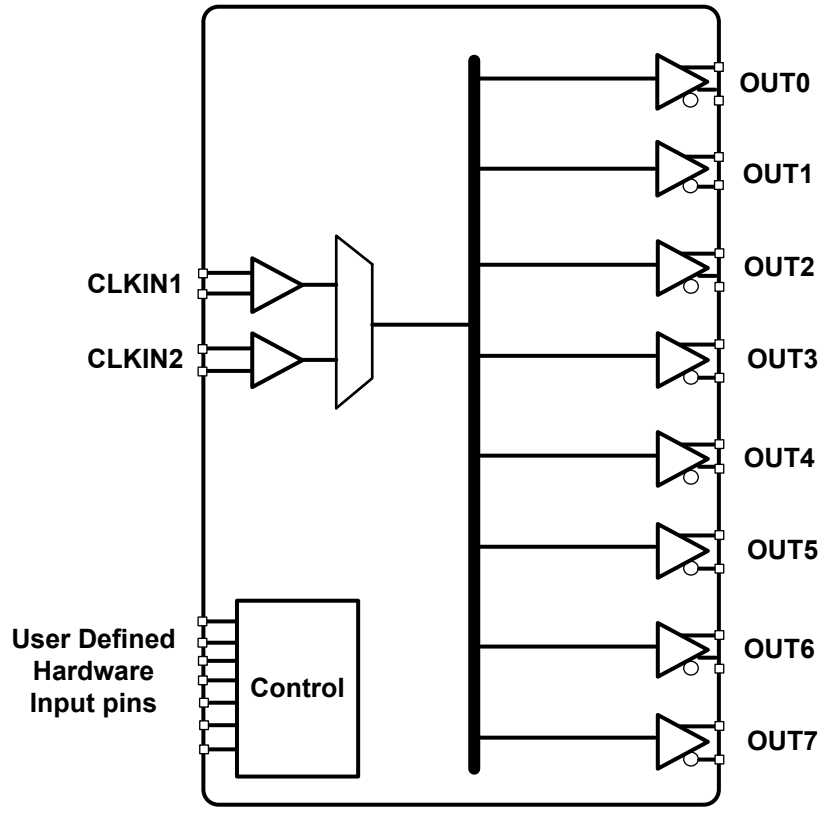


Figure 3.6. Si53358BDxxxxx-AM Functional Block Diagram

3.2 Output Signal Formats

The differential output swing and common mode voltage are compatible with a wide variety of signal formats including HCSL, LVDS, and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS drivers, enabling the device to support both differential and single-ended clock outputs. Output formats can be defined in ClockBuilder Pro or via the serial interface.

Si53352A-D01AM, Si53354A-D01AM, and Si53358A-D01AM signal formats can be set using the pre-defined hardware input pins as follows:

Format_SEL0	Format_SEL1	Output Format
0	0	LVCMOS (in-phase, dual outputs)
0	1	LVPECL
1	0	LVDS
1	1	HCSL (100 Ω)

3.2.1 Differential Output Terminations

LVDS Driver Termination

For a general LVDS interface, the recommended value for the differential termination impedance (Z_T) is between 90 Ω and 132 Ω. Select the actual value to match the differential impedance (Z0) of the transmission line. A typical point-to-point LVDS design uses a 100 Ω parallel resistor at the receiver and a 100 Ω differential transmission-line environment. To avoid any transmission-line reflection issues, surface mount the components and place them as close to the receiver as possible. The standard LVDS termination schematic as shown in Figure 3.7 Standard LVDS Termination on page 8 can be used with either type of output structure. Figure 3.8 Optional LVDS Termination on page 8, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 0.01 to 0.1 µF. If using a non-standard termination, contact Silicon Labs to confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

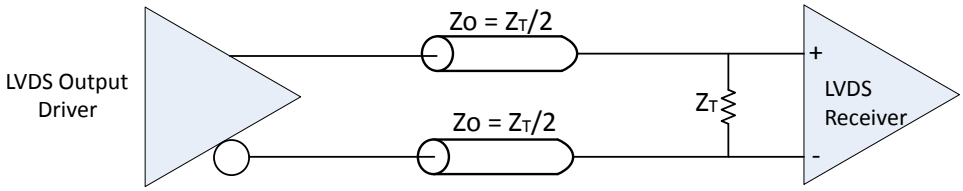


Figure 3.7. Standard LVDS Termination

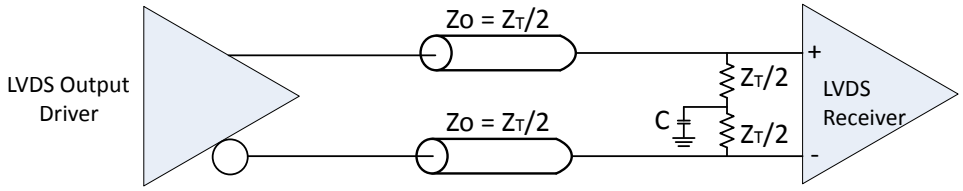


Figure 3.8. Optional LVDS Termination

Termination for 3.3 V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Use matched impedance techniques to maximize operating frequency and minimize signal distortion. Figure 3.9 3.3 V LVPECL Output Termination, Option 1 on page 9 and Figure 3.10 3.3 V LVPECL Output Termination, Option 2 on page 9 show two different layouts. Other suitable clock layouts may exist, but it is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

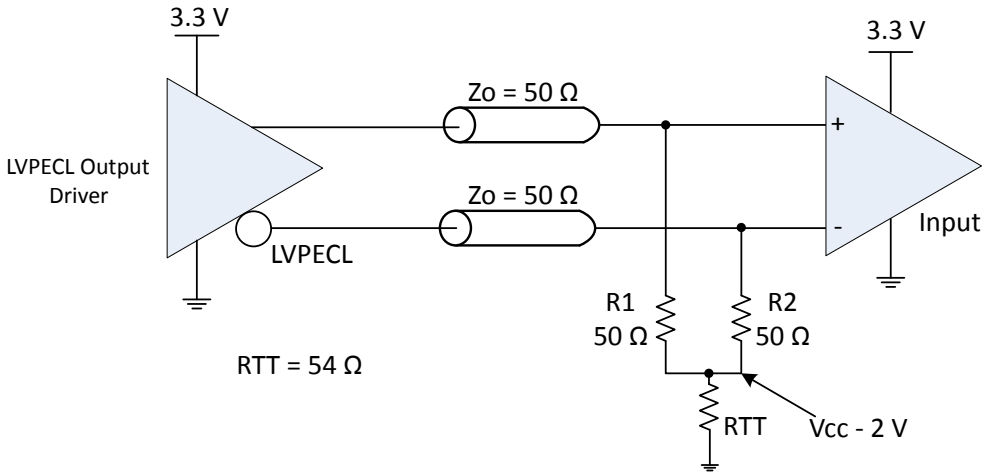


Figure 3.9. 3.3 V LVPECL Output Termination, Option 1

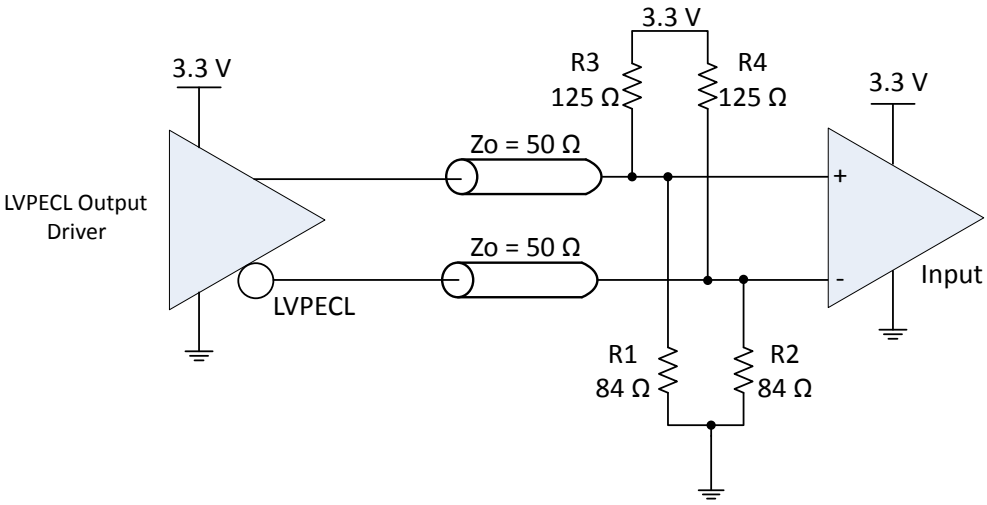


Figure 3.10. 3.3 V LVPECL Output Termination, Option 2

Termination for 2.5 V LVPECL Outputs

Figure 3.11 2.5 V LVPECL Termination Example, Option 1 on page 10 and Figure 3.12 2.5 V LVPECL Termination Example, Option 2 on page 10 show examples of termination for the 2.5 V LVPECL driver option. These terminations are equivalent to terminating 50 Ω to VDDO – 2 V. For VDDO = 2.5 V, the VDDO – 2 V is very close to ground level. The R3 in Figure 3.12 2.5 V LVPECL Termination Example, Option 2 on page 10 can be optionally eliminated using the termination shown in Figure 3.11 2.5 V LVPECL Termination Example, Option 1 on page 10.

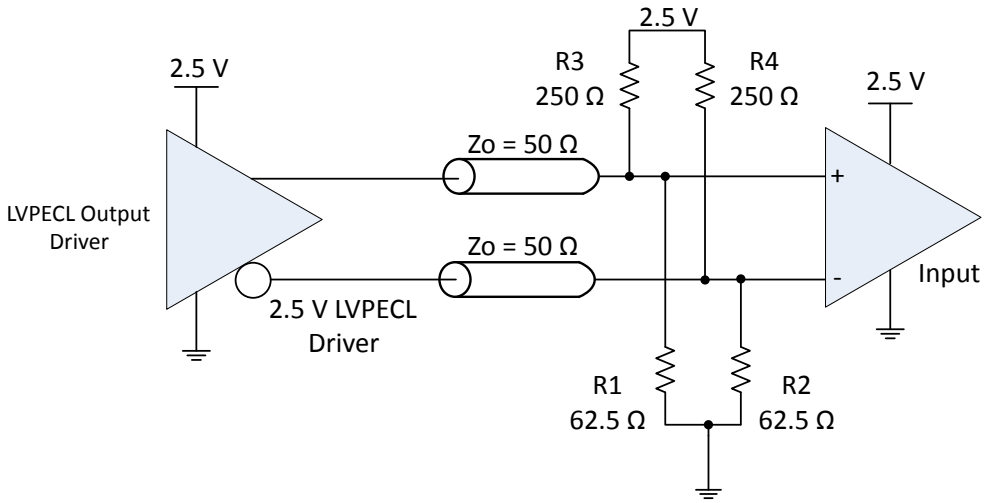


Figure 3.11. 2.5 V LVPECL Termination Example, Option 1

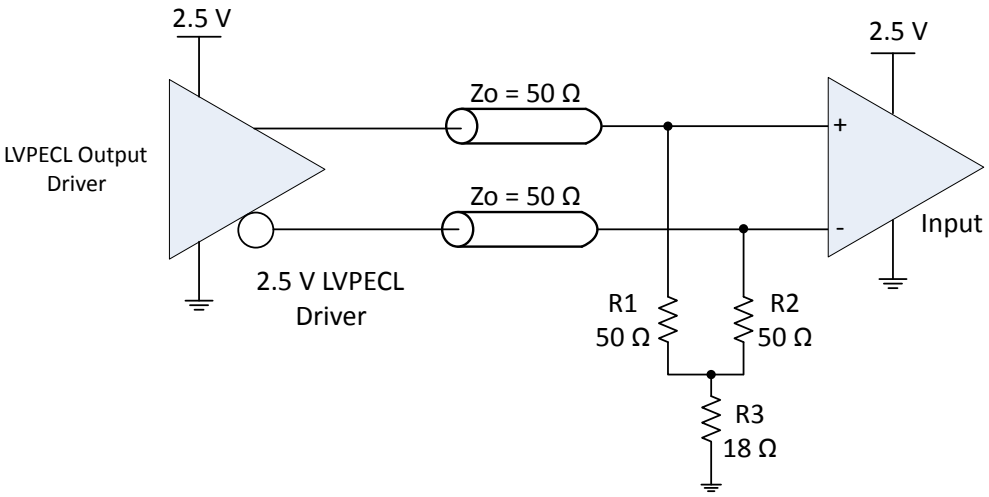


Figure 3.12. 2.5 V LVPECL Termination Example, Option 2

3.2.2 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.

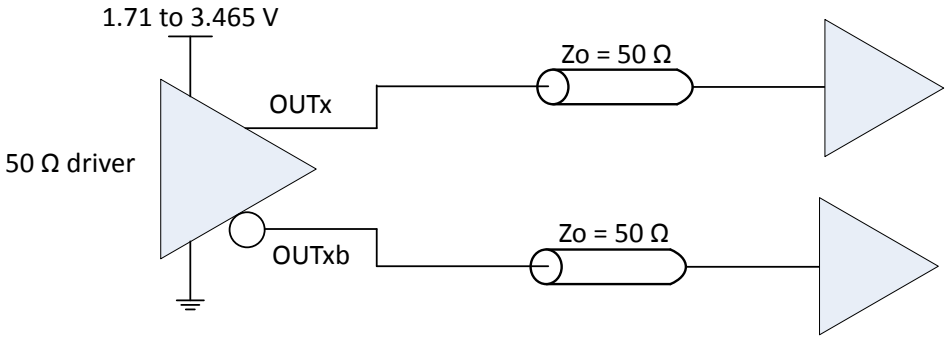


Figure 3.13. LVCMOS Output Termination Example, Option 1

3.2.3 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

3.2.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTxb pin is generated in phase with the clock on the OUTx pin.

3.2.5 Termination for HCSL Outputs

The Si5335x HCSL driver features integrated termination resistors to simplify interfacing to an HCSL receiver.

Si53352A-D01AM, Si53354A-D01AM, Si53358A-D01AM feature HCSL drivers set to match 100 Ω impedance.

Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, and Si53358BDxxxxx-AM feature programmable HCSL output drivers that can be set to match either 100 Ω or 85 Ω impedance in ClockBuilder Pro.

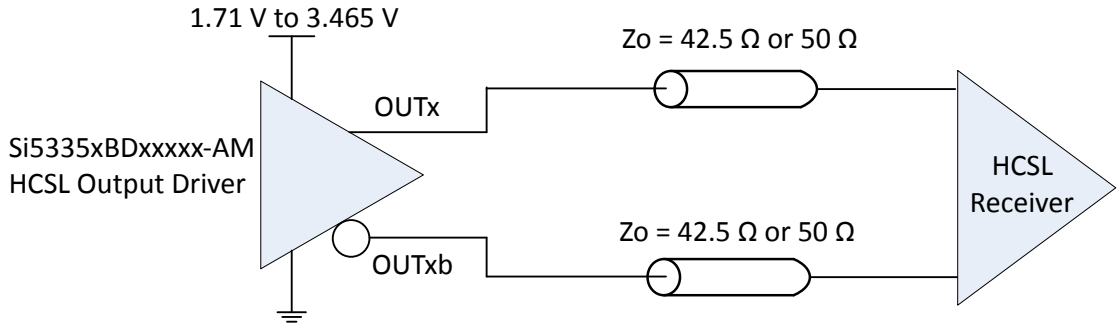


Figure 3.14. HCSL Internal Termination Mode

3.3 Output Enable/Disable

Output enable hardware pins provide a convenient method of disabling or enabling the output drivers. When the output enable pin is held high all designated outputs will be disabled. When held low, the designated outputs will be enabled.

Si53352A-D01AM, Si53354A-D01AM, Si53358A-D01AM have pre-defined output enable pins. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 µs for the output to have a clean clock. Output enabled/disabled for LVCMOS are done in pairs. Each differential buffer True and Compliment output can generate an LVCMOS clock and the OE pin associated with the True and Compliment output buffer will control the respective LVCMOS pair.

Users can opt to define universal hardware pins on Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, and Si53358BDxxxxx-AM as output enable for any output, or any combination of outputs. See Section 3.4 for more details.

3.4 Universal Hardware Input Pins (Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, and Si53358BDxxxxx-AM)

Universal hardware input pins are user-configurable control input pins that can have one or more of the functions listed below assigned to them using ClockBuilder Pro.

Universal hardware pins can be utilized for the following functions:

Description	Type	Function
OE	Input	Output enable for one or more outputs.
Input SEL	Input	Selects between input sources, if 2 input clocks are defined.
LOS	Output	Loss of signal monitor

Output Enable

A universal hardware input pin can be defined to control output enable of a differential output, a bank of differential outputs, or as a global output enable pin controlling all outputs. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 µs for the output to have a clean clock.

Input SEL

A universal hardware input pin can be defined to set the input source clock between the input clocks, if two input clock sources are defined. Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

Loss of Signal (LOS)

LOS is a feature that can be implemented during configuration file development using ClockBuilder Pro on a customized device. The LOS indicator is used to check for the presence of an input reference source (crystal or clock). Users can choose either active high or active low logic when the LOS pin is defined. LOS will assert when the reference source frequency drops below the minimum input frequency specifications noted in Table 5.3 Clock Input Specifications on page 15.

For Active High:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic high (LOS = 1) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic low (LOS = 0) state.

For Active Low:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic low (LOS = 0) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic high (LOS = 1) state.

4. Power Supply Filtering Recommendations

The Si5335x features internal LDOs on each power supply pin, providing excellent power supply noise rejection. As a guideline, each power supply pin should use a parallel combination of a 1 µf and a 0.1 µF bypass capacitor placed as close to the supply pin as possible.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	25	105	°C
Junction Temperature	TJ_{MAX}		—	—	125	°C
Core Supply Voltage	V_{DDA}, V_{DD_DIG}, V_{DD_xtal}		1.71	—	3.46	V
Output Driver Supply Voltage	V_{DDO}		1.71	—	3.46	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

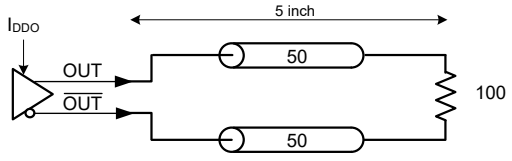
(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Core Supply Current	I_{DD}		—	11	18	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[1] @ 156.25 MHz	—	33	35	mA
		HCSL Output[1] @ 100 MHz	—	20	22	mA
		LVDS Output[1] @ 156.25 MHz	—	11	13	mA
		3.3 V VDDO LVCMOS[2] output @ 170 MHz	—	16	19	mA
		2.5 V VDDO LVCMOS[2] output @ 170 MHz	—	9	11	mA
		1.8 VDDO LVCMOS[2] output @ 170 MHz	—	7.5	8.5	mA
Total Power Dissipation	P_d	40-pin		260	670	mW
		32-pin	—	80	215	mW

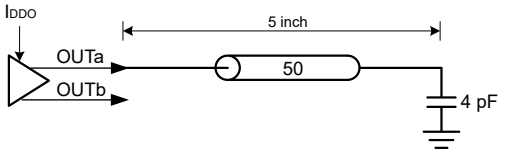
Notes:

1. Differential outputs terminated into a 100 Ω load.
2. LVCMOS outputs measured into a 5 inch 50 Ω PCB trace with 4 pF load.

Differential Output Test Configuration



LVCMOS Output Test Configuration



3. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 5.3. Clock Input Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC-coupled Differential Input Clock on CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#)						
Frequency	F_{IN}	Differential	10	—	250	MHz
Voltage Swing	V_{PP_DIFF}[3]	Differential AC-coupled < 250 MHz	0.5	—	1.8	V_{PP_diff}
Slew Rate	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		2	3.5	6	pF
Input Clock (AC-coupled LVCMOS Input Clock on CLKIN_2 or CLKIN_3)						
Frequency	F_{IN}		10	—	170	MHz
Input High Voltage	V_{IH}		0.8 × V_{DD}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.2 × V_{DD}	V
Slew Rate[1,2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		2	3.5	6	pF

Notes:
1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20}$ = ((0.8 - 0.2) * $V_{IN\_Vpp\_se}$) / SR.
3. V_{PP_DIFF} = 2 x $V_{PP\_SINGLE\text{-}ENDED}$

Table 5.4. Control Pins

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5332 Control Input Pins (Inputx)						
Input Voltage	V_{IL}		-0.1	—	0.3 × VDD[1]	V
	V_{IH}		0.7 × VDD[1]	—	1.1 × V_{DD}	V
Input Capacitance	C_{IN}		—	—	4	pF
Pull-up/down Resistance	R_{IN}		—	50	—	kΩ

Note:
1. V_{DD} indicates all core voltages V_{DD_DIG}, V_{DDA}, and V_{DD_XTAL} which are required to all be using same nominal voltage.

Table 5.5. Differential Clock Output Specifications

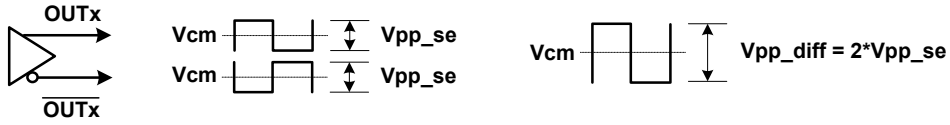
(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Duty Cycle	DC			48	—	52	%
Output-Output Skew	T_{SK}	Within the same bank		—	—	30	ps
		Across banks		—	—	80	ps
Output Voltage Swing	V_{SEPP}	LVPECL		0.6	0.75	0.85	V_{PP}
		LVDS	1.8/2.5/3.3 V	0.3	0.375	0.45	V_{PP}
		HCSL		0.7	0.8	0.9	V_{PP}
Common Mode Voltage	V_{CM}	LVPECL		—	VDDO-1.4	—	V
		LVDS	2.5/3.3 V	1.125	1.2	1.275	V
		LVDS	1.8 V	0.75	0.8	0.85	V
		HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 12,14,18		1	—	4.5	V/ns
HCSL Delta Tr	D_{tr}	Notes 14, 17, 18		—	—	155	ps
HCSL Delta Tf	D_{tf}	Notes 14, 17, 18		—	—	155	ps
HCSL Vcross Abs	V_{xa}	Notes 11,13, 14, 17		250	—	550	mV
HCSL Delta Vcross	D_{vcrs}	Notes 14, 17		—	—	140	mV
HCSL Vovs	V_{ovs}	Notes 14, 17		—	—	V_{HIGH}+300	mV
HCSL Vuds	V_{uds}	Notes 14, 17		—	—	V_{LOW}-300	mV
HCSL Vrng	V_{rng}	Notes 14, 17		V_{HIGH}-200	—	V_{LOW}+200	mV
Rise and Fall Times (20% to 80%)	t_R/t_F	LVDS (fast mode)	3.3 V or 2.5 V	150	200	350	ps
		LVDS (slow mode)	3.3 V or 2.5 V	350	530	620	ps
			1.8 V	150	225	350	ps
Rise and Fall Times (20% to 80%)	t_R/t_F	LVPECL		150	—	320	ps
		HCSL		—	—	420	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units

Notes:

1. For best jitter performance, keep the midpoint differential input slew rate faster than 0.3 V/ns.
2. Not in PLL bypass mode.
3. For best jitter performance, keep the midpoint input single ended slew rate faster than 1 V/ns.
4. On chip termination resistance can be programmed on (100 Ω) or off (high impedance).
5. Not including R divider.
6. Input capacitance on crystal pins targets 23 pf each plus 1 pf external trace capacitance to provide 12 pf series equivalent crystal load capacitance.
7. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
8. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
9. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
10. Test configuration is Rs = 33.2 Ω, Rp = 49.9, 2 pF.
11. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700), Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg).
12. Measurement taken from Single Ended waveform.
13. Measurement taken from differential waveform VLow Math function.
14. Overshoot is defined as the absolute value of the maximum voltage.
15. Undershoot is defined as the absolute value of the minimum voltage.
16. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
17. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system.
18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.



19. LVDS swing levels for 50 Ω transmission lines.
20. Max frequency is 250 MHz.

Table 5.6. LVCMOS Clock Output Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	fout	1.8-3.3 V CMOS	5	—	170	MHz
		1.5 V CMOS	5	—	133.33	MHz
Rise/Fall Time, 3.3 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace, CL = 4 pf	—	0.5	0.8	ns
Rise/Fall Time, 2.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.6	0.95	ns
Rise/Fall Time, 1.8 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.75	1.3	ns
Rise/Fall Time, 1.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.9	1.3	ns
CMOS Output Resistance (Single Strength)		3.3 V	—	46	—	Ω
		2.5 V	—	48	—	Ω
		1.8 V	—	53	—	Ω
		1.5 V	—	58	—	Ω
CMOS Output Resistance (Double Strength)		3.3 V	—	23	—	Ω
		2.5 V	—	24	—	Ω
		1.8 V	—	27	—	Ω
		1.5 V	—	29	—	Ω
CMOS Output Voltage	V_{OH}	–4 mA load	VDDO-0.3	—	—	V
	V_{OL}	4 mA load	—	—	0.3	V
Duty Cycle	DC	XO and PLL mode	45	—	55	%

Table 5.7. Performance Characteristics

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Clock Stabilization from Power-up	t_{STABLE}	Time for clock outputs to appear after POR	—	15	25	ms

Table 5.8. Additive Jitter Performance Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +5%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Typ	Max	Units
Additive Phase Jitter		156.25 MHz, 12 kHz-20 MHz[1], LVDS (slow mode)	130 (LVDS slow)	170	fs RMS
		156.25 MHz, 12 kHz-20 MHz, LVDS (fast mode)	120	150	fs RMS
		156.25 MHz, 12 kHz-20 MHz, LVPECL[1]	110	140	fs RMS
		156.25 MHz, 12 kHz-20 MHz, HCSL[1]	120	150	fs RMS
PCIe Gen3/4 Additive Phase Jitter		100 MHz HCSL input/outputs Includes PLL BW 2–4 MHz, CDR = 10 MHz[2, 3, 4, 5]	54	64	fs RMS
PCIe Gen5 Additive Phase Jitter		100 MHz HCSL input/outputs Includes PLL BW 500 kHz - 1.8 MHz, CDR = 20 MHz[2, 3, 4, 5]	21	27	fs RMS

Note:

1. Measured with differential input on CLKIN_2, bypassing the PLL to any output.
2. Silicon Labs PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt(output jitter^2 - input jitter^2). Input used is 100 MHz from Si5340.
3. Measurements on 100 MHz output use the template file in the PCIe Clock Jitter Tool.
4. For complete PCIe specifications, visit www.pcisig.com.
5. Input clock slew rate of 3.0 V/ns used for jitter measurements.

Table 5.9. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Units
Si53258 — 40 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	23.1	°C/W
		Air Flow 1 m/s	17.5	
		Air Flow 2 m/s	16.5	
Thermal Resistance, Junction to Case	θ_{JC}		13.4	
Thermal Resistance, Junction to Board	θ_{JB}		8.7	
	Ψ_{JB}		8.4	
Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.3	
Si53254 — 32 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	28.4	°C/W
		Air Flow 1 m/s	24	
		Air Flow 2 m/s	23	
Thermal Resistance, Junction to Case	θ_{JC}		15.9	
Thermal Resistance, Junction to Board	θ_{JB}		11.5	
	Ψ_{JB}		11.2	
Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.4	

Note:
1. Based on JEDEC standard 4-layer PCB.

Table 5.10. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	VDD_{xtal}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_I	XIN/XOUT	–0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Soldering Temperature	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK}	T_P		20 to 40	sec

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
3. The device is compliant with JEDEC J-STD-020.

6. Pin Descriptions

6.1 Si53358A-D01AM Pin Descriptions (40-QFN)

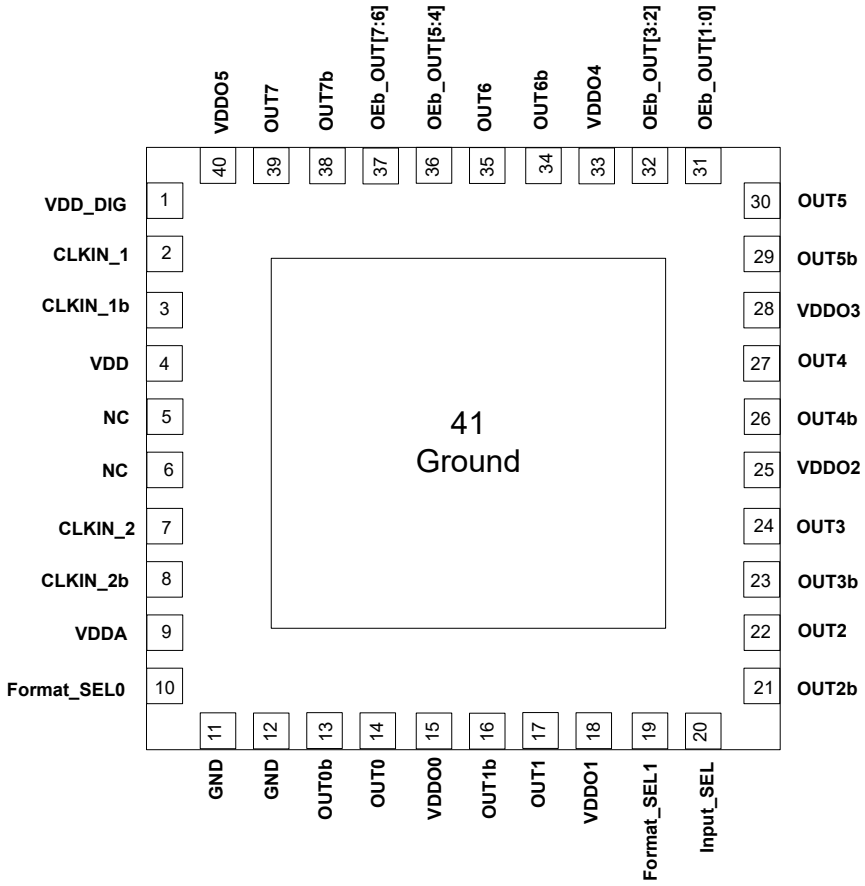


Figure 6.1. Si53358A-D01AM 40-QFN

Table 6.1. Si53358A-D01-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_1b	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
8	CLKIN_2b	I	
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
10	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 19. Reference Section 3.2 Output Signal Formats.
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
14	OUT0	O	
15	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 10. Reference Section 3.2 Output Signal Formats.

Pin Number	Pin Name	Pin Type	Function
20	Input_SEL	I	Input clock selection pin. 0 = CLKIN_1/CLKIN_1b 1 = CLKIN_2/CLKIN_2b
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
22	OUT2	O	
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
27	OUT4	O	
28	VDDO3	P	**Supply Voltage (1.8–3.3 V) for OUT4 and OUT5** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
30	OUT5	O	
31	OEb_OUT[1:0]	I	Output enable pin for OUT0 and OUT1. Default low. Low = output disabled High = output enabled
32	OEb_OUT[3:2]	I	Output enable pin for OUT2 and OUT3. Default low. Low = output disabled High = output enabled
33	VDDO4	P	**Supply Voltage (1.8–3.3 V) for OUT6** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
35	OUT6	O	

Pin Number	Pin Name	Pin Type	Function
36	OEb_OUT[5:4]	I	Output enable pin for OUT5 and OUT5. Default low. Low = output disabled High = output enabled
37	OEb_OUT[7:6]	I	Output enable pin for OUT6 and OUT7. Default low. Low = output disabled High = output enabled
38	OUT7b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
39	OUT7	O	
40	VDDO5	P	**Supply Voltage (1.8–3.3 V) for OUT7** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.2 Si53358BDxxxxx-AM Pin Descriptions (40-QFN)

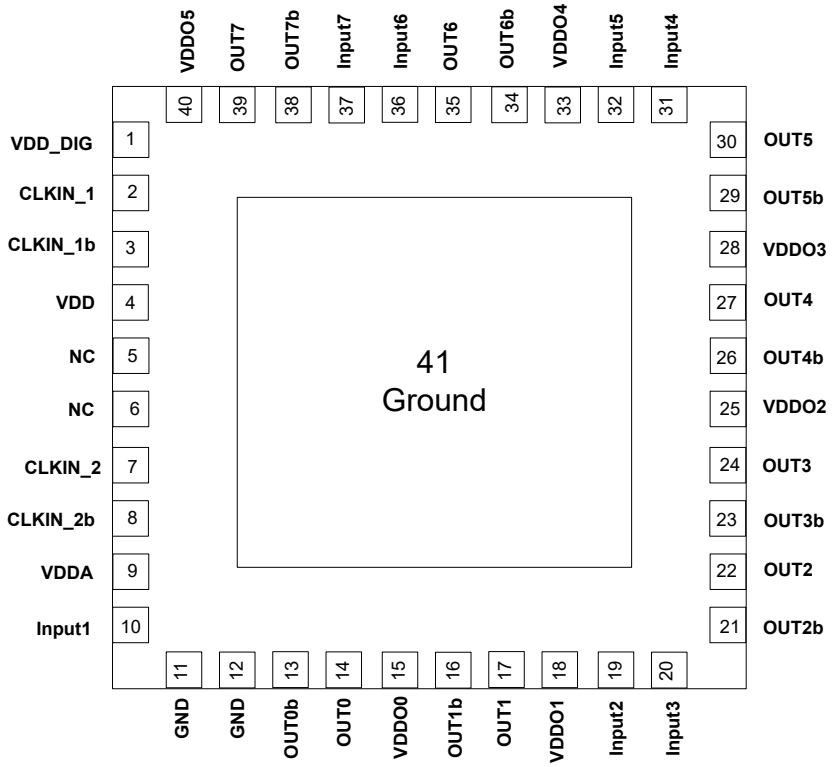


Figure 6.2. Si53358Bxxxxx-AM 40-QFN

Table 6.2. Si53358BDxxxxx-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_1b	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
8	CLKIN_2b	I	
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
10	Input1	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
14	OUT0	O	
15	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Input2	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for

Pin Number	Pin Name	Pin Type	Function
20	Input3	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
22	OUT2	O	
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
27	OUT4	O	
28	VDDO3	P	**Supply Voltage (1.8–3.3 V) for OUT4 and OUT5** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
30	OUT5	O	
31	Input4	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
32	Input5	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
33	VDDO4	P	**Supply Voltage (1.8–3.3 V) for OUT6** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
35	OUT6	O	
36	Input6	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
37	Input7	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for

Pin Number	Pin Name	Pin Type	Function
38	OUT7b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
39	OUT7	O	
40	VDDO5	P	**Supply Voltage (1.8–3.3 V) for OUT7** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.3 Si53354A-D01AM Pin Descriptions (40-QFN)

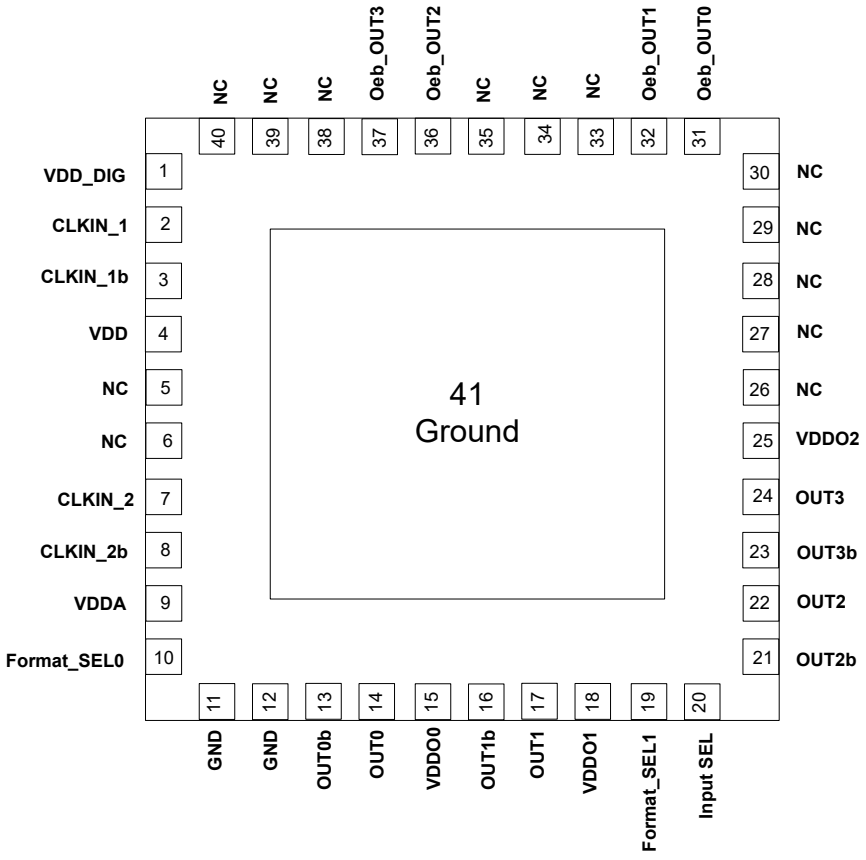


Figure 6.3. Si53354A-D01-AM 40-QFN

Table 6.3. Si53354A-D01AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_1b	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
8	CLKIN_2b	I	
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
10	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 19. Reference Section 3.2 Output Signal Formats.
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
14	OUT0	O	
15	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 10. Reference Section 3.2 Output Signal Formats.

Pin Number	Pin Name	Pin Type	Function
20	Input_SEL	I	Input clock selection pin. 0 = CLKIN_1/CLKIN_1b 1 = CLKIN_2/CLKIN_2b
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
22	OUT2	O	
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	NC	—	Do not connect these pins to anything.
27	NC	—	
28	NC	—	Do not connect these pins to anything.
29	NC	—	Do not connect these pins to anything.
30	NC	—	
31	OEb_OUT0	I	Output enable for OUT0 0 = output disabled 1 = output enabled
32	OEb_OUT1	I	Output enable for OUT1 0 = output disabled 1 = output enabled
33	NC	—	Do not connect these pins to anything.
34	NC	—	Do not connect these pins to anything.
35	NC	—	
36	OEb_OUT2	I	Output enable for OUT2 0 = output disabled 1 = output enabled
37	OEb_OUT3	I	Output enable for OUT3 0 = output disabled 1 = output enabled
38	NC	—	Do not connect these pins to anything.
39	NC	—	
40	NC	—	Do not connect these pins to anything.

Pin Number	Pin Name	Pin Type	Function
41	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.4 Si53354BDxxxxx-AM Pin Descriptions (40-QFN)

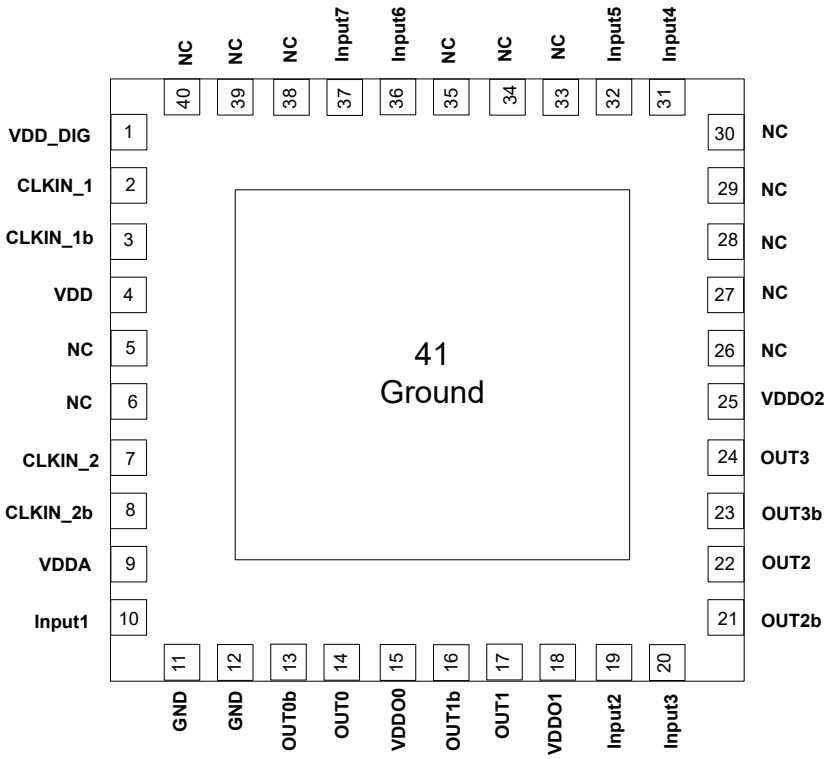


Figure 6.4. Si53354BDxxxxx-AM 40-QFN

Table 6.4. Si53354BDxxxxx-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_1b	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
8	CLKIN_2b	I	
9	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
10	Input1	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
14	OUT0	O	
15	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
17	OUT1	O	
18	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Input2	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for

Pin Number	Pin Name	Pin Type	Function
20	Input3	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
21	OUT2b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
22	OUT2	O	
23	OUT3b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
24	OUT3	O	
25	VDDO2	P	**Supply Voltage (1.8–3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	NC	—	Do not connect these pins to anything.
27	NC	—	
28	NC	—	
29	NC	—	
30	NC	—	
31	Input4	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
32	Input5	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
33	NC	—	Do not connect these pins to anything.
34	NC	—	
35	NC	—	
36	Input6	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
37	Input7	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
38	NC	—	Do not connect these pins to anything.
39	NC	—	
40	NC	—	
41	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.5 Si53352A-D01AM Pin Descriptions (32-QFN)

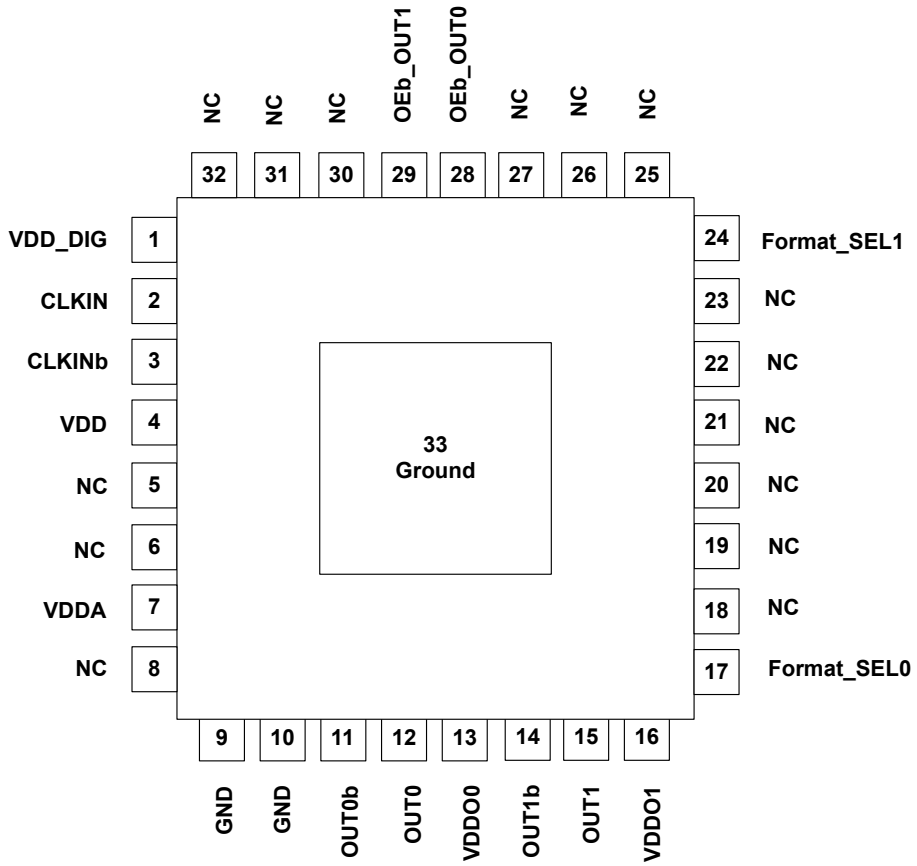


Figure 6.5. Si53352A-D01AM 32-QFN

Table 6.5. Si53352A-D01AM Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
2	CLKIN	I	Clock input. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKINb	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
8	GND	P	Connect these pins to ground.
9	GND	P	
10	NC	—	Do not connect this pin to anything.

Pin Number	Pin Name	Pin Type	Function
11	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
12	OUT0	O	
13	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
15	OUT1	O	
16	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 17. Reference Section 3.2 Output Signal Formats.
18	NC	—	Do not connect these pins to anything.
19	NC	—	
20	NC	—	
21	NC	—	
22	NC	—	
23	NC	—	
24	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 8. Reference Section 3.2 Output Signal Formats.
25	NC	—	Do not connect these pins to anything.
26	NC	—	
27	NC	—	
28	OEb_OUT0	I	Output enable for OUT0 0 = output disabled 1 = output enabled
29	OEb_OUT1	I	Output enable for OUT1 0 = output disabled 1 = output enabled
30	NC	—	Do not connect these pins to anything.
31	NC	—	
32	NC	—	
33	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.6 Si53352BDxxxxx-AM Pin Descriptions (32-QFN)

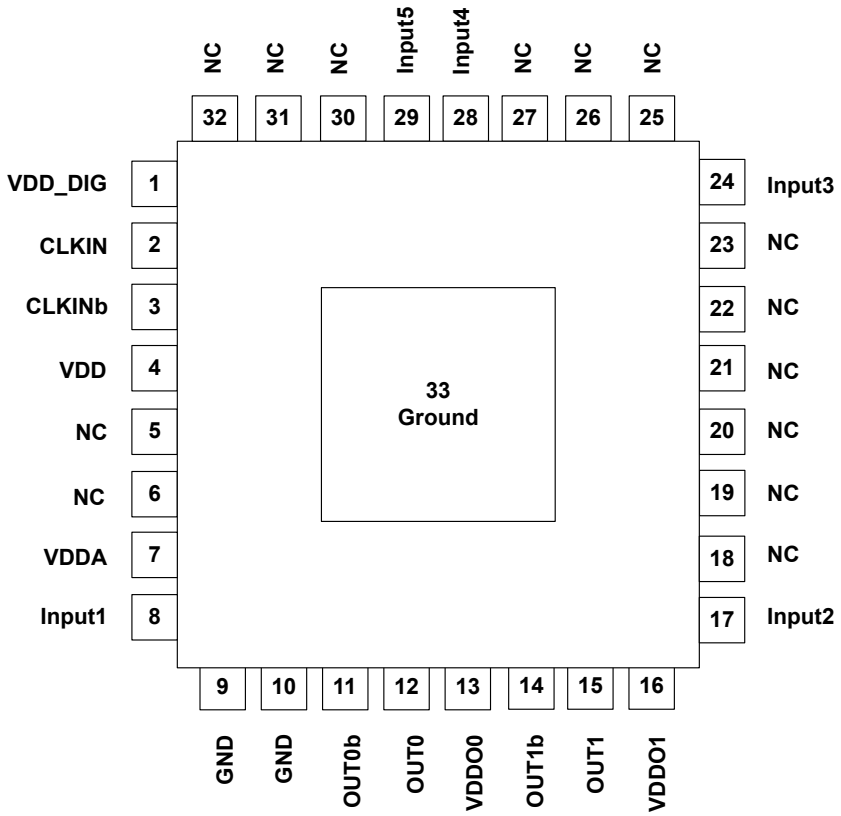


Figure 6.6. Si53352A-Dxxxxx-AM 32-QFN

Table 6.6. Si53352BDxxxxx-AM Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
2	CLKIN	I	Clock input. These pins accept both differential and single-ended clock signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKINb	I	
4	VDD	P	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
8	Input1	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for

Pin Number	Pin Name	Pin Type	Function
9	GND	P	Connect these pins to ground.
10	GND	P	
11	OUT0b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
12	OUT0	O	
13	VDDO0	P	**Supply Voltage (1.8–3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	O	**Output Clock** These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
15	OUT1	O	
16	VDDO1	P	**Supply Voltage (1.8–3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	Input2	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
18	NC	—	Do not connect these pins to anything.
19	NC	—	
20	NC	—	
21	NC	—	
22	NC	—	
23	NC	—	
24	Input3	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
25	NC	—	Do not connect these pins to anything.
26	NC	—	
27	NC	—	
28	Input4	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
29	Input5	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for
30	NC	—	Do not connect these pins to anything.
31	NC	—	
32	NC	—	

Pin Number	Pin Name	Pin Type	Function
33	Ground	GND	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

7. Package Outline

7.1 6x6 mm 40-QFN Package Diagram

The figure below illustrates the package details for 40-QFN. The table below lists the values for the dimensions shown in the illustration.

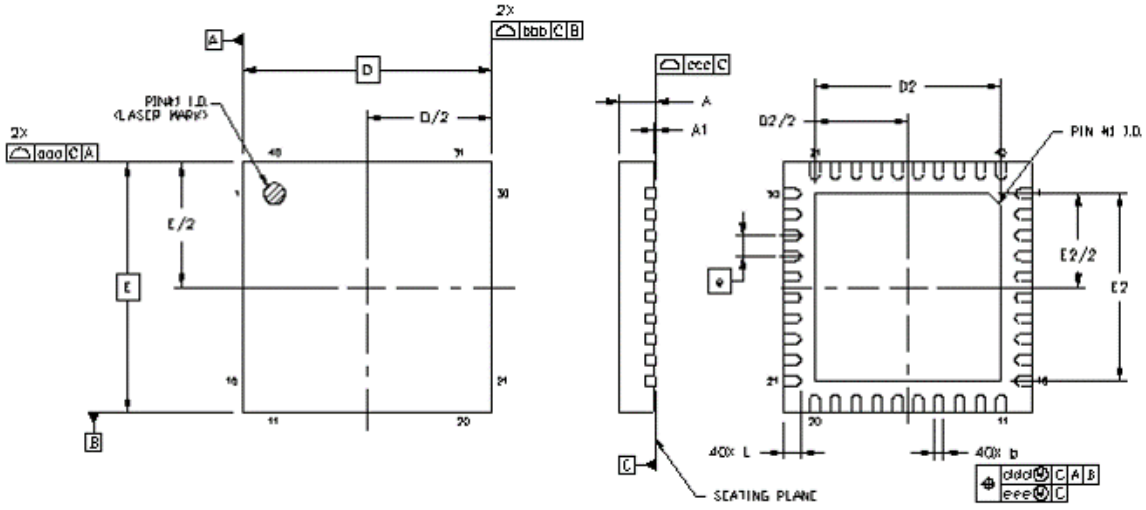


Figure 7.1. 40-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee			0.05

Dimension	Min	Nom	Max

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensions and Tolerances per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 5x5 mm 32-QFN Package Diagram

The figure below illustrates the package details for 32-QFN option. The table below lists the values for the dimensions shown in the illustration.

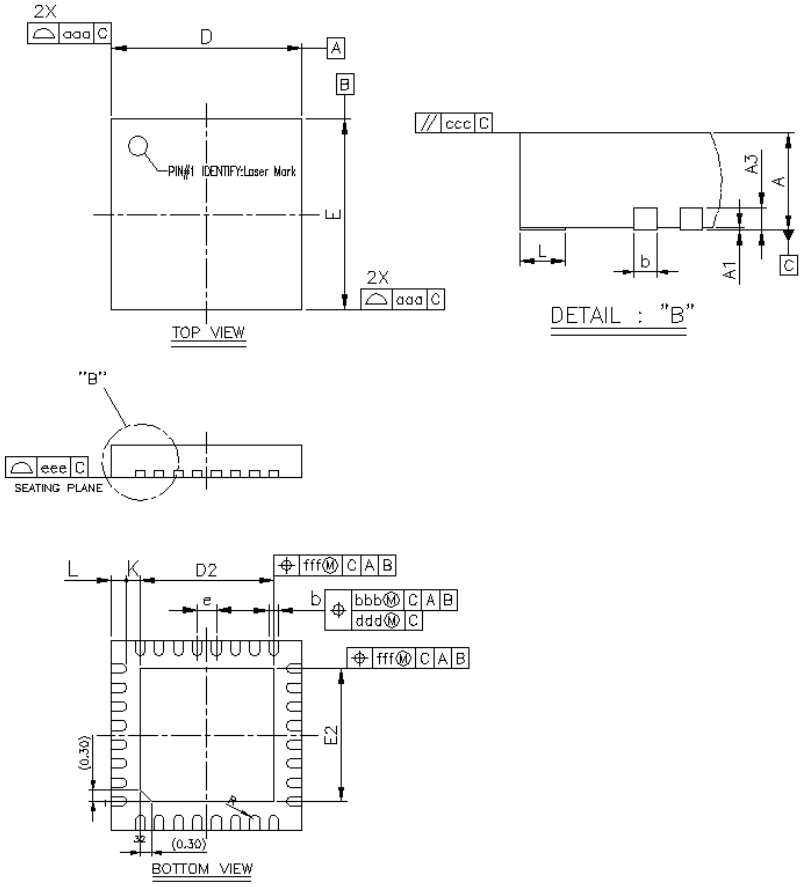


Figure 7.2. 32-Pin Quad Flat No-Lead (QFN)

Table 7.2. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	

Dimension	MIN	NOM	MAX
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensions and Tolerances per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1 40-QFN Land Pattern

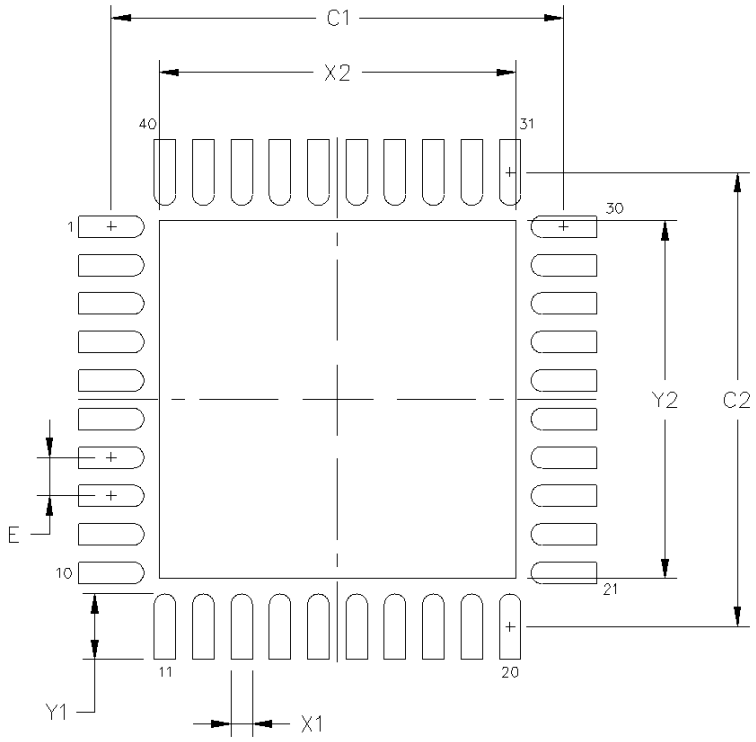


Figure 8.1. 40-QFN Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for 32-QFN package. The table below lists the values for the dimensions shown in the illustration.

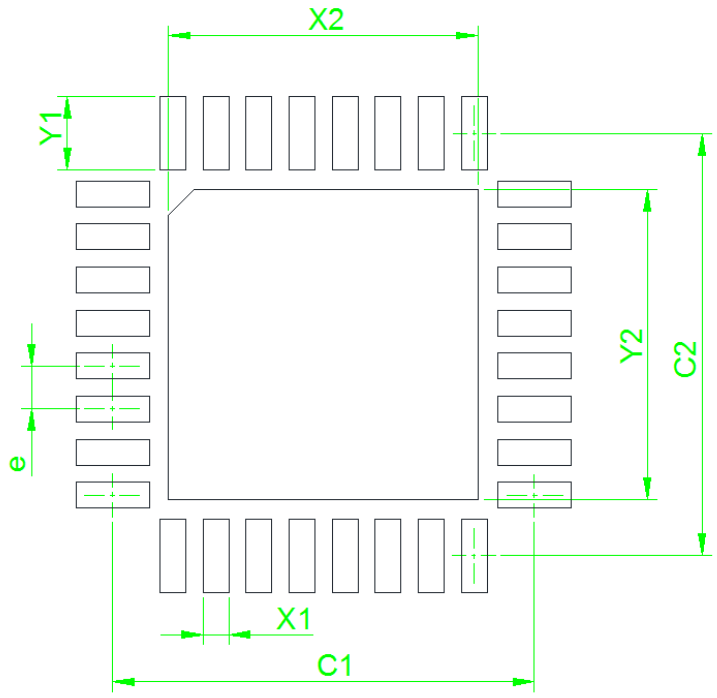


Figure 8.2. 32-QFN Land Pattern

Table 8.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

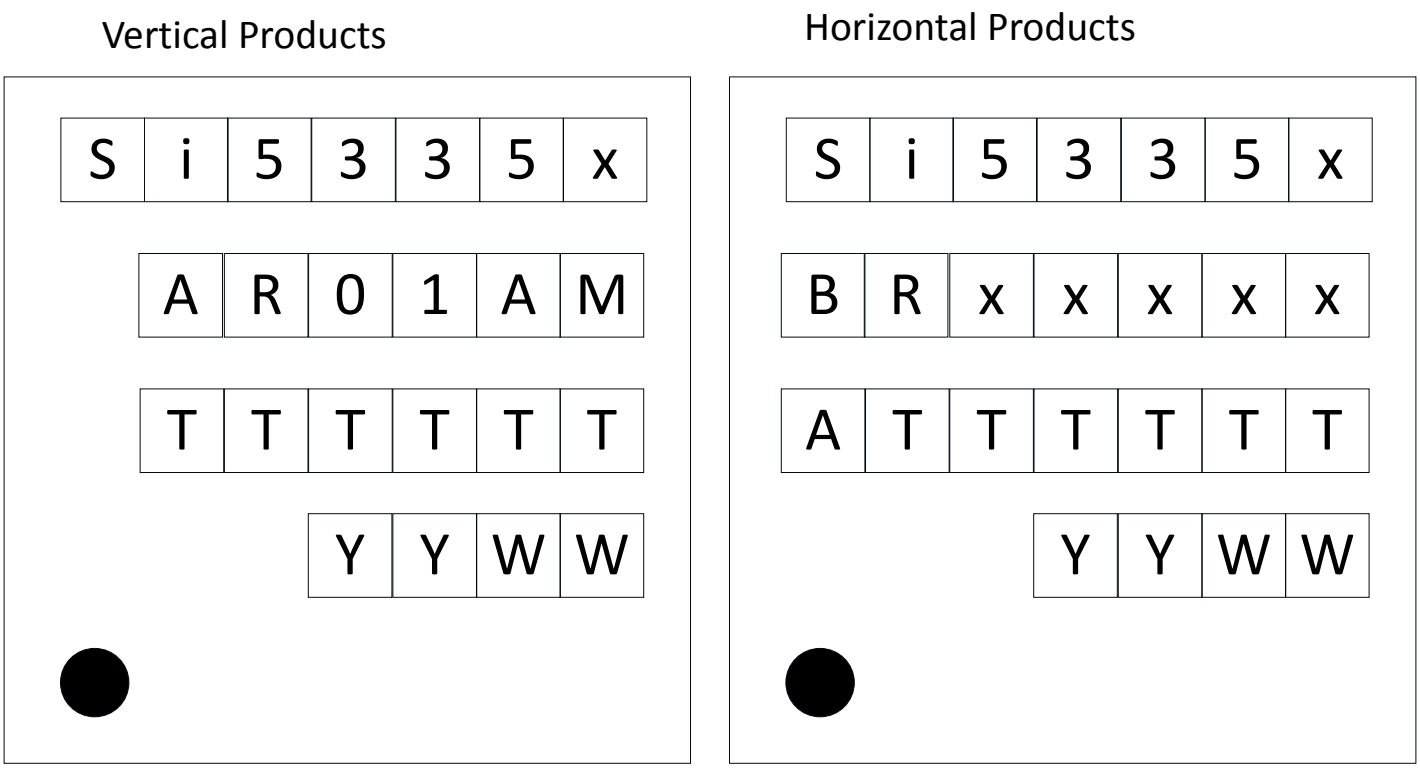


Figure 9.1. Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description
1	Si53358 Si53354 Si53352	Base part number
2	AR01AM	A = Product grade R = Product revision (see Ordering Guide for current revision) 01 = Device ID AM = Automotive temperature range (-40 °C to +105 °C) and Package (QFN)
	BDxxxxx	B = Product grade
		R = Product revision (see Ordering Guide for current revision)
		XXXXX = Customer specific NVM sequence number. NVM code assigned for custom, factory pre-programmed devices using ClockBuilder Pro.
3	TTTTTT	Manufacturing trace code
	ATTTTTT	AM = Automotive temperature range (-40 °C to +105 °C) and Package (QFN)
		TTTTTT = Manufacturing trace code
4	YYWW	Year (YY) and work week (WW) of package assembly

10. Document Change List

Revision 0.7

September, 2019

- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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