Si5391 数据表

超低抖动，12 路输出，任意频率，任意输出时钟发生器

该任意频率、任意输出 Si5391 时钟发生器结合宽带 PLL 和专有的 MultiSynth™ 分数频率合成器技术，提供了一个多功能且高性能的时钟发生器平台。这种高度灵活的架构能够在 12 个差分时钟输出上合成高达 1 GHz 的广泛的整数和非整数相关频率，同时提供针对 100G/200G/400G 应用优化的低于 100 fs rms 的相位抖动性能。每个时钟输出都可以分配自己的格式和输出电压，使 Si5391 能够用一个器件取代多个时钟 IC 和振荡器，使其成为真正的“片上时钟树”

可使用 ClockBuilder Pro 软件快速而方便地对 Si5391 进行配置。使用 ClockBuilder Pro™ 可自动分配自定义零件编号，以便快速、自由且轻松地进行工厂预编程，也可以通过 I2C 和 SPI 串行接口对 Si5391 进行编程。

应用：
• 100/200/400G 交换机
• 56G/112G PAM4 SerDes 参考时钟
• 时钟树代替 XO、缓冲区、信号格式转换器
• FPGA、处理器、内存时钟
• 以太网交换机/路由器
• OTN 成帧器/映射器/处理器

主要特点
• 从任何输入频率生成任何输出频率的组合
• 超低抖动性能
  • 69fs RMS（精密校准）
  • 75fs RMS（整数模式）
  • 115fs RMS（分数模式）
• 输入频率范围：
  • 外部晶体：25 MHz 至 54 MHz
  • 差分时钟：10 MHz 至 750 MHz
  • LVCMOS 时钟：10 MHz 至 250 MHz
• 输出频率范围：
  • 差分：100 Hz 至 1028 MHz
  • LVCMOS：100 Hz 至 250 MHz
• 高度可配置的输出，与 LVDS、LVPECL、LVCMOS、CML 和 HCSL 兼容，可编程信号幅度
• Si5391：4 路输入、12 路输出、64 QFN 9×9 mm
1. 功能列表

Si5391 功能如下所列:

- 从任何输入频率生成任何输出频率的组合
- 超低相位抖动性能
  - 69fs RMS（精密校准）
  - 75fs RMS（整数模式）
  - 115fs RMS（分数模式）
- 输入频率范围:
  - 外部晶体: 25 MHz 至 54 MHz
  - 差分时钟: 10 MHz 至 750 MHz
  - LVCMOS 时钟: 10 MHz 至 250 MHz
- 输出频率范围:
  - 差分: 100 Hz 至 1028 MHz
  - LVCMOS: 100 Hz 至 250 MHz
- 输入可配置的输出，与 LVDS、LVPECL、LVCMOS、CML 和 HCSL 兼容，可编程信号幅度
- 可选的零延迟模式
- 无毛刺的实时输出频率变化
- DCO 模式: 低至 0.001 ppb 步长
- 内核电压
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- 独立输出时钟供应引脚
  - 3.3 V、2.5 V 或 1.8 V
- 串行接口: I2C 或 SPI
- 在线可编程，具有非易失性 OTP 存储器
- ClockBuilder Pro 软件能够简化设备配置
- 64-QFN 9x9mm
- 温度范围: -40 至 +85 °C
- 无铅、符合 RoHS-6
## 2. Related Documents

<table>
<thead>
<tr>
<th>Document/Resource</th>
<th>Description/URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quality and Reliability</td>
<td><a href="http://www.silabs.com/quality">http://www.silabs.com/quality</a></td>
</tr>
</tbody>
</table>
### 3. Ordering Guide

#### Table 3.1. Si5391 Ordering Guide

<table>
<thead>
<tr>
<th>Ordering Part Number (OPN)</th>
<th>Number of Input/Output Clocks</th>
<th>Output clock frequency range (MHz)</th>
<th>Frequency Synthesis Mode</th>
<th>Package</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si5391A-A-GM(^{1, 2})</td>
<td>4/12</td>
<td>0.001 to 1028</td>
<td>Integer and Fractional</td>
<td>64-QFN 9x9mm</td>
<td>-40 to 85°C</td>
</tr>
<tr>
<td>Si5391B-A-GM(^{1, 2})</td>
<td></td>
<td>0.001 to 350</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si5391C-A-GM(^{1, 2})</td>
<td></td>
<td>0.001 to 1028</td>
<td>Integer Only</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si5391D-A-GM(^{1, 2})</td>
<td></td>
<td>0.001 to 350</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si5391P-A-EGM</td>
<td>Crystal / 12</td>
<td>312.5/156.25/100/50 /25</td>
<td>Precision Calibration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si5391A-A-EVB</td>
<td>4 / 12</td>
<td>Any-Frequency, Any Output</td>
<td>Integer and Fractional</td>
<td>Evaluation Board (A/B/C/D Grades)</td>
<td></td>
</tr>
<tr>
<td>Si5391P-A-EVB</td>
<td>Crystal /12</td>
<td>Ultra low jitter clocks for 56G/112G SerDes</td>
<td>Precision Calibration</td>
<td>Evaluation Board (P Grade)</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility. Custom part number format is: e.g., Si5391A-Axxxxx-GM, where "xxxxx" is a unique numerical sequence representing the preprogrammed configuration.

---

**Si5391g-Rxxxxx-GM**

- **Timing product family**
- \( f = \) Multi-PLL clock family member (7, 6)
- \( g = \) Device grade (A, B, C, D, P)
- **Product Revision (A)**
- Custom ordering part number (OPN) sequence ID**
- Package, ambient temperature range (QFN, -40 °C to +85°C)

*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

**Figure 3.1. Ordering Part Number Fields**
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4. Functional Description

The Si5391 combines a wide band PLL with next generation MultiSynth technology to offer the industry's most versatile and high-performance clock generator. The PLL locks to either an external **crystal** between XA/XB or to an external **clock** connected to XA/XB or IN0, 1, 2. A fractional or integer multiplier takes the selected input clock or crystal frequency up to a very high frequency that is then divided by the MultiSynth output stage to any frequency in the range of 100 Hz to 1 GHz on each output. The MultiSynth stage can divide by both integer and fractional values. The high-resolution fractional MultiSynth dividers enable true any-frequency input to any-frequency on any of the outputs. The output drivers offer flexible output formats which are independently configurable on each of the outputs. This clock generator is fully configurable via its serial interface (I²C/SPI) and includes in-circuit programmable non-volatile memory.

4.1 Power-up and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is done. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

![Si5391 Power-Up and Initialization](image)

4.2 Frequency Configuration

The phase-locked loop is fully contained and does not require external loop filter components to operate. Its function is to phase lock to the selected input and provide a common reference to the MultiSynth high-performance fractional dividers.

A crosspoint mux connects any of the MultiSynth divided frequencies to any of the outputs drivers. Additional output integer dividers provide further frequency division by an even integer from 2 to \((2^{25})-2\). The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (Mn/Md), the MultiSynth fractional dividers (Nn/Nd), and the output integer dividers (R). Silicon Labs's ClockBuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan.

4.3 Inputs

The Si5391 requires either an external crystal at its XA/XB pins or an external clock at XA/XB or IN0, 1, 2.
4.3.1 XA/XB Clock and Crystal Input

An internal crystal oscillator exists between pin XA and XB. When this oscillator is enabled, an external crystal connected across these pins will oscillate and provide a clock input to the PLL. A crystal frequency of 25 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for best jitter performance. The Si5391 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to Table 6.12 Crystal Specifications on page 30 for crystal specifications. Si5391P must use a 48 MHz crystal input.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. A clock (e.g., XO) may be used in lieu of the crystal, but it will result in higher output jitter. See the Si5391 Family Reference Manual for more information.

Selection between the external XTAL or input clock is controlled by register configuration. The internal crystal load capacitors (CL) are disabled in the input clock mode. Refer to Table 6.3 Input Clock Specifications on page 20 for the input clock requirements at XAXB. Both a single-ended or a differential input clock can be connected to the XA/XB pins as shown in the figure below. A P_XAXB divider is available to accommodate external clock frequencies higher than 54 MHz.

Figure 4.2. XAXB External Crystal and Clock Connections
4.3.2 Input Clocks (IN0, IN1, IN2)

A differential or single-ended clock can be applied at IN2, IN1, or IN0. The recommended input termination schemes are shown in the figure below. Input clock support is not available on Precision Calibration Si5391P.

![Figure 4.3. Termination of Differential and LVCMOS Input Signals](image-url)
4.3.3 Input Selection (IN0, IN1, IN2, XA/XB)

The active clock input is selected using the IN_SEL[1:0] pins or by register control. A register bit determines input selection as pin or register selectable. There are internal pull ups on the IN_SEL pins.

<table>
<thead>
<tr>
<th>IN_SEL[1:0]</th>
<th>Selected Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>IN0</td>
</tr>
<tr>
<td>0 1</td>
<td>IN1</td>
</tr>
<tr>
<td>1 0</td>
<td>IN2</td>
</tr>
<tr>
<td>1 1</td>
<td>XA/XB</td>
</tr>
</tbody>
</table>

4.4 Fault Monitoring

The Si5391 provides fault indicators which monitor loss of signal (LOS) of the inputs (IN0, IN1, IN2, XA/XB, FB_IN) and loss of lock (LOL) for the PLL as shown in the figure below.

![Figure 4.4. LOS and LOL Fault Monitors](image)

4.4.1 Status Indicators

The state of the status monitors are accessible by reading registers through the serial interface or with a dedicated pin (LOLb). Each of the status indicator register bits has a corresponding sticky bit in a separate register location. Once a status bit is asserted its corresponding sticky bit (_FLG) will remain asserted until cleared. Writing a logic zero to a sticky register bit clears its state.

4.4.2 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status registers. All status registers are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status registers.
4.5 Outputs

The Si5391 supports 12 differential output drivers which can be independently configured as differential or LVCMOS.

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

4.5.1 Grade A/B/C/D

The Si539x grades A/B/C/D can generate any output frequency in any format with best-in-class jitter. These devices are available as a preprogrammed option or can be written to the device via I2C. The input/output frequency plan determines whether the output divider operates in integer or fractional mode. In the fractional mode, the device can generate any output frequency or any format from any input frequency with best-in-class jitter. Some frequency plans allow the user to use an integer mode that delivers even lower jitter. See the family reference manual for more details.

4.5.2 Grade P

Some applications, including 56G/112G PAM4 SerDes, require even better RMS phase jitter performance. The Si5391P grade internally calibrates out linearity errors to deliver the world’s best jitter performance for applications focused on 312.5 MHz and 156.25 MHz frequencies. In addition to the primary 312.5/156.25 MHz frequencies, the device can also support 100 MHz, 50 MHz and 25 MHz outputs. The three conditions required for optimum performance Precision Calibration grade are:

1. An unused channel between the low-jitter 156.25/312.5 MHz clocks and secondary clocks (100/50/25 MHz)
2. CMOS clocks should not be used for the secondary clocks.
3. 48 MHz crystal input. Clock input is not supported on Precision Calibration grade.

A typical example is shown in the figure below. With this configuration, it is possible to deliver a best-in-class 69 fs of phase jitter on the 312.5 MHz and 156.25 MHz outputs.

![Figure 4.5. Si5391P, 56G SerDes Application](image-url)

4.5.3 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable and compatible with a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.
4.5.4 Differential Output Terminations

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in the figure below.

**DC Coupled LVDS**

**AC Coupled LVDS/LVPECL**

**AC Coupled HCSL**

**AC Coupled LVPECL/CML**

---

4.5.5 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential modes are programmable so that LVDS specifications can be met and for the best signal integrity with different supply voltages. When dc coupling the output driver it is essential that the receiver should have a relatively high common mode impedance so that the common mode current from the output driver is very small.

4.5.6 LVCMOS Output Terminations

LVCMOS outputs are typically dc-coupled, as shown in the figure below.

**DC Coupled LVCMOS**

---

Figure 4.6. Supported Differential Output Terminations

<table>
<thead>
<tr>
<th>VDDRx</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td>442 ohms</td>
<td>56.2 ohms</td>
</tr>
<tr>
<td>2.5 V</td>
<td>332 ohms</td>
<td>59 ohms</td>
</tr>
<tr>
<td>1.8 V</td>
<td>243 ohms</td>
<td>63.4 ohms</td>
</tr>
</tbody>
</table>

For $V_{CM} = 0.37$ V

Figure 4.7. LVCMOS Output Terminations
4.5.7 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance. It is highly recommended that the minimum output impedance (strongest drive setting) is selected and a suitable series resistor (Rs) is chosen to match the trace impedance.

<table>
<thead>
<tr>
<th>VDDO</th>
<th>CMOS_DRIVE_Selection</th>
<th>OUTx_CMOS_DRV=1</th>
<th>OUTx_CMOS_DRV=2</th>
<th>OUTx_CMOS_DRV=3</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td>38 Ω</td>
<td>30 Ω</td>
<td>22 Ω</td>
<td></td>
</tr>
<tr>
<td>2.5 V</td>
<td>43 Ω</td>
<td>35 Ω</td>
<td>24 Ω</td>
<td></td>
</tr>
<tr>
<td>1.8 V</td>
<td>—</td>
<td>46 Ω</td>
<td>31 Ω</td>
<td></td>
</tr>
</tbody>
</table>

Note: Refer to the Si5391 Family Reference Manual for more information on register settings.

4.5.8 LVCMOS Output Signal Swing

The signal swing (\(V_{OL}/V_{OH}\)) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

4.5.9 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with complementary polarity with the clock on the OUTx pin. The LVCMOS OUTx and OUTxb outputs can also be generated in phase.

4.5.10 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

4.5.11 Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low or disable high.

4.5.12 Synchronous/Asynchronous Output Disable Feature

Outputs can be configured to disable synchronously or asynchronously. The default state is synchronous output disable. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode the output clock will disable immediately without waiting for the period to complete.
4.5.13 Zero Delay Mode (Grade A/B/C/D)

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. It is recommended to connect OUT9A to FB_IN for external feedback. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance.

![Si5391 Zero Delay Mode Setup](image.png)

**Figure 4.8. Si5391 Zero Delay Mode Setup**

4.5.14 Output Crosspoint

The output crosspoint allows any of the N dividers to connect to any of the clock outputs.

4.5.15 Digitally Controlled Oscillator (DCO) Modes

Each MultiSynth can be digitally controlled so that all outputs connected to the MultiSynth change frequency in real time without any transition glitches. There are two ways to control the MultiSynth to accomplish this task:

- Use the Frequency Increment/Decrement Pins or register bits.
- Write directly to the numerator of the MultiSynth divider.

An output that is controlled as a DCO is useful for simple tasks such as frequency margining or CPU speed control. The output can also be used for more sophisticated tasks such as FIFO management by adjusting the frequency of the read or write clock to the FIFO or using the output as a variable Local Oscillator in a radio application.

4.5.15.1 DCO with Frequency Increment/Decrement Pins/Bits

Each of the MultiSynth fractional dividers can be independently stepped up or down in predefined steps with a resolution as low as 0.001 ppb. Setting of the step size and control of the frequency increment or decrement is accomplished by setting the step size with the 44 bit Frequency Step Word (FSTEPW). When the FINC or FDEC pin or register bit is asserted the output frequency will increment or decrement respectively by the amount specified in the FSTEPW.
4.5.15.2 DCO with Direct Register Writes

When a MultiSynth numerator and its corresponding update bit is written, the new numerator value will take effect and the output frequency will change without any glitches. The MultiSynth numerator and denominator terms can be left and right shifted so that the least significant bit of the numerator word represents the exact step resolution that is needed for your application.

4.6 Power Management

Several unused functions can be powered down to minimize power consumption. Consult the Si5391 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.7 In-Circuit Programming

The Si5391 is fully configurable using the serial interface (I²C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5391 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.8 Serial Interface

Configuration and operation of the Si5391 is controlled by reading and writing registers using the I²C or SPI interface. The I2C_SEL pin selects I²C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5391 Family Reference Manual for details.

4.9 Custom Factory Preprogrammed Devices

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed device will generate clocks at power-up. Use the ClockBuilder Pro custom part number wizard (www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your configuration. In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship to you typically within two weeks.

4.10 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-Programmed Devices

As with essentially all software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at http://www.silabs.com and opting in for updates to software, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Si5391 Family Reference Manual. However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is NOT yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. An example of this type of feature or custom setting is the customizable amplitudes for the clock outputs. After careful review of your project file and custom requirements, a Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled, using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown below:

<table>
<thead>
<tr>
<th>Location</th>
<th>Name</th>
<th>Type</th>
<th>Target</th>
<th>Dec Value</th>
<th>Hex Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0128[6:4]</td>
<td>OUT6_AMPL</td>
<td>User</td>
<td>OPN &amp; EVB</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Once you receive the updated design file, simply open it in CBPro. After you create a custom OPN, the device will begin operation after startup with the values in the NVM file, including the Silicon Labs-supplied override settings.
Do I need a pre-programmed device with a feature or setting which is unavailable in ClockBuilder Pro?

No → Configure device using CBPro

Yes → Contact Silicon Labs Technical Support to submit & review your non-standard configuration request & CBPro project file

Receive updated CBPro project file from Silicon Labs with “Settings Override” → Load project file into CBPro and test

Yes → Generate Custom OPN in CBPro

No → Does the updated CBPro Project file match your requirements?

Yes → End: Place sample order

Figure 4.9. Flowchart to Order Custom Parts with Features not Available in CBPro

Note: Contact Silicon Labs Technical Support at www.silabs.com/support/Pages/default.aspx.
5. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. Refer to the Si5391 Family Reference Manual for a complete list of register descriptions and settings.

Note: It is strongly recommended that ClockBuilder Pro be used to create and manage register settings.

5.1 Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address + 8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the ‘Set Page Address’ byte located at address 0x01 of each page.
# 6. Electrical Specifications

Table 6.1. Recommended Operating Conditions$^1$

(V$_{DD}$=1.8 V ± 5%, V$_{DDA}$=3.3 V ± 5%, T$_A$= –40 to 85°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature</td>
<td>T$_A$</td>
<td>–40</td>
<td>25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T$_{J\text{MAX}}$</td>
<td>—</td>
<td>—</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Core Supply Voltage</td>
<td>V$_{DD}$</td>
<td>1.71</td>
<td>1.80</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V$_{DDA}$</td>
<td>3.14</td>
<td>3.30</td>
<td>3.47</td>
<td>V</td>
</tr>
<tr>
<td>Output Driver Supply Voltage</td>
<td>V$_{DDO}$</td>
<td>3.14</td>
<td>3.30</td>
<td>3.47</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.37</td>
<td>2.50</td>
<td>2.62</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.71</td>
<td>1.80</td>
<td>1.89</td>
<td>V</td>
</tr>
</tbody>
</table>

Note:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
### Table 6.2. DC Characteristics

\((V_{DD}=1.8V \pm 5\%, V_{DDA}=3.3V \pm 5\%, V_{DDO}=1.8V \pm 5\%, 2.5V \pm 5\%, \text{ or } 3.3V \pm 5\%, T_A= -40 \text{ to } 85^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Supply Current(^1)</td>
<td>(I_{DD})</td>
<td>Si5391</td>
<td>—</td>
<td>115</td>
<td>230</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(I_{DDA})</td>
<td>Si5391</td>
<td>—</td>
<td>120</td>
<td>130</td>
<td>mA</td>
</tr>
<tr>
<td>Output Buffer Supply Current</td>
<td>(I_{DDOx})</td>
<td>LVPECL Output(^2)@ 156.25 MHz</td>
<td>—</td>
<td>22</td>
<td>26</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS Output(^2)@ 156.25 MHz</td>
<td>—</td>
<td>15</td>
<td>18</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V LVCMOS(^3) output@ 156.25 MHz</td>
<td>—</td>
<td>22</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5 V LVCMOS(^3) output@ 156.25 MHz</td>
<td>—</td>
<td>18</td>
<td>23</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8 V LVCMOS(^3) output@ 156.25 MHz</td>
<td>—</td>
<td>12</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td>Total Power Dissipation(^1, 4)</td>
<td>(P_d)</td>
<td>Si5391</td>
<td>—</td>
<td>880</td>
<td>1350</td>
<td>mW</td>
</tr>
</tbody>
</table>

**Note:**

1. Si5391 test configuration: 7 x 2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
2. Differential outputs terminated into an ac-coupled 100 \(\Omega\) load.
3. LVCMOS outputs measured into a 6-inch 50 \(\Omega\) PCB trace with 5 pF load. The LVCMOS outputs were set to \(\text{OUT}_x\text{.CMOS\\_DRV}=3\), which is the strongest driver setting. Refer to the [Si5391 Family Reference Manual](https://silabs.com) for more details on register settings.

#### Differential Output Test Configuration

![Differential Output Test Configuration](image)

#### LVCMOS Output Test Configuration

![LVCMOS Output Test Configuration](image)

4. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.
Table 6.3. Input Clock Specifications

\(V_{DD} = 1.8 \pm 5\%, \; V_{DDA} = 3.3 \pm 5\%, \; T_A = -40 \text{ to } 85 \; ^\circ C\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Input Buffer with Differential or Single-Ended - AC-Coupled (IN0/IN0b, IN1/IN1b, IN2/IN2b, FB_IN/FB_INb)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Frequency Range</td>
<td>(f_{IN})</td>
<td></td>
<td>Differential</td>
<td>10</td>
<td>—</td>
<td>750</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All Single-ended Signals</td>
<td>10</td>
<td>—</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(including LVCMOS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Swing</td>
<td>(V_{IN})</td>
<td>Differential AC-coupled</td>
<td>100</td>
<td>—</td>
<td>1800</td>
<td>mVpp_se</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(f_{IN} &lt; 250 ; MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential AC-coupled</td>
<td>225</td>
<td>—</td>
<td>1800</td>
<td>mVpp_se</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(250 ; MHz &lt; f_{IN} &lt; 750 ; MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single-ended AC-coupled</td>
<td>100</td>
<td>—</td>
<td>3600</td>
<td>mVpp_se</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(f_{IN} &lt; 250 ; MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>(SR)</td>
<td></td>
<td>400</td>
<td>—</td>
<td>—</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>(C_{IN})</td>
<td></td>
<td>—</td>
<td>0.3</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Input Resistance Differential</td>
<td>(R_{IN_DIFF})</td>
<td></td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>k\Omega</td>
</tr>
<tr>
<td>Input Resistance Single-Ended</td>
<td>(R_{IN_SE})</td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>k\Omega</td>
</tr>
<tr>
<td>Pulsed CMOS Input Buffer - DC Coupled (IN0, IN1, IN2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Frequency</td>
<td>(f_{IN})</td>
<td></td>
<td>10</td>
<td>—</td>
<td>250</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(V_{IL})</td>
<td></td>
<td>—0.2</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{IH})</td>
<td></td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>(SR)</td>
<td></td>
<td>400</td>
<td>—</td>
<td>—</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>Minimum Pulse Width</td>
<td>(PW)</td>
<td>Pulse Input</td>
<td>1.6</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>(R_{IN})</td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>k\Omega</td>
</tr>
<tr>
<td>REFCLK (Applied to XA/XB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Frequency Range</td>
<td>(f_{IN})</td>
<td>Full operating range. Jitter performance may be reduced.</td>
<td>10</td>
<td>—</td>
<td>200</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Range for best jitter.</td>
<td>48</td>
<td>—</td>
<td>54</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Single-ended Voltage Swing</td>
<td>(V_{IN_SE})</td>
<td></td>
<td>365</td>
<td>—</td>
<td>2000</td>
<td>mVpp_se</td>
</tr>
<tr>
<td>Input Differential Voltage Swing</td>
<td>(V_{IN_DIFF})</td>
<td></td>
<td>365</td>
<td>—</td>
<td>2500</td>
<td>mVpp_diff</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>(SR)</td>
<td>Imposed for best jitter performance</td>
<td>400</td>
<td>—</td>
<td>—</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>Input Duty Cycle</td>
<td>(DC)</td>
<td></td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
</tr>
</tbody>
</table>
### Table 6.4. Control Input Pin Specifications

\((V_{DD} = 1.8 \text{ V} \pm 5\%, V_{DDA} = 3.3 \text{ V} \pm 5\%, V_{DDS} = 3.3 \text{ V} \pm 5\%, 1.8 \text{ V} \pm 5\%, T_A = -40 \text{ to } 85 \text{ °C})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si5391 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, SYNCb, A1, SCLK, A0/CSb, FINC, FDEC, SDA/SDIO)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(V_{IL})</td>
<td>—</td>
<td>—</td>
<td>0.3x(V_{DDIO})(^1)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{IH})</td>
<td>—</td>
<td>—</td>
<td>0.7x(V_{DDIO})(^1)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>(C_{IN})</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>(R_{IN})</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Minimum Pulse Width</td>
<td>(T_{PW})</td>
<td>RSTb, SYNCh, FINC, and FDEC</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Frequency Update Rate</td>
<td>(F_{UR})</td>
<td>FINC and FDEC</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>MHz</td>
</tr>
</tbody>
</table>

### Note:
1. \(V_{DDIO}\) is determined by the IO_VDD_SEL bit. It is selectable as \(V_{DDA}\) or \(V_{DD}\). Refer to the Si5391 Family Reference Manual for more details on register settings.

---

1. Voltage swing is specified as single-ended mVpp.
2. Imposed for jitter performance.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds \((V_{IL}, V_{IH})\) of this buffer are non-standard (0.4 and 0.8 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the Si5391 Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard AC-Coupled, Single-ended input mode.
4. DC-coupled CMOS Input Buffer selection is not supported in ClockBuilder Pro for new designs. For single-ended LVCMOS inputs to IN0,1,2 it is required to ac-couple into the differential input buffer.
5. Clock input is not supported on Si5391P, Precision Calibration mode.
### Table 6.5. Differential Clock Output Specifications

\( \text{V}_{\text{DD}} = 1.8 \, \text{V} \pm 5\%, \text{V}_{\text{DDA}} = 3.3 \, \text{V} \pm 5\%, \text{V}_{\text{DDO}} = 1.8 \, \text{V} \pm 5\%, \text{V}_{\text{DDO}} = 2.5 \, \text{V} \pm 5\%, \text{or} \, 3.3 \, \text{V} \pm 5\%, \text{T}_{\text{A}} = -40 \text{ to } 85 \, ^\circ \text{C} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Frequency</td>
<td>( \text{f}_{\text{OUT}} )</td>
<td>MultiSynth not used</td>
<td>0.0001</td>
<td>—</td>
<td>720</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>733.33</td>
<td>—</td>
<td>800.00</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>825</td>
<td>—</td>
<td>1028</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>MultiSynth used</td>
<td>0.0001</td>
<td>—</td>
<td>720</td>
<td>MHz</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>( \text{DC} )</td>
<td>( \text{f}_{\text{OUT}} &lt; 400 , \text{MHz} )</td>
<td>48</td>
<td>—</td>
<td>52</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 400 , \text{MHz} &lt; \text{f}_{\text{OUT}} &lt; 1028 , \text{MHz} )</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Output-Output Skew</td>
<td>( \text{T}_{\text{SKS}} )</td>
<td>Outputs on same MultiSynth (Measured at 712.5 MHz)</td>
<td>—</td>
<td>—</td>
<td>75</td>
<td>ps</td>
</tr>
<tr>
<td>Using Same MultiSynth</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT-OUT( \text{b} ) Skew</td>
<td>( \text{T}_{\text{SK_OUT}} )</td>
<td>Measured from the positive to negative output pins</td>
<td>—</td>
<td>0</td>
<td>50</td>
<td>ps</td>
</tr>
<tr>
<td>Output Voltage Swing(^1)</td>
<td>( \text{V}_{\text{OUT}} )</td>
<td>LVDS</td>
<td>350</td>
<td>430</td>
<td>510</td>
<td>mV\text{pp}_\text{se}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL</td>
<td>640</td>
<td>750</td>
<td>900</td>
<td></td>
</tr>
<tr>
<td>Common Mode Voltage(^1)</td>
<td>( \text{V}_{\text{CM}} )</td>
<td>( \text{V}_{\text{DDO}} = 3.3 , \text{V} )</td>
<td>LVDS</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVPECL</td>
<td>1.9</td>
<td>2.0</td>
<td>2.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{V}_{\text{DDO}} = 2.5 , \text{V} )</td>
<td>LVPECL</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{V}_{\text{DDO}} = 1.8 , \text{V} )</td>
<td>Sub-LVDS</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
</tr>
<tr>
<td>Rise and Fall Times</td>
<td>( \text{t}_{\text{R/F}} )</td>
<td>(20% to 80%)</td>
<td>—</td>
<td>100</td>
<td>150</td>
<td>ps</td>
</tr>
<tr>
<td>Differential Output Impedance</td>
<td>( \text{Z}_{\text{O}} )</td>
<td></td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td>Power Supply Noise Rejection(^2)</td>
<td>( \text{PSRR} )</td>
<td>10 kHz sinusoidal noise</td>
<td>—</td>
<td>—101</td>
<td>—</td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 kHz sinusoidal noise</td>
<td>—</td>
<td>—96</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 kHz sinusoidal noise</td>
<td>—</td>
<td>—99</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz sinusoidal noise</td>
<td>—</td>
<td>—97</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Output-Output Crosstalk(^3)</td>
<td>( \text{XTALK} )</td>
<td>Si5391</td>
<td>—</td>
<td>—72</td>
<td>—</td>
<td>dBc</td>
</tr>
</tbody>
</table>

**Notes:**

1. Output amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5391 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.

2. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.

3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz.
Table 6.6. LVCMOS Clock Output Specifications

(V<sub>DD</sub> = 1.8 V ± 5%, V<sub>DDA</sub> = 3.3 V ± 5%, V<sub>DDO</sub> = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T<sub>A</sub> = –40 to 85 °C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Frequency</td>
<td></td>
<td></td>
<td>0.0001</td>
<td>—</td>
<td>250</td>
<td>MHz</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>DC</td>
<td>f&lt;sub&gt;OUT&lt;/sub&gt; &lt; 100 MHz</td>
<td>48</td>
<td>—</td>
<td>52</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 MHz &lt; f&lt;sub&gt;OUT&lt;/sub&gt; &lt; 250 MHz</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Output Voltage High&lt;sup&gt;1, 2, 3&lt;/sup&gt;</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=1</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -10 mA</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.85</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -12 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -17 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 2.5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=1</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -6 mA</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.85</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -8 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -11 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -4 mA</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.85</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -5 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Output Voltage Low&lt;sup&gt;1, 2, 3&lt;/sup&gt;</td>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=1</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 10 mA</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 12 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 17 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 2.5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=1</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 6 mA</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 8 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 11 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=2</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 4 mA</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; x 0.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT&lt;sub&gt;X&lt;/sub&gt; CMOS_DRV=3</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 5 mA</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS Rise and Fall Times&lt;sup&gt;3&lt;/sup&gt;</td>
<td>tr/tf</td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 3.3V</td>
<td>—</td>
<td>400</td>
<td>600</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 2.5 V</td>
<td>—</td>
<td>450</td>
<td>600</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDO&lt;/sub&gt; = 1.8 V</td>
<td>—</td>
<td>550</td>
<td>750</td>
<td>ps</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Units</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-------</td>
</tr>
</tbody>
</table>

**Notes:**
1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the [Si5391 Family Reference Manual](#) for more details on register settings.
2. \( I_{OL}/I_{OH} \) is measured at \( V_{OL}/V_{OH} \) as shown in the dc test configuration.
3. A series termination resistor (\( R_s \)) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

**AC Test Configuration**

![AC Test Configuration Diagram]

**DC Test Configuration**

![DC Test Configuration Diagram]
Table 6.7. Output Status Pin Specifications

\((V_{DD} = 1.8 \pm 5\%, V_{DDA} = 3.3 \pm 5\%, V_{DDS} = 3.3 \pm 5\%, 1.8 \pm 5\%, T_A = –40 \text{ to } 85^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Si5391 Status Output Pins (INTRb, SDA/SDIO)(^1)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>(V_{OH})</td>
<td>(I_{OH} = -2) mA</td>
<td>(V_{DDIO}^2 \times 0.85)</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{OL})</td>
<td>(I_{OL} = 2) mA</td>
<td>—</td>
<td>—</td>
<td>(V_{DDIO}^2 \times 0.15)</td>
<td>V</td>
</tr>
<tr>
<td><strong>Si5391 Status Output Pins (LOLb)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>(V_{OH})</td>
<td>(I_{OH} = -2) mA</td>
<td>(V_{DDIO}^2 \times 0.85)</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{OL})</td>
<td>(I_{OL} = 2) mA</td>
<td>—</td>
<td>—</td>
<td>(V_{DDIO}^2 \times 0.15)</td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes:**
1. The \(V_{OH}\) specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high. \(V_{OL}\) remains valid in all cases.
2. \(V_{DDIO}\) is determined by the IO\_VDD\_SEL bit. It is selectable as \(V_{DDA}\) or \(V_{DD}\). Refer to the Si5391 Family Reference Manual for more details on register settings.

Table 6.8. Performance Characteristics

\((V_{DD} = 1.8 \pm 5\%, V_{DDA} = 3.3 \pm 5\%, T_A = –40 \text{ to } 85^\circ C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL Loop Bandwidth</td>
<td>(f_{BW})</td>
<td></td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td>Initial Start-Up Time</td>
<td>(t_{START})</td>
<td>Time from power-up to when the device generates clocks (Input Frequency &gt;48 MHz)</td>
<td>—</td>
<td>30</td>
<td>45</td>
<td>ms</td>
</tr>
<tr>
<td>PLL Lock Time(^1)</td>
<td>(t_{ACQ})</td>
<td>(f_{IN} = 19.44) MHz</td>
<td>15</td>
<td>—</td>
<td>150</td>
<td>ms</td>
</tr>
<tr>
<td>POR(^2) to Serial Interface Ready</td>
<td>(t_{RDY})</td>
<td></td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td>RMS Phase Jitter(^5) (Grade P)</td>
<td>(J_{GEN})</td>
<td>(f_{IN} = 48) MHz crystal</td>
<td>(f_{OUT} = 156.25) MHz</td>
<td>69</td>
<td>90</td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(f_{OUT} = 312.5) MHz</td>
<td>69</td>
<td>95</td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(f_{OUT} = 100) MHz</td>
<td>150</td>
<td>200</td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(f_{OUT} = 50/25) MHz</td>
<td>200</td>
<td>300</td>
<td>fs</td>
</tr>
<tr>
<td>RMS Phase Jitter(^6) (Grade A/B/C/D)</td>
<td>(J_{GEN})</td>
<td>(f_{IN} = 48) MHz crystal</td>
<td>Output divider Integer Mode(^3)</td>
<td>75</td>
<td>115</td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output divider Fractional Mode(^4)</td>
<td>115</td>
<td>145</td>
<td>fs</td>
</tr>
<tr>
<td>RMS Phase Jitter(^6) (Grade A/B/C/D)</td>
<td>(J_{GEN})</td>
<td>(f_{IN} = 100) MHz clock</td>
<td>Output divider Integer Mode(^3)</td>
<td>145</td>
<td>195</td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output divider Fractional Mode(^4)</td>
<td>165</td>
<td>215</td>
<td>fs</td>
</tr>
</tbody>
</table>
### Notes:

1. PLL lock time is measured by first letting the PLL lock, then turning off the input clock, and then turning on the input clock. The time from the first edge of the input clock being re-applied until LOL de-asserts is the PLL lock time.

2. Measured as time from valid VDD and VDD33 rails (90% of their value) to when the serial interface is ready to respond to commands. Measured in SPI 4-wire mode, with SCLK @ 10 MHz.

3. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.

4. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.

5. Grade P is calibrated for optimum performance in 56G/112G SerDes applications at frequencies of 312.5MHz or 156.25MHz. All outputs are assumed to be LVPECL, and an unused output is required between the 312.5/156.25MHz and 100/50/25MHz outputs. For more details refer to 4.5.2 Grade P

6. Grade A/B/C/D are targeted for applications that require more flexibility and set the output divider to Integer or Fractional modes. Integer mode test conditions: fin = 100MHz, fout = 156.25MHz (Multisynth in integer mode). Fractional mode test conditions: fin = 100MHz, fout = 156.25MHz (Multisynth in fractional mode). Outputs are assumed to be LVPECL. For more details, refer to 4.5.1 Grade A/B/C/D.

---

### Table 6.9. \( I^2C \) Timing Specifications (SCL,SDA)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Standard Mode 100 kbps</th>
<th>Fast Mode 400 kbps</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>SCL Clock Frequency</td>
<td>( f_{SCL} )</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Hold Time (Repeated) START Condition</td>
<td>( t_{HD:STA} )</td>
<td></td>
<td>4.0</td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td>Low Period of the SCL Clock</td>
<td>( t_{LOW} )</td>
<td></td>
<td>4.7</td>
<td></td>
<td>1.3</td>
</tr>
<tr>
<td>HIGH Period of the SCL Clock</td>
<td>( t_{HIGH} )</td>
<td></td>
<td>4.0</td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td>Set-up Time for a Repeated START Condition</td>
<td>( t_{SU:STA} )</td>
<td></td>
<td>4.7</td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>( t_{HD:DAT} )</td>
<td></td>
<td>100</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>Data Set-up Time</td>
<td>( t_{SU:DAT} )</td>
<td></td>
<td>250</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>Rise Time of Both SDA and SCL Signals</td>
<td>( t_r )</td>
<td></td>
<td></td>
<td>1000</td>
<td>20</td>
</tr>
<tr>
<td>Fall Time of Both SDA and SCL Signals</td>
<td>( t_f )</td>
<td></td>
<td></td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>Set-up Time for STOP Condition</td>
<td>( t_{SU:STO} )</td>
<td></td>
<td>4.0</td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td>Bus Free Time between a STOP and START Condition</td>
<td>( t_{BUF} )</td>
<td></td>
<td>4.7</td>
<td></td>
<td>1.3</td>
</tr>
<tr>
<td>Data Valid Time</td>
<td>( t_{VD:DAT} )</td>
<td></td>
<td></td>
<td>3.45</td>
<td></td>
</tr>
<tr>
<td>Data Valid Acknowledge Time</td>
<td>( t_{VD:ACK} )</td>
<td></td>
<td></td>
<td>3.45</td>
<td></td>
</tr>
</tbody>
</table>
Figure 6.1. $\text{i}^2\text{C}$ Serial Port Timing Standard and Fast Modes
Table 6.10. SPI Timing Specifications (4-Wire)

(V\textsubscript{DD}=1.8 V ± 5%, V\textsubscript{DDA}=3.3 V ± 5%, T\textsubscript{A}= -40 to 85 °C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK Frequency</td>
<td>f\textsubscript{SPI}</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>SCLK Duty Cycle</td>
<td>T\textsubscript{DC}</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>SCLK Period</td>
<td>T\textsubscript{C}</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, SCLK Fall to SDO Active</td>
<td>T\textsubscript{D1}</td>
<td>—</td>
<td>—</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, SCLK Fall to SDO</td>
<td>T\textsubscript{D2}</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, CSb Rise to SDO Tri-State</td>
<td>T\textsubscript{D3}</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time, CSb to SCLK</td>
<td>T\textsubscript{SU1}</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time, CSb to SCLK Rise</td>
<td>T\textsubscript{H1}</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time, SDI to SCLK Rise</td>
<td>T\textsubscript{SU2}</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time, SDI to SCLK Rise</td>
<td>T\textsubscript{H2}</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time Between Chip Selects (CSb)</td>
<td>T\textsubscript{CS}</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>T\textsubscript{C}</td>
</tr>
</tbody>
</table>

Figure 6.2. 4-Wire SPI Serial Interface Timing
Table 6.11. SPI Timing Specifications (3-Wire)

\((V_{DD}=1.8 \text{ V } \pm 5\%, V_{DDA}=3.3 \text{ V } \pm 5\%, T_A= -40 \text{ to } 85 \degree C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK Frequency</td>
<td>(f_{SPI})</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>SCLK Duty Cycle</td>
<td>(T_{DC})</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>SCLK Period</td>
<td>(T_C)</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, SCLK Fall to SDO Turn-on</td>
<td>(T_{D1})</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, SCLK Fall to SDO Next-bit</td>
<td>(T_{D2})</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time, CSb Rise to SDO Tri-State</td>
<td>(T_{D3})</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time, CSb to SCLK</td>
<td>(T_{SU1})</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time, CSb to SCLK Rise</td>
<td>(T_{H1})</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time, SDI to SCLK Rise</td>
<td>(T_{SU2})</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time, SDI to SCLK Rise</td>
<td>(T_{H2})</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Delay Time Between Chip Selects (CSb)</td>
<td>(T_{CS})</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>(T_C)</td>
</tr>
</tbody>
</table>

Figure 6.3. 3-Wire SPI Serial Interface Timing
### Table 6.12. Crystal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal Frequency Range</td>
<td>f&lt;sub&gt;XTAL&lt;/sub&gt;</td>
<td>Full operating range. Jitter performance may be reduced.</td>
<td>24.97</td>
<td>—</td>
<td>54.06</td>
<td>MHz</td>
</tr>
<tr>
<td>Si5391P requires 48 MHz XTAL</td>
<td></td>
<td>Range for best jitter.</td>
<td>48</td>
<td>—</td>
<td>54</td>
<td>MHz</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>C&lt;sub&gt;L&lt;/sub&gt;</td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Crystal Drive Level</td>
<td>d&lt;sub&gt;L&lt;/sub&gt;</td>
<td></td>
<td>—</td>
<td>—</td>
<td>200</td>
<td>μW</td>
</tr>
<tr>
<td>Equivalent Series Resistance</td>
<td>r&lt;sub&gt;ESR&lt;/sub&gt;</td>
<td>Refer to the Si5391 Family Reference Manual to determine ESR and shunt capacitance.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td>C&lt;sub&gt;O&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. Refer to the Si534x/8x Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 48 to 54 MHz crystals. The Si5391 is designed to work with crystals that meet these specifications.

### Table 6.13. Thermal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si5391 - 64QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>θ&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>Still Air</td>
<td>22</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Ambient</td>
<td></td>
<td>Air Flow 1 m/s</td>
<td>19.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Air Flow 2 m/s</td>
<td>18.3</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>θ&lt;sub&gt;JC&lt;/sub&gt;</td>
<td></td>
<td>9.5</td>
<td></td>
</tr>
<tr>
<td>Junction to Case</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>θ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td></td>
<td>9.4</td>
<td></td>
</tr>
<tr>
<td>Junction to Board</td>
<td>ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td></td>
<td>9.3</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td></td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>Junction to Top Center</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. Based on PCB Dimension: 3 x 4.5 mm, PCB Land/Via under GND pad: 36, Number of Cu Layers: 4
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{STG}$</td>
<td></td>
<td>-55 to +150°C</td>
<td>°C</td>
</tr>
<tr>
<td>DC Supply Voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>-0.5 to 3.8 V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{DDA}$</td>
<td></td>
<td>-0.5 to 3.8 V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{DDO}$</td>
<td></td>
<td>-0.5 to 3.8 V</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$V_{I1}$</td>
<td>IN0-IN2, FB_IN</td>
<td>-1.0 to 3.8 V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{I2}$</td>
<td>IN_SEL[1:0], RSTb, OEb, SYNCb, I2C_SEL, SDI, SCLK, A0/CSb, A1, SDA/SDIO, FINC/FDEC</td>
<td>-0.5 to 3.8 V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{I3}$</td>
<td>XA/XB</td>
<td>-0.5 to 2.7 V</td>
<td>V</td>
</tr>
<tr>
<td>Latch-up Tolerance</td>
<td>$LU$</td>
<td></td>
<td>JESD78 Compliant</td>
<td></td>
</tr>
<tr>
<td>ESD Tolerance</td>
<td>$HBM$</td>
<td>100 pF, 1.5 kΩ</td>
<td>2.0</td>
<td>kV</td>
</tr>
<tr>
<td>Maximum Junction Temperature in Operation</td>
<td>$T_{JCT}$</td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Soldering Temperature (Pb-free profile)&lt;sup&gt;3&lt;/sup&gt;</td>
<td>$T_{PEAK}$</td>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Soldering Temperature Time at $T_{PEAK}$ (Pb-free profile)&lt;sup&gt;3&lt;/sup&gt;</td>
<td>$T_P$</td>
<td></td>
<td>20 to 40 sec</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN packages are RoHS-6 compliant.
3. The device is compliant with JEDEC J-STD-020.
Figure 7.1. Si5391 Block Diagram
8. Typical Operating Characteristics

Figure 8.1. 156.25MHz Output (3.3V LVPECL) in Precision Calibration Mode (Grade P)
9. Pin Descriptions

Si 5391 64QFN
Top View

GND Pad
### Table 9.1. Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Si5391</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Inputs</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XA</td>
<td>8</td>
<td>I</td>
<td><strong>Crystal and External Clock Input.</strong> These pins are used to connect an external crystal or an external clock. See 4.3.1 XA/XB Clock and Crystal Input and Figure 4.2 XAXB External Crystal and Clock Connections on page 8 for connection information. If IN_SEL[1:0] = 11b, then the XAXB input is selected. If the XAXB input is not used and powered down, then both inputs can be left unconnected. ClockBuilder Pro will power down an input that is set as &quot;Unused&quot;.</td>
</tr>
<tr>
<td>XB</td>
<td>9</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>X1</td>
<td>7</td>
<td>I</td>
<td><strong>XTAL Shield.</strong> Connect these pins directly to the XTAL ground pins. X1, X2, and the XTAL ground pins must not be connected to the PCB ground plane. DO NOT GROUND THE CRYSTAL GROUND PINS. Refer to the Si5391 Family Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock.</td>
</tr>
<tr>
<td>X2</td>
<td>10</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>IN0</td>
<td>63</td>
<td>I</td>
<td><strong>Clock Inputs.</strong> These pins accept both differential and single-ended clock signals. Refer 4.3.2 Input Clocks (IN0, IN1, IN2) for input termination options. These pins are high-impedance and must be terminated externally. If both the INx and INxb inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as &quot;Unused&quot;.</td>
</tr>
<tr>
<td>IN0b</td>
<td>64</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>IN1</td>
<td>1</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>IN1b</td>
<td>2</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>IN2</td>
<td>14</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>IN2b</td>
<td>15</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>FB_IN</td>
<td>61</td>
<td>I</td>
<td><strong>External Feedback Input.</strong> These pins are used as the external feedback input (FB_IN/FB_Inb) for the optional zero delay mode. See 4.5.13 Zero Delay Mode (Grade A/B/C/D) for details on the optional zero delay mode. If FB_IN and FB_Inb are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as &quot;Unused&quot;.</td>
</tr>
<tr>
<td>FB_Inb</td>
<td>62</td>
<td>I</td>
<td></td>
</tr>
</tbody>
</table>
### Pin Descriptions

#### Outputs

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT0</td>
<td>24</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT0b</td>
<td>23</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT0A</td>
<td>21</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT0Ab</td>
<td>20</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT1</td>
<td>28</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT1b</td>
<td>27</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT2</td>
<td>31</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT2b</td>
<td>30</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT3</td>
<td>35</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT3b</td>
<td>34</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT4</td>
<td>38</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT4b</td>
<td>37</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT5</td>
<td>42</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT5b</td>
<td>41</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT6</td>
<td>45</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT6b</td>
<td>44</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT7</td>
<td>51</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT7b</td>
<td>50</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT8</td>
<td>54</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT8b</td>
<td>53</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT9</td>
<td>56</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT9b</td>
<td>55</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT9A</td>
<td>59</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>OUT9Ab</td>
<td>58</td>
<td>O</td>
<td></td>
</tr>
</tbody>
</table>

**Output Clocks.** These output clocks support a programmable signal amplitude when configured as a differential output. Desired output signal format is configurable using register control. Termination recommendations are provided in 4.5.4 Differential Output Terminations and 4.5.6 LVCMOS Output Terminations. Unused outputs should be left unconnected.

#### Serial Interface

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_SEL</td>
<td>39</td>
<td>I</td>
<td>I²C Select.² This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit.</td>
</tr>
<tr>
<td>SDA/SDIO</td>
<td>18</td>
<td>I/O</td>
<td>Serial Data Interface.² This is the bidirectional data pin (SDA) for the I²C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.</td>
</tr>
<tr>
<td>A1/SDO</td>
<td>17</td>
<td>I/O</td>
<td>Address Select 1/Serial Data Output.² In I²C mode, this pin functions as the A1 address input pin and does not have an internal pull up or pull down resistor. In 4-wire SPI mode this is the serial data output (SDO) pin (SDO) pin and drives high to the voltage selected by the IO_VDD_SEL pin.</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Type</td>
<td>Function</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>----------</td>
<td>----------</td>
</tr>
<tr>
<td>SCLK</td>
<td>16</td>
<td>I</td>
<td>Serial Clock Input. This pin functions as the serial clock input for both I^2C and SPI modes. This pin is internally pulled up by a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. In I^2C mode this pin should have an external pull up of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.</td>
</tr>
<tr>
<td>A0/CSb</td>
<td>19</td>
<td>I</td>
<td>Address Select 0/Chip Select. This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled up by a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit.</td>
</tr>
<tr>
<td>INTRb</td>
<td>12</td>
<td>O</td>
<td>Interrupt. This pin is asserted low when a change in device status has occurred. This interrupt has a push pull output and should be left unconnected when not in use.</td>
</tr>
<tr>
<td>RSTb</td>
<td>6</td>
<td>I</td>
<td>Device Reset. Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit.</td>
</tr>
<tr>
<td>OEb</td>
<td>11</td>
<td>I</td>
<td>Output Enable. This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use.</td>
</tr>
<tr>
<td>LOLb</td>
<td>47</td>
<td>O</td>
<td>Loss Of Lock. This output pin indicates when the DSPLL™ is locked (high) or out-of-lock (low). An external pull up or pull down is not needed.</td>
</tr>
<tr>
<td>SYNCb</td>
<td>5</td>
<td>I</td>
<td>Output Clock Synchronization. An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. For a tighter alignment of the clocks, a soft reset should be applied. This pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit and can be left unconnected when not in use.</td>
</tr>
<tr>
<td>FDEC</td>
<td>25</td>
<td>I</td>
<td>Frequency Decrement Pin. This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low with a ~20 kΩ resistor and can be left unconnected when not in use.</td>
</tr>
<tr>
<td>FINC</td>
<td>48</td>
<td>I</td>
<td>Frequency Increment Pin. This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low with a ~20 kΩ resistor and can be left unconnected when not in use.</td>
</tr>
<tr>
<td>IN_SEL0</td>
<td>3</td>
<td>I</td>
<td>Input Reference Select. The IN_SEL[1:0] pins are used in the manual pin controlled mode to select the active clock input. These pins are internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit and can be left unconnected when not in use.</td>
</tr>
<tr>
<td>IN_SEL1</td>
<td>4</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>32</td>
<td>P</td>
<td>Core Supply Voltage. The device core operates from a 1.8 V supply. A 1.0 µf bypass capacitor is recommended.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

control/status
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDA</td>
<td>13</td>
<td>P</td>
<td>Core Supply Voltage 3.3 V. This core supply pin requires a 3.3 V power source. A 1.0 µf bypass capacitor is recommended.</td>
</tr>
<tr>
<td>VDDO0</td>
<td>22</td>
<td>P</td>
<td>Output Clock Supply Voltage 0–9. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTx, OUTx outputs. See the Si5391 Family Reference Manual for power supply filtering recommendations. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.</td>
</tr>
<tr>
<td>VDDO1</td>
<td>26</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO2</td>
<td>29</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO3</td>
<td>33</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO4</td>
<td>36</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO5</td>
<td>40</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO6</td>
<td>43</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO7</td>
<td>49</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO8</td>
<td>52</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>VDDO9</td>
<td>57</td>
<td>P</td>
<td></td>
</tr>
<tr>
<td>GND PAD</td>
<td></td>
<td>P</td>
<td>Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plan as short as possible.</td>
</tr>
</tbody>
</table>

Note:

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
10. Package Outlines

10.1 Si5391 9x9 mm 64-QFN Package Diagram

The figure below illustrates the package details for the Si5391. The table below lists the values for the dimensions shown in the illustration.

![Si5391 9x9 mm 64-QFN Package Diagram](image)

**Figure 10.1. 64-Pin Quad Flat No-Lead (QFN)**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.80</td>
<td>0.85</td>
<td>0.90</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.02</td>
<td>0.05</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td>9.00 BSC</td>
</tr>
<tr>
<td>D2</td>
<td>5.10</td>
<td>5.20</td>
<td>5.30</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>0.50 BSC</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>9.00 BSC</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>5.10</td>
<td>5.20</td>
<td>5.30</td>
</tr>
<tr>
<td>L</td>
<td>0.30</td>
<td>0.40</td>
<td>0.50</td>
</tr>
<tr>
<td>aaa</td>
<td>—</td>
<td>—</td>
<td>0.15</td>
</tr>
<tr>
<td>bbb</td>
<td>—</td>
<td>—</td>
<td>0.10</td>
</tr>
<tr>
<td>ccc</td>
<td>—</td>
<td>—</td>
<td>0.08</td>
</tr>
<tr>
<td>ddd</td>
<td>—</td>
<td>—</td>
<td>0.10</td>
</tr>
<tr>
<td>eee</td>
<td>—</td>
<td>—</td>
<td>0.05</td>
</tr>
</tbody>
</table>

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
11. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration.

![PCB Land Pattern Diagram]

**Figure 11.1. PCB Land Pattern**
Table 11.1. PCB Land Pattern Dimensions

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Si5391 (Max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>8.90</td>
</tr>
<tr>
<td>C2</td>
<td>8.90</td>
</tr>
<tr>
<td>E</td>
<td>0.50</td>
</tr>
<tr>
<td>X1</td>
<td>0.30</td>
</tr>
<tr>
<td>Y1</td>
<td>0.85</td>
</tr>
<tr>
<td>X2</td>
<td>5.30</td>
</tr>
<tr>
<td>Y2</td>
<td>5.30</td>
</tr>
</tbody>
</table>

Notes:

**General**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

**Solder Mask Design**
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3×3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

**Card Assembly**
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
## 12. Top Marking

![Si5391 Top Marking](image)

**Figure 12.1. Si5391 Top Marking**

<table>
<thead>
<tr>
<th>Line</th>
<th>Characters</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1    | Si5391g-   | Base part number and Device Grade for Low Jitter, Any-Frequency, 12-output Clock Generator.  
Si5391: 10-output, 64-QFN  
– = Dash character. |
| 2    | Rxxxxx-GM  | R = Product revision. (See ordering guide for current revision).  
xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices.  
Characters are not included for standard, factory default configured devices. See Ordering Guide for more information.  
–GM = Package (QFN) and temperature range (–40 to +85 °C) |
| 3    | YYWWTTTTTTT| YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly.  
TTTTTT = Manufacturing trace code. |
| 4    | Circle w/ 1.6 mm (64-QFN) diameter | Pin 1 indicator; left-justified |
|      | TW         | TW = Taiwan; Country of Origin (ISO Abbreviation) |
13. Device Errata

Please log in or register at www.silabs.com to access the device errata document.
14. Revision History

Revision 0.7
June 2018
• Initial release.
ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
www.silabs.com/timing

SW/HW
www.silabs.com/CBPro

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

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