Si541 Ultra Series 発振器
Si541 データ・シート

超低ジッタ・デュアル任意周波数 X0 (125 fs)、0.2 ～ 1500 MHz

Si541 Ultra Series 発振器は Silicon Labs の高度な第 4 世代 DSPLL テクノロジーを使用し、超低ジッタ、低位相ノイズのクロックを選択可能な 2 つの周波数で実現します。デバイスは、0.2 ～ 1500 MHz の選択可能な任意の 2 つの周波数に対応するよう、1 ppb 未満の分解能で工場出荷時にプログラムされ、動作範囲全体の数周波数と数周波数両方で非常に低いジッタを維持します。Si541 は優れた信頼性と周波数の安定性を提供し、長年にわたる性能も保証されています。オンチップの電源フィルタリングにより、業界最先端の電源ノイズ除去性能を実現しており、スイッチング方式の電源を使用するノイズの多いシステムで、超低ジッタ・クロックの生成タスクを簡素化します。Si541 は業界標準のフットプリントで提供され、サプライチェーンが非常に簡素化されているため、Si541 はカスタム周波数のサンプルを受注後 1 ~ 2 週間で出荷できます。出力周波数ごとに異なる水晶が必要な従来の XO とは異なり、Si541 は 1つの簡単な水晶と DSPLL IC ベースのアプローチで必要な出力周波数を生成します。このプロセスでは、各デバイスの 100% 電気的試験も実施しています。Si541 は、周波数、出力形態、OE ピン配列/極性など、幅広いユーザ仕様に合わせて工場出荷時に構成されています。カスタム発振器に伴う長いリードタイムを排除するために、固有の構成は工場出荷時にプログラムされています。

主な機能
- 0.2 MHz ～ 1500 MHz の選択可能な任意の 2 つの周波数で利用可能
- 超低ジッタ: 125 fs (標準値) RMS (12 kHz ～ 20 MHz)
- 優れた PSNR および電源ノイズ耐久性: -80 dBC (標準値)
- 7 ppm 安定性オプション (−40 ～ 85 ℃)
- 同じ部品番号から、3.3 V、2.5 V および 1.8 V VDD の電源動作
- LVPECL、LVDS、CML、HCSL、CMOS、およびデュアル CMOS 出力オプション
- 2.5×3.2、3.2×5、5×7 mm パッケージ・フットプリント
- 1 ～ 2 週間のリード・タイムで任意のカスタム周波数を提供

アプリケーション
- 100G/200G/400G OTN、コヒーレント光学
- 106/40G/100G 光イーサネット
- 3G-SDI/12G-SDI/24G-SDI 放送ビデオ
- サーバ、スイッチ、ストレージ、NIC、検索の高速化
- テストおよび測定
- クロックおよびデータ・リカバリ
- FPGA/ASIC クロッキング

ピン番号 説明
---|---
1, 2 | 発注オプションにより選択可能
   | OE = 出力イネーブル、FS = 周波数選択
3 | GND = グランド
4 | CLK+ = クロック出力
5 | CLK- = 相補クロック出力。CMOS には未使用。
6 | VDD = 電源
1. Ordering Guide

The Si541 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.

### Ordering Guide

<table>
<thead>
<tr>
<th>XO Series</th>
<th>Description</th>
<th>Temp Stability</th>
<th>Total Stability</th>
<th>Package</th>
<th>Temperature Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>541</td>
<td>Dual Frequency</td>
<td>A ± 20 ppm</td>
<td>± 50 ppm</td>
<td>A 5x7 mm</td>
<td>±40 to 85 °C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B ± 10 ppm</td>
<td>± 25 ppm</td>
<td>B 3.2x5 mm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C ± 7 ppm</td>
<td>± 20 ppm</td>
<td>C 2.5x3.2 mm</td>
<td></td>
</tr>
</tbody>
</table>

### Frequency Code

```
xxxxxx
```

Two unique frequencies can be specified within the supported range of the selected signal format. Either frequency can be assigned to FS=0 or FS=1. A six digit numeric code will be assigned for the specific combination of frequencies.

### Notes:

1. Contact Silicon Labs for non-standard configurations.
2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.

1.1 Technical Support

<table>
<thead>
<tr>
<th>Frequently Asked Questions (FAQ)</th>
<th><a href="http://www.silabs.com/Si541-FAQ">www.silabs.com/Si541-FAQ</a></th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Phase Noise Lookup Utility</td>
<td><a href="http://www.silabs.com/oscillator-phase-noise-lookup">www.silabs.com/oscillator-phase-noise-lookup</a></td>
</tr>
<tr>
<td>Quality and Reliability</td>
<td><a href="http://www.silabs.com/quality">www.silabs.com/quality</a></td>
</tr>
<tr>
<td>Development Kits</td>
<td><a href="http://www.silabs.com/oscillator-tools">www.silabs.com/oscillator-tools</a></td>
</tr>
</tbody>
</table>
## 2. Electrical Specifications

### Table 2.1. Electrical Specifications

\( V_{DD} = 1.8 \text{ V}, 2.5 \text{ or } 3.3 \text{ V } \pm 5\%, \ T_A = -40 \text{ to } 85 \text{ °C} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition/Comment</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Range</td>
<td>( T_A )</td>
<td></td>
<td>(-40)</td>
<td>—</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>( F_{CLK} )</td>
<td>LVPECL, LVDS, CML</td>
<td>0.2</td>
<td>—</td>
<td>1500</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL</td>
<td>0.2</td>
<td>—</td>
<td>400</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS, Dual CMOS</td>
<td>0.2</td>
<td>—</td>
<td>250</td>
<td>MHz</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{DD} )</td>
<td>3.3 V</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5 V</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8 V</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>( I_{DD} )</td>
<td>LVPECL (output enabled)</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS/CML (output enabled)</td>
<td>—</td>
<td>75</td>
<td>111</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL (output enabled)</td>
<td>—</td>
<td>80</td>
<td>125</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS (output enabled)</td>
<td>—</td>
<td>74</td>
<td>108</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dual CMOS (output enabled)</td>
<td>—</td>
<td>80</td>
<td>125</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tristate Hi-Z (output disabled)</td>
<td>—</td>
<td>64</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Temperature Stability</td>
<td></td>
<td>Frequency stability Grade A</td>
<td>(-20)</td>
<td>—</td>
<td>20</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency stability Grade B</td>
<td>(-10)</td>
<td>—</td>
<td>10</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency stability Grade C</td>
<td>(-7)</td>
<td>—</td>
<td>7</td>
<td>ppm</td>
</tr>
<tr>
<td>Total Stability(^1)</td>
<td>( F_{STAB} )</td>
<td>Frequency stability Grade A</td>
<td>(-50)</td>
<td>—</td>
<td>50</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency stability Grade B</td>
<td>(-25)</td>
<td>—</td>
<td>25</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency stability Grade C</td>
<td>(-20)</td>
<td>—</td>
<td>20</td>
<td>ppm</td>
</tr>
<tr>
<td>Rise/Fall Time (20% to 80% ( V_{PP} ))</td>
<td>( T_{R/T_F} )</td>
<td>LVPECL/LVDS/CML</td>
<td>—</td>
<td>—</td>
<td>350</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS / Dual CMOS, ( (C_L = 5 \text{ pF}) )</td>
<td>—</td>
<td>0.5</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCSL, ( F_{CLK} &gt; 50 \text{ MHz} )</td>
<td>—</td>
<td>—</td>
<td>550</td>
<td>ps</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>( D_C )</td>
<td>All formats</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Output Enable (OE) Frequency Select (FS)(^2)</td>
<td>( V_{IH} )</td>
<td>0.7 × ( V_{DD} )</td>
<td>—</td>
<td>—</td>
<td>( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IL} )</td>
<td>—</td>
<td>—</td>
<td>0.3 × ( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_D )</td>
<td>Output Disable Time, ( F_{CLK} &gt; 10 \text{ MHz} )</td>
<td>—</td>
<td>—</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_E )</td>
<td>Output Enable Time, ( F_{CLK} &gt; 10 \text{ MHz} )</td>
<td>—</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_{FS} )</td>
<td>Settling Time after FS Change</td>
<td>—</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>Powerup Time</td>
<td>( t_{OSC} )</td>
<td>Time from 0.9 × ( V_{DD} ) until output frequency (( F_{CLK} )) within spec</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>LVPECL Output Option(^3)</td>
<td>( V_{OC} )</td>
<td>Mid-level</td>
<td>( V_{DD} - 1.42 )</td>
<td>—</td>
<td>( V_{DD} - 1.25 )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Swing (diff)</td>
<td>1.1</td>
<td>—</td>
<td>1.9</td>
<td>( V_{PP} )</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition/Comment</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>--------</td>
<td>----------------------------------------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>LVDS Output Option</td>
<td></td>
<td>Mid-level (2.5 V, 3.3 V VDD)</td>
<td>1.125</td>
<td>1.20</td>
<td>1.275</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mid-level (1.8 V VDD)</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OC</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Swing (diff)</td>
<td>0.5</td>
<td>0.7</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td>HCSL Output Option</td>
<td></td>
<td>Output voltage high</td>
<td>660</td>
<td>750</td>
<td>850</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output voltage low</td>
<td>−150</td>
<td>0</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Crossing voltage</td>
<td>250</td>
<td>350</td>
<td>550</td>
<td>mV</td>
</tr>
<tr>
<td>CML Output Option (AC-Coupled)</td>
<td></td>
<td>Swing (diff)</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>CMOS Output Option</td>
<td></td>
<td>OH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = 8/6/4 mA for 3.3/2.5/1.8 V VDD</td>
<td>0.85 × V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.15 × V&lt;sub&gt;DD&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

**Notes:**
1. Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high. Includes a 50 kΩ pull-down to GND for OE active low. FS includes a 50 kΩ pull-up to VDD.
3. 50 Ω to V<sub>DD</sub> – 2.0 V.
4. R<sub>term</sub> = 100 Ω (differential).
5. 50 Ω to GND.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition/Comment</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Jitter (RMS, 12kHz - 20MHz)&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td>Differential Formats</td>
<td>—</td>
<td>125</td>
<td>200</td>
<td>fs</td>
</tr>
<tr>
<td>2.5 x 3.2 mm, 3.2 x 5 mm, F&lt;sub&gt;CLK&lt;/sub&gt; ≥ 100 MHz</td>
<td></td>
<td>CMOS, Dual CMOS</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>fs</td>
</tr>
<tr>
<td>Phase Jitter (RMS, 12kHz - 20MHz)&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td>Differential Formats</td>
<td>—</td>
<td>150</td>
<td>200</td>
<td>fs</td>
</tr>
<tr>
<td>5 x 7 mm, F&lt;sub&gt;CLK&lt;/sub&gt; ≥ 100 MHz</td>
<td></td>
<td>CMOS, Dual CMOS</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>fs</td>
</tr>
<tr>
<td>Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output</td>
<td>PSNR</td>
<td>100 kHz sine wave</td>
<td>—</td>
<td>-83</td>
<td>—</td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200 kHz sine wave</td>
<td>—</td>
<td>-83</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 kHz sine wave</td>
<td>—</td>
<td>-82</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz sine wave</td>
<td>—</td>
<td>-85</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
Table 2.3. 3.2 x 5 mm Clock Output Phase Noise (Typical, 50ppm Total Stability Option)

<table>
<thead>
<tr>
<th>Offset Frequency (f)</th>
<th>Offset Frequency (f)</th>
<th>156.25 MHz LVDS</th>
<th>200 MHz LVDS</th>
<th>644.53125 MHz LVDS</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 Hz</td>
<td>–110</td>
<td>–107</td>
<td>–99</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 kHz</td>
<td>–121</td>
<td>–120</td>
<td>–109</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 kHz</td>
<td>–132</td>
<td>–130</td>
<td>–121</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 kHz</td>
<td>–139</td>
<td>–137</td>
<td>–127</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>1 MHz</td>
<td>–151</td>
<td>–149</td>
<td>–138</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 MHz</td>
<td>–160</td>
<td>–161</td>
<td>–155</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 MHz</td>
<td>–161</td>
<td>–162</td>
<td>–157</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

Figure 2.1. Phase Jitter vs. Output Frequency
### Table 2.4. Environmental Compliance and Package Information

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solderability</td>
<td>MIL-STD-883, Method 2003</td>
</tr>
<tr>
<td>Gross and Fine Leak</td>
<td>MIL-STD-883, Method 1014</td>
</tr>
<tr>
<td>Resistance to Solder Heat</td>
<td>MIL-STD-883, Method 2036</td>
</tr>
<tr>
<td>Moisture Sensitivity Level (MSL): 3.2x5, 5x7 packages</td>
<td>1</td>
</tr>
<tr>
<td>Moisture Sensitivity Level (MSL): 2.5x3.2 package</td>
<td>2</td>
</tr>
<tr>
<td>Contact Pads</td>
<td>Gold over Nickel</td>
</tr>
</tbody>
</table>

**Note:**
1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: [www.silabs.com/support/quality/Pages/RoHSInformation.aspx](http://www.silabs.com/support/quality/Pages/RoHSInformation.aspx).

### Table 2.5. Thermal Conditions

Max Junction Temperature = 125° C

<table>
<thead>
<tr>
<th>Package</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 x 3.2 mm 6-pin DFN</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>Θ_{JA}</td>
<td>Still Air, 85 °C</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Board</td>
<td>Ψ_{JB}</td>
<td>Still Air, 85 °C</td>
<td>39</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Top Center</td>
<td>Ψ_{JT}</td>
<td>Still Air, 85 °C</td>
<td>17</td>
<td>°C/W</td>
</tr>
<tr>
<td>3.2 x 5 mm 6-pin CLCC</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>Θ_{JA}</td>
<td>Still Air, 85 °C</td>
<td>55</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Board</td>
<td>Ψ_{JB}</td>
<td>Still Air, 85 °C</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Top Center</td>
<td>Ψ_{JT}</td>
<td>Still Air, 85 °C</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td>5 x 7 mm 6-pin CLCC</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>Θ_{JA}</td>
<td>Still Air, 85 °C</td>
<td>53</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Board</td>
<td>Ψ_{JB}</td>
<td>Still Air, 85 °C</td>
<td>26</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal Parameter Junction to Top Center</td>
<td>Ψ_{JT}</td>
<td>Still Air, 85 °C</td>
<td>26</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Note:**
1. Based on PCB Dimensions: 4.5" x 7", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.

### Table 2.6. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Operating Temp.</td>
<td>T_{AMAX}</td>
<td>95</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_{S}</td>
<td>--55 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>V_{DD}</td>
<td>--0.5 to 3.8</td>
<td>°C</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>V_{IN}</td>
<td>--0.5 to V_{DD} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>ESD HBM (JESD22-A114)</td>
<td>HBM</td>
<td>2.0</td>
<td>kV</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Rating</td>
<td>Unit</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>---------</td>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>Solder Temperature(^2)</td>
<td>T(_{\text{PEAK}})</td>
<td>260</td>
<td>ºC</td>
</tr>
<tr>
<td>Solder Time at T(_{\text{PEAK}})(^2)</td>
<td>T(_{P})</td>
<td>20–40</td>
<td>sec</td>
</tr>
</tbody>
</table>

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.
3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si541 device.

Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs
4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

![AC-Coupled LVPECL – Thevenin Termination](image1)

![DC-Coupled LVPECL – Thevenin Termination](image2)

![AC-Coupled LVPECL - 50 Ω w/VTT Bias](image3)

![DC-Coupled LVPECL - 50 Ω w/VTT Bias](image4)

**Figure 4.1. LVPECL Output Terminations**

<table>
<thead>
<tr>
<th>VDD</th>
<th>AC Coupled LVPECL Termination Resistor Values</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R1</td>
</tr>
<tr>
<td>3.3 V</td>
<td>127 Ω</td>
</tr>
<tr>
<td>2.5 V</td>
<td>250 Ω</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VDD</th>
<th>DC Coupled LVPECL Termination Resistor Values</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R1</td>
</tr>
<tr>
<td>3.3 V</td>
<td>127 Ω</td>
</tr>
<tr>
<td>2.5 V</td>
<td>250 Ω</td>
</tr>
</tbody>
</table>
Figure 4.2. LVDS and HCSL Output Terminations

DC-Coupled LVDS

AC-Coupled LVDS

Source Terminated HCSL

Destination Terminated HCSL

CML Termination without VCM

CML Termination with VCM

Single CMOS Termination

Dual CMOS Termination

Figure 4.3. CML and CMOS Output Terminations
5. Package Outline

5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si541. The table below lists the values for the dimensions shown in the illustration.

![Si541 (5×7 mm) Outline Diagram](image)

**Table 5.1. Package Diagram Dimensions (mm)**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Dimension</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.13</td>
<td>1.28</td>
<td>1.43</td>
<td>L</td>
<td>1.17</td>
<td>1.27</td>
<td>1.37</td>
</tr>
<tr>
<td>A2</td>
<td>0.50</td>
<td>0.55</td>
<td>0.60</td>
<td>L1</td>
<td>0.05</td>
<td>0.10</td>
<td>0.15</td>
</tr>
<tr>
<td>A3</td>
<td>0.50</td>
<td>0.55</td>
<td>0.60</td>
<td>p</td>
<td>1.70</td>
<td>—</td>
<td>1.90</td>
</tr>
<tr>
<td>b</td>
<td>1.30</td>
<td>1.40</td>
<td>1.50</td>
<td>R</td>
<td>0.70</td>
<td>REF</td>
<td></td>
</tr>
<tr>
<td>c</td>
<td>0.50</td>
<td>0.60</td>
<td>0.70</td>
<td>aaa</td>
<td>0.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>5.00</td>
<td></td>
<td>BSC</td>
<td>bbb</td>
<td>0.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>4.30</td>
<td>4.40</td>
<td>4.50</td>
<td>ccc</td>
<td>0.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>2.54</td>
<td></td>
<td>BSC</td>
<td>ddd</td>
<td>0.10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>7.00</td>
<td></td>
<td>BSC</td>
<td>eee</td>
<td>0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>6.10</td>
<td>6.20</td>
<td>6.30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si541. The table below lists the values for the dimensions shown in the illustration.

![Si541 (3.2×5 mm) Outline Diagram](image)

**Figure 5.2. Si541 (3.2×5 mm) Outline Diagram**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.06</td>
<td>1.17</td>
<td>1.33</td>
</tr>
<tr>
<td>b</td>
<td>0.54</td>
<td>0.64</td>
<td>0.74</td>
</tr>
<tr>
<td>c</td>
<td>0.35</td>
<td>0.45</td>
<td>0.55</td>
</tr>
<tr>
<td>D</td>
<td>3.20</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>2.55</td>
<td>2.60</td>
<td>2.65</td>
</tr>
<tr>
<td>e</td>
<td>1.27</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>5.00</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>4.35</td>
<td>4.40</td>
<td>4.45</td>
</tr>
<tr>
<td>H</td>
<td>0.45</td>
<td>0.55</td>
<td>0.65</td>
</tr>
<tr>
<td>L</td>
<td>0.80</td>
<td>0.90</td>
<td>1.00</td>
</tr>
<tr>
<td>L1</td>
<td>0.05</td>
<td>0.10</td>
<td>0.15</td>
</tr>
<tr>
<td>p</td>
<td>1.36</td>
<td>1.46</td>
<td>1.56</td>
</tr>
<tr>
<td>R</td>
<td></td>
<td>0.32</td>
<td>REF</td>
</tr>
<tr>
<td>aaa</td>
<td></td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>bbb</td>
<td></td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>ccc</td>
<td></td>
<td>0.08</td>
<td></td>
</tr>
<tr>
<td>ddd</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>eee</td>
<td></td>
<td>0.05</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
5.3 Package Outline (2.5x3.2 mm)

The figure below illustrates the package details for the 2.5x3.2 mm Si541. The table below lists the values for the dimensions shown in the illustration.

![Si541 (2.5×3.2 mm) Outline Diagram](image)

**Figure 5.3. Si541 (2.5×3.2 mm) Outline Diagram**

**Table 5.3. Package Diagram Dimensions (mm)**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.90</td>
<td>0.95</td>
<td>1.00</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0.36 REF</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td></td>
<td>0.53 REF</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>0.55</td>
<td>0.60</td>
<td>0.65</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>3.2 BSC</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>2.5 BSC</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>1.10 BSC</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.65</td>
<td>0.70</td>
<td>0.75</td>
</tr>
<tr>
<td>n</td>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td>2.2 BSC</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td></td>
<td>1.589 BSC</td>
<td></td>
</tr>
<tr>
<td>aaa</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>bbb</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>ddd</td>
<td></td>
<td>0.08</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
6. PCB Land Pattern

6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si541. The table below lists the values for the dimensions shown in the illustration.

![Si541 (5×7 mm) PCB Land Pattern](image)

Table 6.1. PCB Land Pattern Dimensions (mm)

<table>
<thead>
<tr>
<th>Dimension (mm)</th>
<th>(mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>4.20</td>
</tr>
<tr>
<td>E</td>
<td>2.54</td>
</tr>
<tr>
<td>X1</td>
<td>1.55</td>
</tr>
<tr>
<td>Y1</td>
<td>1.95</td>
</tr>
</tbody>
</table>

Notes:

**General**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si541. The table below lists the values for the dimensions shown in the illustration.

![Figure 6.2. Si541 (3.2×5 mm) PCB Land Pattern](image)

<table>
<thead>
<tr>
<th>Dimension (mm)</th>
<th>C1</th>
<th>2.60</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td></td>
<td>1.27</td>
</tr>
<tr>
<td>X1</td>
<td></td>
<td>0.80</td>
</tr>
<tr>
<td>Y1</td>
<td></td>
<td>1.70</td>
</tr>
</tbody>
</table>

Notes:

**General**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
6.3 PCB Land Pattern (2.5×3.2 mm)

The figure below illustrates the 2.5×3.2 mm PCB land pattern for the Si541. The table below lists the values for the dimensions shown in the illustration.

![Figure 6.3. Si541 (2.5×3.2 mm) PCB Land Pattern](image)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
<th>Value (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>Width - leads on long sides</td>
<td>0.85</td>
</tr>
<tr>
<td>Y1</td>
<td>Height - leads on long sides</td>
<td>0.7</td>
</tr>
<tr>
<td>D1</td>
<td>Pitch in X directions of XLY1 leads</td>
<td>1.639</td>
</tr>
<tr>
<td>E1</td>
<td>Lead pitch XLY1 leads</td>
<td>1.10</td>
</tr>
</tbody>
</table>

Table 6.3. PCB Land Pattern Dimensions (mm)

Notes: The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
7. Top Marking (5x7 and 3.2x5 Packages)

The figure below illustrates the mark specification for the Si541. The table below lists the line information.

![Figure 7.1. Mark Specification](image)

Table 7.1. Si541 Top Mark Description

<table>
<thead>
<tr>
<th>Line</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1–8</td>
<td>&quot;Si541&quot;, xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si541AAA)</td>
</tr>
<tr>
<td>2</td>
<td>1–6</td>
<td>Frequency Code&lt;br&gt;(6-digit custom code as described in the Ordering Guide)</td>
</tr>
<tr>
<td>3</td>
<td>Trace Code&lt;br&gt;&lt;br&gt;Position 1</td>
<td>Pin 1 orientation mark (dot)</td>
</tr>
<tr>
<td></td>
<td>Position 2</td>
<td>Product Revision (B)</td>
</tr>
<tr>
<td></td>
<td>Position 3–5</td>
<td>Tiny Trace Code (3 alphanumeric characters per assembly release instructions)</td>
</tr>
<tr>
<td></td>
<td>Position 6–7</td>
<td>Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)</td>
</tr>
<tr>
<td></td>
<td>Position 8–9</td>
<td>Calendar Work Week number (1–53), to be assigned by assembly site</td>
</tr>
</tbody>
</table>
8. Top Marking (2.5x3.2 Package)

The figure below illustrates the mark specification for the Si541 2.5x3.2 package sizes. The table below lists the line information.

![Mark Specification](image)

**Figure 8.1. Mark Specification**

<table>
<thead>
<tr>
<th>Line</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1–6</td>
<td>B = Si541, CCCCC = Custom Mark Code</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td><strong>Trace Code</strong></td>
</tr>
<tr>
<td></td>
<td>1–6</td>
<td>6 digit trace code per assembly release instructions</td>
</tr>
<tr>
<td>3</td>
<td>Position 1</td>
<td>Pin 1 orientation mark (dot)</td>
</tr>
<tr>
<td></td>
<td>Position 2–3</td>
<td>Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)</td>
</tr>
<tr>
<td></td>
<td>Position 4–5</td>
<td>Calendar Work Week number (1–53), to be assigned by assembly site</td>
</tr>
</tbody>
</table>

**Table 8.1. Si541 Top Mark Description**
9. Revision History

Revision 1.1
November 2019
• Added 2.5x3.2 mm package option.

Revision 1.0
July 2018
• Added 20 ppm total stability option.

Revision 0.75
March 2018
• Added 25 ppm total stability option.

Revision 0.71
December 11, 2017
• Added 5x7 package and land pattern.

Revision 0.7
June 27, 2017
• Initial release.
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