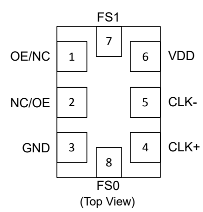
# Ultra Series™ 水晶発振器
# Si542 データ・シート

## 超低ジッタ・クワッド任意周波数 XO (125 fs)、0.2 ～ 1500 MHz

Si542 Ultra Series™ 発振器は Silicon Labs の高度な第 4 世代 DSPLL® テクノロジーを使用し、超低ジッタ、低位相ノイズのクロックを選択可能な 4 つの周波数で実現します。デバイスは、0.2 ～ 1500 MHz の選択可能な任意の 4 つの周波数に対応するよう、1 ppb 未満の分解能で工場出荷時にプログラムされ、動作範囲全体の整数周波数と分数周波数両方で非常に低いジッタを維持します。Si542 は優れた信頼性と周波数の安定性を提供し、経年的な性能も保証されています。オンチップの電源フィルタリングにより、業界最先端の電源ノイズ除去性能を実現しており、スィッチング方式の電源を使用するノイズの多いシステムで、低ジッタ・クロックの生成タスクを簡素化します。Si542 は業界標準の 3.2×5 mm および 5×7 mm フットプリントで提供され、サプライ・チェーンが非常に簡素化されているため、Silicon Labs はカスタム周波数のサンプルを受注後 1 ～ 2 週間で出荷できます。出力周波数ごとに異なる水晶が必要な従来の XO とは違い、Si542 は 1 つの簡単な水晶と DSPLL IC ベースのアプローチで必要な出力周波数を生成します。このプロセスでは、各デバイスの 100% 電気的試験も保証しています。Si542 は、周波数、出力形式、OE ピン配列/極性など、幅広いユーザ仕様に合わせて工場出荷時に構成できます。カスタム発振器に伴う長いリード・タイムを排除するために、固有の構成は工場出荷時にプログラムされています。


ピン配置




**主な機能**

- 200 kHz ～ 1500 MHz の選択可能な任意の 4 つの周波数で利用可能
- 超低ジッタ : 125 fs (標準値) RMS (12 kHz ～ 20 MHz)
- 優れた PSRR および電源ノイズ耐久性 : -80 dBc (標準値)
- 7 ppm 安定性オプション (-40 ～ 85 ° C)
- 同じ部品番号から、3.3 V、2.5 V および 1.8 V $V_{DD}$ の電源動作
- LVPECL、LVDS、CML、HCSL、CMOS、およびデュアル CMOS 出力オプション
- 3.2×5、5×7 mm パッケージ・フットプリント
- 1 ～ 2 週間のリード･タイムでサンプルを提供

**アプリケーション**

- 100G/200G/400G OTN、コヒーレント光学
- 10G/25G/40G/100G イーサネット
- 3G-SDI/12G-SDI/24G-SDI 放送ビデオ
- サーバ、スイッチ、ストレージ、NIC、検索の高速化
- テストおよび測定
- クロックおよびデータ・リカバリ
- FPGA/ASIC クロッキング

# 1. Ordering Guide

The Si542 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.

| XO Series | Description |
|---|---|
| 542 | Quad Frequency |

| | Temp Stability | Total Stability[2] |
|---|---|---|
| A | ± 20 ppm | ± 50 ppm |
| B | ± 10 ppm | ± 25 ppm |
| C | ± 7 ppm | ± 20 ppm |

| | Package |
|---|---|
| A | 5x7 mm |
| B | 3.2x5 mm |

| | Temperature Grade |
|---|---|
| G | -40 to 85 °C |

542 A A A - - - - - - A B G R

| Signal Format | VDD Range | Order Option |
|---|---|---|
| LVPECL | 2.5, 3.3 V | A |
| LVDS | 1.8, 2.5, 3.3 V | B |
| CMOS | 1.8, 2.5, 3.3 V | C |
| CML | 1.8, 2.5, 3.3 V | D |
| HCSL | 1.8, 2.5, 3.3 V | E |
| Dual CMOS (In-Phase) | 1.8, 2.5, 3.3 V | F |
| Dual CMOS (Complementary) | 1.8, 2.5, 3.3 V | G |
| Custom[1] | 1.8, 2.5, 3.3 V | X |

| | OE Pin | OE Polarity |
|---|---|---|
| A | Pin 1 | Active High |
| B | Pin 1 | Active Low |
| C | Pin 2 | Active High |
| D | Pin 2 | Active Low |

Device Revision

| | Reel |
|---|---|
| R | Tape and Reel |
| <Blank> | Coil Tape |

| Frequency Code[3] | Description |
|---|---|
| xxxxxx | Four unique frequencies can be specified within the supported range of the selected signal format. The frequencies can be arranged in any order from FS[1:0]=00 to FS[1:0]=11. A six digit numeric code will be assigned for the specific combination of frequencies. |

**Notes:**

1. Contact Silicon Labs for non-standard configurations.
2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
3. Create custom part numbers at www.silabs.com/oscillators.

## 1.1 Technical Support

| | |
|---|---|
| Frequently Asked Questions (FAQ) | www.silabs.com/Si542-FAQ |
| Oscillator Phase Noise Lookup Utility | www.silabs.com/oscillator-phase-noise-lookup |
| Quality and Reliability | www.silabs.com/quality |
| Development Kits | www.silabs.com/oscillator-tools |

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**

$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 ºC

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Range | $T_A$ | | –40 | — | 85 | ºC |
| Frequency Range | $F_{CLK}$ | LVPECL, LVDS, CML | 0.2 | — | 1500 | MHz |
| | | HCSL | 0.2 | — | 400 | MHz |
| | | CMOS, Dual CMOS | 0.2 | — | 250 | MHz |
| Supply Voltage | $V_{DD}$ | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| Supply Current | $I_{DD}$ | LVPECL (output enabled) | — | 100 | 132 | mA |
| | | LVDS/CML (output enabled) | — | 75 | 111 | mA |
| | | HCSL (output enabled) | — | 80 | 125 | mA |
| | | CMOS (output enabled) | — | 74 | 108 | mA |
| | | Dual CMOS (output enabled) | — | 80 | 125 | mA |
| | | Tristate Hi-Z (output disabled) | — | 64 | 100 | mA |
| Temperature Stability | | Frequency stability Grade A | –20 | — | 20 | ppm |
| | | Frequency stability Grade B | –10 | — | 10 | ppm |
| | | Frequency stability Grade C | –7 | — | 7 | ppm |
| Total Stability[1] | $F_{STAB}$ | Frequency stability Grade A | –50 | — | 50 | ppm |
| | | Frequency stability Grade B | –25 | — | 25 | ppm |
| | | Frequency stability Grade C | –20 | — | 20 | ppm |
| Rise/Fall Time (20% to 80% $V_{PP}$) | $T_R/T_F$ | LVPECL/LVDS/CML | — | — | 350 | ps |
| | | CMOS / Dual CMOS, ($C_L$ = 5 pF) | — | 0.5 | 1.5 | ns |
| | | HCSL, $F_{CLK}$ >50 MHz | — | — | 550 | ps |
| Duty Cycle | $D_C$ | All formats | 45 | — | 55 | % |
| Output Enable (OE) Frequency Select (FS0, FS1)[2] | $V_{IH}$ | | 0.7 × $V_{DD}$ | — | — | V |
| | $V_{IL}$ | | — | — | 0.3 × $V_{DD}$ | V |
| | $T_D$ | Output Disable Time, $F_{CLK}$ > 10 MHz | — | — | 3 | µs |
| | $T_E$ | Output Enable Time, $F_{CLK}$ > 10 MHz | — | — | 20 | µs |
| | $T_{FS}$ | Settling Time after FS Change | — | — | 10 | ms |
| Powerup Time | $t_{OSC}$ | Time from 0.9 × $V_{DD}$ until output frequency ($F_{CLK}$) within spec | — | — | 10 | ms |
| LVPECL Output Option[3] | $V_{OC}$ | Mid-level | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| | $V_O$ | Swing (diff) | 1.1 | — | 1.9 | $V_{PP}$ |

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LVDS Output Option[4] | $V_{OC}$ | Mid-level (2.5 V, 3.3 V VDD) | 1.125 | 1.20 | 1.275 | V |
| | | Mid-level (1.8 V VDD) | 0.8 | 0.9 | 1.0 | V |
| | $V_O$ | Swing (diff) | 0.5 | 0.7 | 0.9 | $V_{PP}$ |
| HCSL Output Option[5] | $V_{OH}$ | Output voltage high | 660 | 750 | 850 | mV |
| | $V_{OL}$ | Output voltage low | –150 | 0 | 150 | mV |
| | $V_C$ | Crossing voltage | 250 | 350 | 550 | mV |
| CML Output Option (AC-Coupled) | $V_O$ | Swing (diff) | 0.6 | 0.8 | 1.0 | $V_{PP}$ |
| CMOS Output Option | $V_{OH}$ | $I_{OH}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | 0.85 × $V_{DD}$ | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | — | — | 0.15 × $V_{DD}$ | V |

**Notes:**

1. Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high. Includes a 50 kΩ pull-down to GND for OE active low. FS0 and FS1 pins each include a 50 kΩ pull-up to VDD. NC (No Connect) pins include a 50 kΩ pull-down to GND.
3. 50 Ω to $V_{DD}$ – 2.0 V.
4. $R_{term}$ = 100 Ω (differential).
5. 50 Ω to GND.

**Table 2.2. Clock Output Phase Jitter and PSRR**

$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 °C

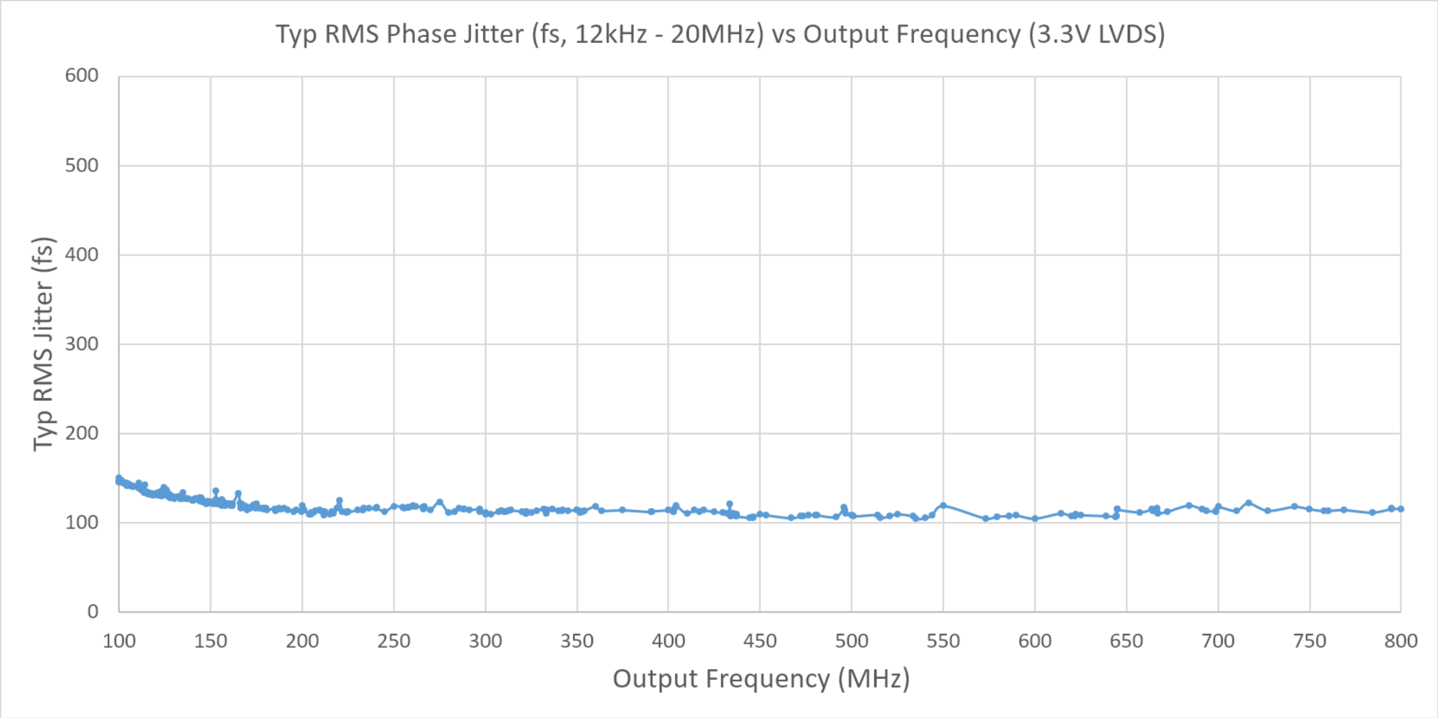
| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS, 12kHz - 20MHz)[1] 3.2 x 5 mm, $F_{CLK}$ ≥ 100 MHz | $\phi_J$ | Differential Formats | — | 125 | 200 | fs |
| | | CMOS, Dual CMOS | — | 200 | — | fs |
| Phase Jitter (RMS, 12kHz - 20MHz)[1] 5 x 7 mm, $F_{CLK}$ ≥ 100 MHz | $\phi_J$ | Differential Formats | — | 150 | 200 | fs |
| | | CMOS, Dual CMOS | — | 200 | — | fs |
| Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output | PSRR | 100 kHz sine wave | — | -83 | — | dBc |
| | | 200 kHz sine wave | — | -83 | — | |
| | | 500 kHz sine wave | — | -82 | — | |
| | | 1 MHz sine wave | — | -85 | — | |

**Note:**

1. Guaranteed by characterization. Jitter inclusive of any spurs.

**Table 2.3. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

| Offset Frequency (f) | 156.25 MHz LVDS | 200 MHz LVDS | 644.53125 MHz LVDS | Unit |
|---|---|---|---|---|
| 100 Hz | –110 | –107 | –99 | dBc/Hz |
| 1 kHz | –121 | –120 | –109 | |
| 10 kHz | –132 | –130 | –121 | |
| 100 kHz | –139 | –137 | –127 | |
| 1 MHz | –151 | –149 | –138 | |
| 10 MHz | –160 | –161 | –155 | |
| 20 MHz | –161 | –162 | –157 | |
| **Offset Frequency (f)** | **156.25 MHz LVPECL** | **200 MHz LVPECL** | **644.53125 MHz LVPECL** | **Unit** |
| 100 Hz | –113 | –110 | –100 | dBc/Hz |
| 1 kHz | –123 | –120 | –110 | |
| 10 kHz | –133 | –130 | –119 | |
| 100 kHz | –139 | –137 | –127 | |
| 1 MHz | –151 | –149 | –138 | |
| 10 MHz | –162 | –166 | –156 | |
| 20 MHz | –163 | –167 | –157 | |




Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

**Figure 2.1. Phase Jitter vs. Output Frequency**

**Table 2.4. Environmental Compliance and Package Information**

| Parameter | Test Condition |
|---|---|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Gross and Fine Leak | MIL-STD-883, Method 1014 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Moisture Sensitivity Level (MSL) | 1 |
| Contact Pads | Gold over Nickel |

**Note:**

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx.

**Table 2.5. Thermal Conditions**

| Package | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|
| 3.2×5 mm 8-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 79.1 | ºC/W |
| | Thermal Resistance Junction to Board | $\Theta_{JB}$ | Still Air, 85 °C | 49.6 | ºC/W |
| | Max Junction Temperature | $T_J$ | Still Air, 85 °C | 125 | ºC |
| 5 × 7 mm 8-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 ºC | 67.1 | ºC/W |
| | Thermal Resistance Junction to Board | $\Theta_{JB}$ | Still Air, 85 ºC | 51.7 | ºC/W |
| | Max Junction Temperature | $T_J$ | Still Air, 85 ºC | 125 | ºC |

**Table 2.6. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum Operating Temp. | $T_{AMAX}$ | 95 | ºC |
| Storage Temperature | $T_S$ | –55 to 125 | ºC |
| Supply Voltage | $V_{DD}$ | –0.5 to 3.8 | ºC |
| Input Voltage | $V_{IN}$ | –0.5 to $V_{DD}$ + 0.3 | V |
| ESD HBM (JESD22-A114) | HBM | 2.0 | kV |
| Solder Temperature[2] | $T_{PEAK}$ | 260 | ºC |
| Solder Time at $T_{PEAK}$[2] | $T_P$ | 20–40 | sec |

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

# 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si542 device.

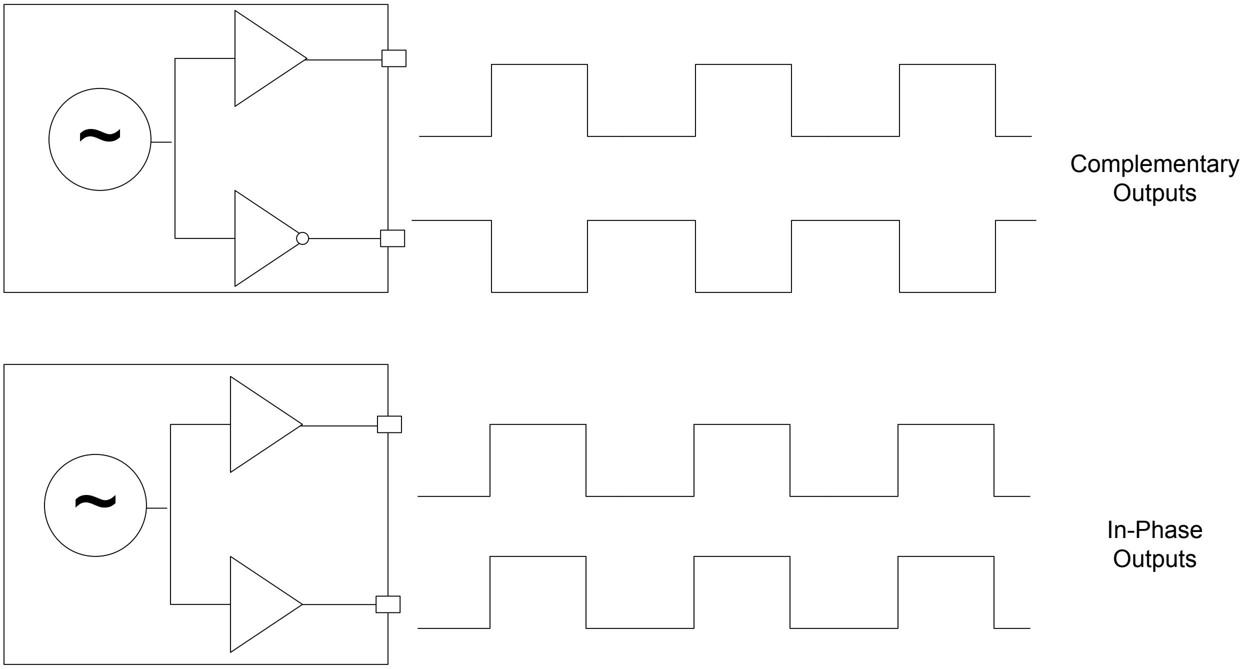



**Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

## 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

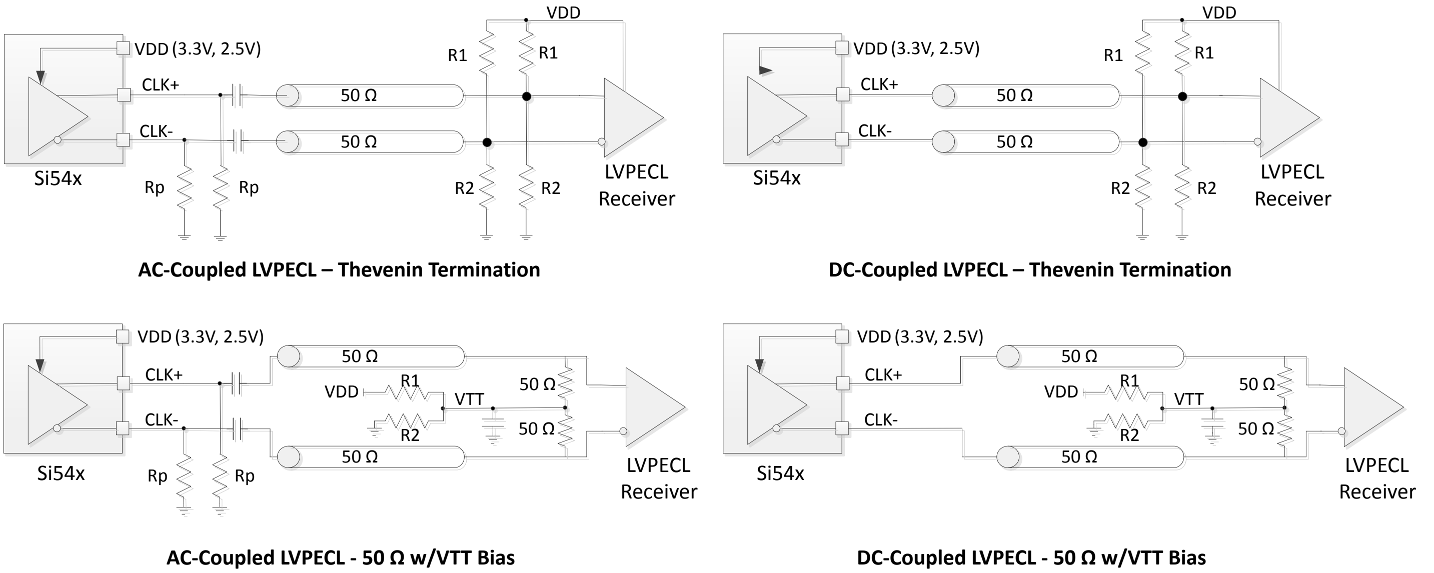



**Figure 4.1. LVPECL Output Terminations**

| AC Coupled LVPECL Termination Resistor Values | | | |
|---|---|---|---|
| **VDD** | R1 | R2 | Rp |
| **3.3 V** | 127 Ω | 82.5 Ω | 130 Ω |
| **2.5 V** | 250 Ω | 62.5 Ω | 90 Ω |

| DC Coupled LVPECL Termination Resistor Values | | |
|---|---|---|
| **VDD** | R1 | R2 |
| **3.3 V** | 127 Ω | 82.5 Ω |
| **2.5 V** | 250 Ω | 62.5 Ω |

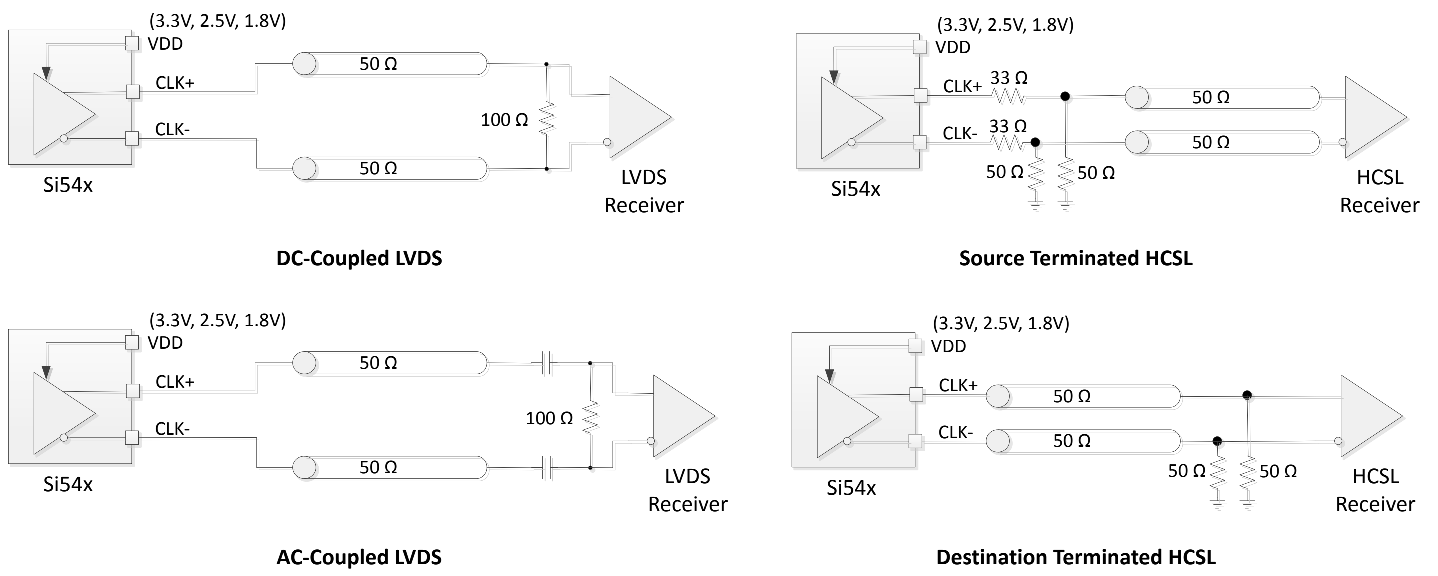



**Figure 4.2. LVDS and HCSL Output Terminations**

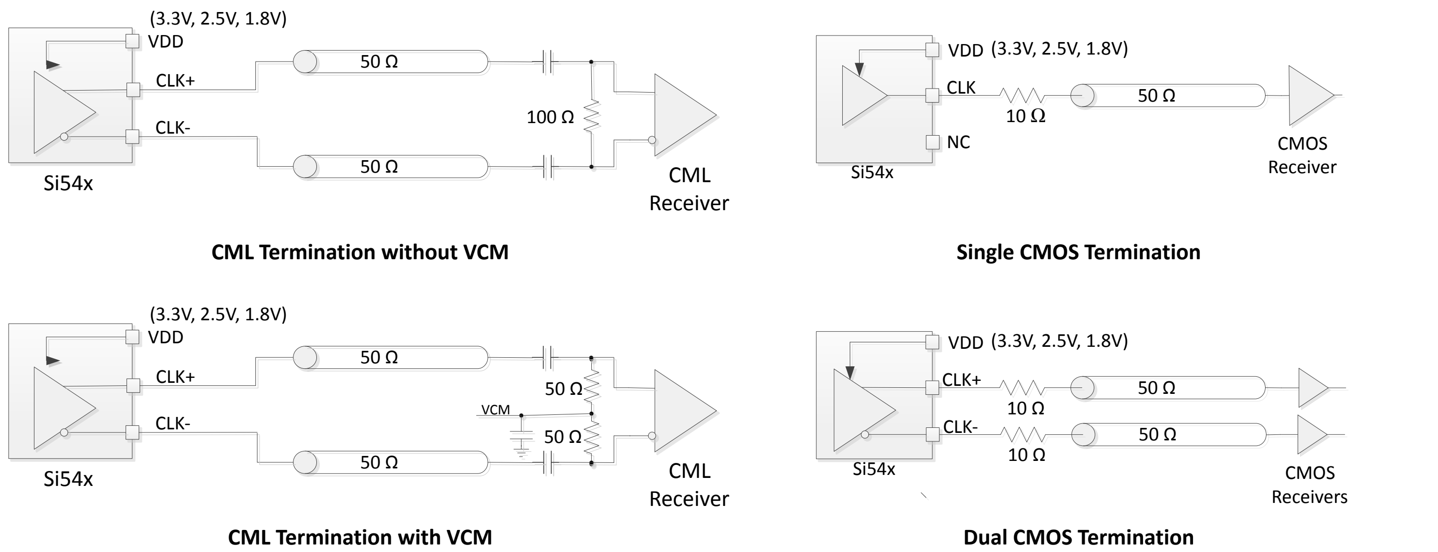



**Figure 4.3. CML and CMOS Output Terminations**

# 5. Package Outline

## 5.1 Package Outline (5x7 mm)

The figure below illustrates the package details for the 5x7 mm Si542. The table below lists the values for the dimensions shown in the illustration.

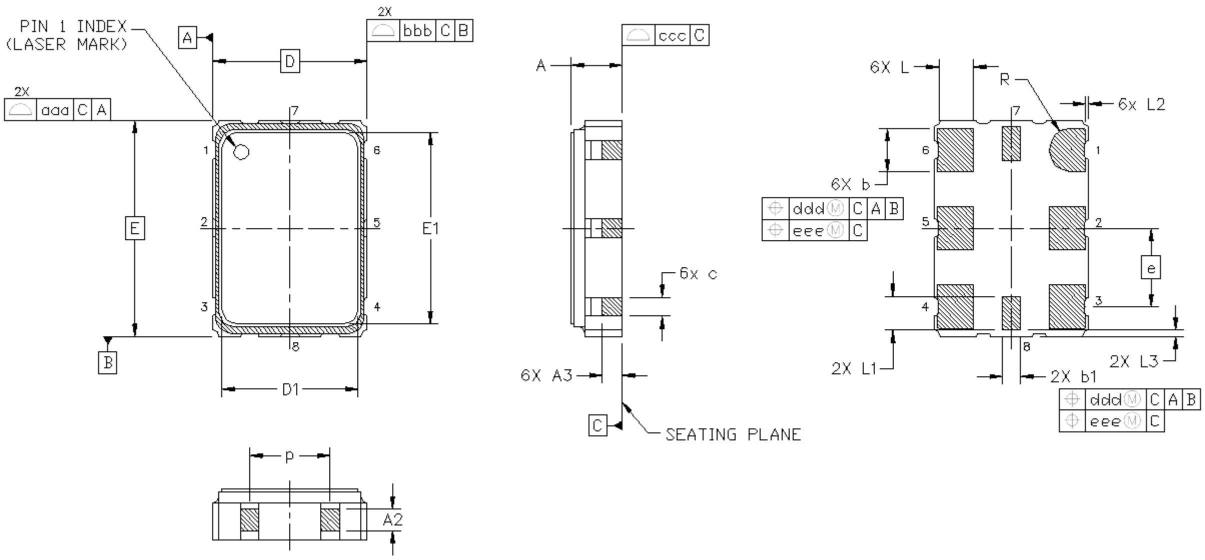



**Figure 5.1. Si542 (5x7 mm) Outline Diagram**

**Table 5.1. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max | Dimension | Min | Nom | Max |
|---|---|---|---|---|---|---|---|
| A | 1.07 | 1.18 | 1.33 | E1 | 6.10 | 6.20 | 6.30 |
| A2 | 0.40 | 0.50 | 0.60 | L | 1.07 | 1.17 | 1.27 |
| A3 | 0.45 | 0.55 | 0.65 | L1 | 1.00 | 1.10 | 1.20 |
| b | 1.30 | 1.40 | 1.50 | p | 1.70 | -- | 1.90 |
| b1 | 0.50 | 0.60 | 0.70 | R | 0.70 REF | | |
| c | 0.50 | 0.60 | 0.70 | aaa | 0.15 | | |
| D | 5.00 BSC | | | bbb | 0.15 | | |
| D1 | 4.30 | 4.40 | 4.50 | ccc | 0.08 | | |
| e | 2.54 BSC | | | ddd | 0.10 | | |
| E | 7.00 BSC | | | eee | 0.05 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

### 5.2 Package Outline (3.2x5 mm)

The figure below illustrates the package details for the 5x3.2 mm Si542. The table below lists the values for the dimensions shown in the illustration.

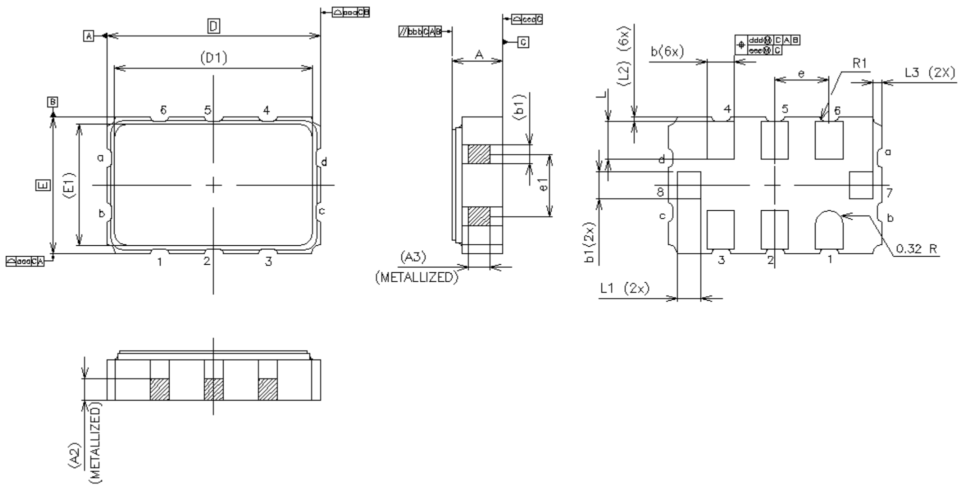



**Figure 5.2. Si542 (3.2x5 mm) Outline Diagram**

**Table 5.2. Package Diagram Dimensions (mm)**

| Dimension | MIN | NOM | MAX | | Dimension | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|---|
| A | 1.02 | 1.17 | 1.33 | | E1 | 2.85 BSC | | |
| A2 | 0.50 | 0.55 | 0.60 | | L | 0.8 | 0.9 | 1.0 |
| A3 | 0.45 | 0.50 | 0.55 | | L1 | 0.45 | 0.55 | 0.65 |
| b | 0.54 | 0.64 | 0.74 | | L2 | 0.05 | 0.10 | 0.15 |
| b1 | 0.54 | 0.64 | 0.75 | | L3 | 0.15 | 0.20 | 0.25 |
| D | 5.00 BSC | | | | aaa | 0.15 | | |
| D1 | 4.65 BSC | | | | bbb | 0.15 | | |
| e | 1.27 BSC | | | | ccc | 0.08 | | |
| e1 | 1.625 TYP | | | | ddd | 0.10 | | |
| E | 3.20 BSC | | | | eee | 0.05 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

# 6. PCB Land Pattern

## 6.1 PCB Land Pattern (5x7 mm)

The figure below illustrates the 5x7 mm PCB land pattern for the Si542. The table below lists the values for the dimensions shown in the illustration.

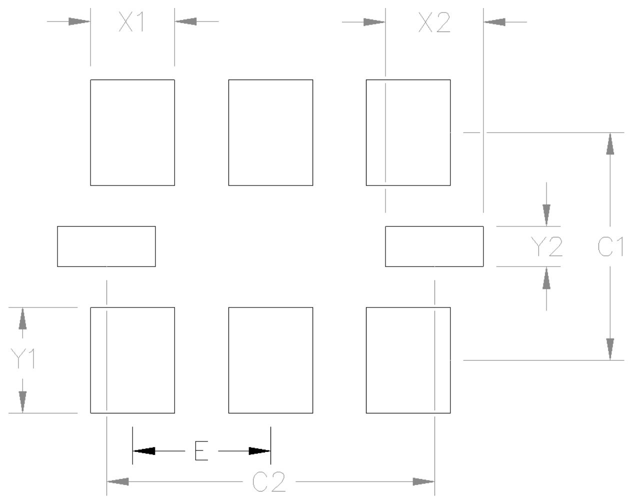



**Figure 6.1. Si542 (5x7 mm) PCB Land Pattern**

**Table 6.1. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) | | Dimension | (mm) |
|---|---|---|---|---|
| C1 | 4.20 | | Y1 | 1.95 |
| C2 | 6.05 | | X2 | 1.80 |
| E | 2.54 | | Y2 | 0.75 |
| X1 | 1.55 | | | |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

### 6.2 PCB Land Pattern (3.2x5 mm)

The figure below illustrates the 3.2x5.0 mm PCB land pattern for the Si542. The table below lists the values for the dimensions shown in the illustration.

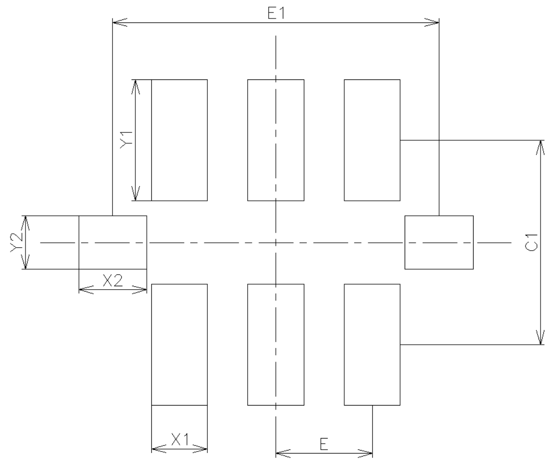



**Figure 6.2. Si542 (3.2x5 mm) PCB Land Pattern**

**Table 6.2. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) | | Dimension | (mm) |
|---|---|---|---|---|
| C1 | 2.70 | | X2 | 0.90 |
| E | 1.27 | | Y1 | 1.60 |
| E1 | 4.30 | | Y2 | 0.70 |
| X1 | 0.74 | | | |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

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**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

# 7. Top Marking

The figure below illustrates the mark specification for the Si542. The table below lists the line information.

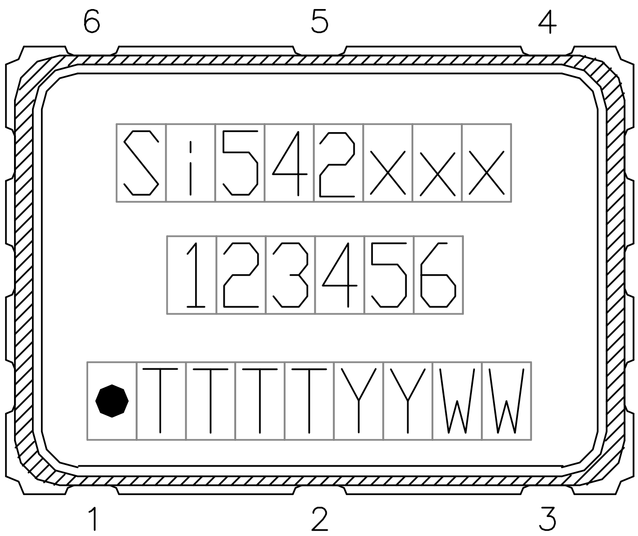


**Figure 7.1. Mark Specification**

**Table 7.1. Si542 Top Mark Description**

| Line | Position | Description |
| --- | --- | --- |
| 1 | 1–8 | "Si542", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si542AAA) |
| 2 | 1–6 | Frequency Code<br>(6-digit custom code as described in the Ordering Guide) |
| 3 | **Trace Code** | |
| | Position 1 | Pin 1 orientation mark (dot) |
| | Position 2 | Product Revision (B) |
| | Position 3–5 | Tiny Trace Code (3 alphanumeric characters per assembly release instructions) |
| | Position 6–7 | Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17) |
| | Position 8–9 | Calendar Work Week number (1–53), to be assigned by assembly site |

# 8. Revision History

**Revision 0.8**

July, 2018

- Added 20 ppm total stability option.

**Revision 0.75**

March, 2018

- Added 25 ppm total stability option.

**Revision 0.71**

December 11, 2017

- Added 5x7 package and land pattern.

**Revision 0.7**

June 27, 2017

- Initial release.


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